A 3.8–8.4 GHz 0.13 μM CMOS POWER AMPLIFIER FOR ULTRA-WIDEBAND APPLICATIONS

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ABSTRACT

Implementation of highly power-efficient transceivers has thus become a crucial research area with the move to wideband technologies. CMOS power amplifiers (PAs) are becoming an essential component of the technology mix for RF front-end devices. However, their properties could be limiting for complete system efficiency. Decreased power dissipation and less area are considered the main design challenges for portable and low-cost devices. Therefore, to increase battery lifetime and reduced cost, a high performance integrated CMOS power amplifier (PA) has been proposed in this paper. Our scheme achieves a power gain of 12.7 dB with better gain flatness of ±0.5 dB over the frequency band beginning from 3.8 GHz to 8.4 GHz, and a power dissipation of 24.8 mW with less area of 0.40 mm2, using 130 nm CMOS technology.

KEYWORDS: *CMOS power amplifiers, Common source power amplifier, Current-reused cascode topology, Gain flatness, Low-power, Power-added-efficiency (PAE), Ultra-wideband (UWB).*

I. INTRODUCTION

Ultra-wideband (UWB) is a promising radio-based communication technology for small distance coverage wireless communication interfaces which enable data transmission through a great wide frequency band beginning at 3.1 GHz and ending at 10.6 GHz with an extremely least power spectral density [1]. The UWB transmission includes very minimal effective radiated power spectral density about −41.3 dBm/MHz. The low-power transmission also enables lower power consumption in wireless communication systems and a long battery time, which are the basic requirements in different fields of applications [2, 3]. Tracking applications, medical applications, wireless body area network (WBAN) applications, smart healthcare systems, and real-world applications are several applications that demand low power dissipation, large bandwidth, and great data rate. UWB supports these requirements with a typical performance.

Power amplifier (PA) considers an essential building block within the UWB wireless transceiver [4]. CMOS power amplifiers main function is to boost the input signal power level to the demanded output power level for transmission. Several implementation schemes to raise the gain of power amplifiers over the wideband frequency spectrum have been proposed [4-29].

Trade-offs exist among several performance parameters such as gain, gain-flatness, power dissipation, area, input/output loss matching, and power-added-efficiency (PAE) while maintaining a broad frequency band. In order to achieve optimum performance requirements, several configurations to implement broad band CMOS power amplifiers have been reported [5]. Among these configurations are resistive shunt feedback configuration, staggered tuning technique, source inductive degeneration topology, and current-reuse cascode structure. These various main schemes are commonly used for wideband power amplifiers designed to address the requirements of high gain, minimum gain flatness, low power consumption, less matching loss, and high PAE.

Also, the staggered tuning technique has been employed to get gain-flatness better over a wide bandwidth. Two schemes can implement staggered tuning [11, 12]. Three-stage power amplifier

stagger tuning scheme to maximize the frequency band [11] or two-stage with interstage matching stagger tuning scheme to boost the gain-flatness [12]. This depends on adjusting the tuning midpoint frequency of each stage at different frequencies that are as away as possible to obtain a large frequency spectrum. While this configuration can widen the frequency bandwidth with acceptable gain-flatness level, the cost in area and power can be considerable.

Likewise, to obtain a better flat gain with higher linearity, the source inductive degeneration topology is utilized [13-16]. In this configuration, an inductor has been added at the source of the PA transistor to enhance linearity and gain flatness through the proposed band of frequencies. One of the drawbacks of the source inductive degeneration topology is the lower impedance matching networks of the design circuit which may result in a higher die area.

Saving power with gain flatness enhancement can be obtained by employing the current-reuse cascode configuration [17-20]. Furthermore, good isolation and significant gain and output power are achieved in the whole frequency band.

An introduction to the ultra-wideband technology (UWB) and the recent previous power amplifiers work have been introduced in section I. The proposed design is discussed in section II. Section III covers the simulation results and comparison. The conclusion of the work is presented in section IV.

II. PROPOSED CMOS POWER AMPLIFIER DESIGN

The progress in downscaling the nanotechnology CMOS transistor manufacture of integrated circuits has led to a jump in the implementation of CMOS power amplifiers by making them fully integrated with all components. Consequently, reducing energy loss and chip area has become an urgent need to keep up with the marketing requirements for different portable products and different fields of applications including the medical sector. Therefore, maintaining the battery life as long as possible is one of the greatest important requirements. Employing the cascode configuration in the implementation of PA helps reduce power consumption with higher power gain over a wideband of frequencies compared with the cascaded configuration. The current-reused cascode scheme has been utilized in the design of the proposed PA in this paper.

2.1. Conventional Cascode Configuration

Figure 1 demonstrates the schematic of the conventional cascode PA and the current-reused cascode PA. The conventional cascode scheme is composed of a current-source transistor directed by a common-gate transistor as demonstrated in figure 1(a). This configuration offers good input-output isolation which removes the Miller effect and increases stability [21-24]. CMOS M2 separates between the drain of CMOS M1 and the RF output. Although the cascode scheme provides higher power gain with typical gain bandwidth, low power consumption performance is still a challenge.

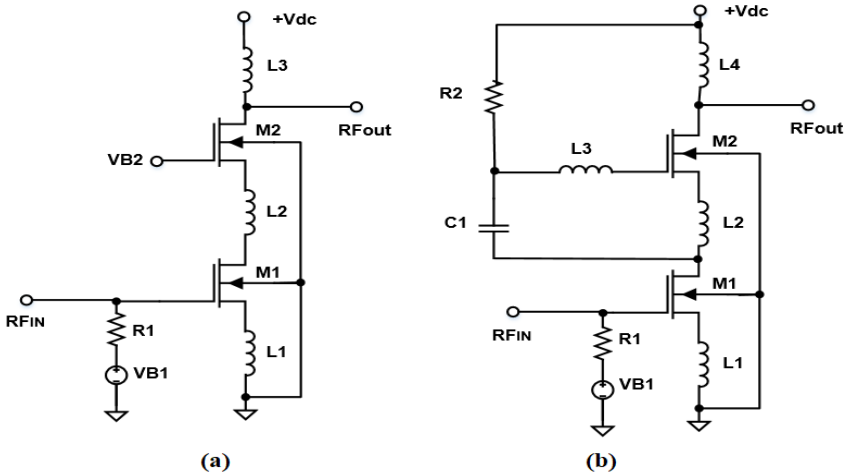

Figure 1. The cascode PA, (a) The conventional cascode PA, (b) The current-reused cascode PA.

The current-reused cascode scheme tackles this challenge by exploiting the bias share model leading to a decrease in the consumed power [25-27]. As demonstrated in figure 1(b), the output at the drain of common-source CMOS M1 is directed to the input at the gate of M2 through the path of capacitor C1 and inductor L3. This converts the common-gate CMOS M2 into a common-source configuration. Thus the two CMOS M1 and M2 share the same bias current which directed to the lowest power dissipation. At the same time, this enhances the gate flatness through a broad frequency range.

2.2. Current-Reused Cascode Configuration

The block diagram of the proposed design is described in figure 2. In order to attain higher power gain with slight ripples and the least power consumption over a broad spectrum, the current-reused cascode configuration is employed in the initial phase of the proposed power amplifier. A common-source CMOS transistor is utilized in the following phase to raise the output power and the power gain. To attain improved gain flatness on a large range of frequencies, an interstage composed of an inductor Lint and a capacitor Cint is inserted between the first phase and the second phase. The value of these components is chosen carefully to obtain good matching performance with almost flat gain.

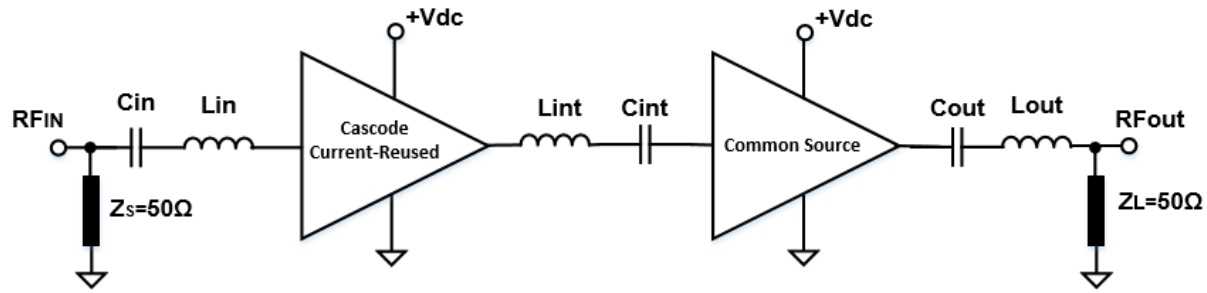

Figure 2. Block diagram of the proposed PA.

The proposed circuit design of CMOS PA is demonstrated in figure 3. The first phase PA includes the CMOS M1 and M2 with inductors L2, L3 and capacitor C2 to construct a current-reused cascode scheme.

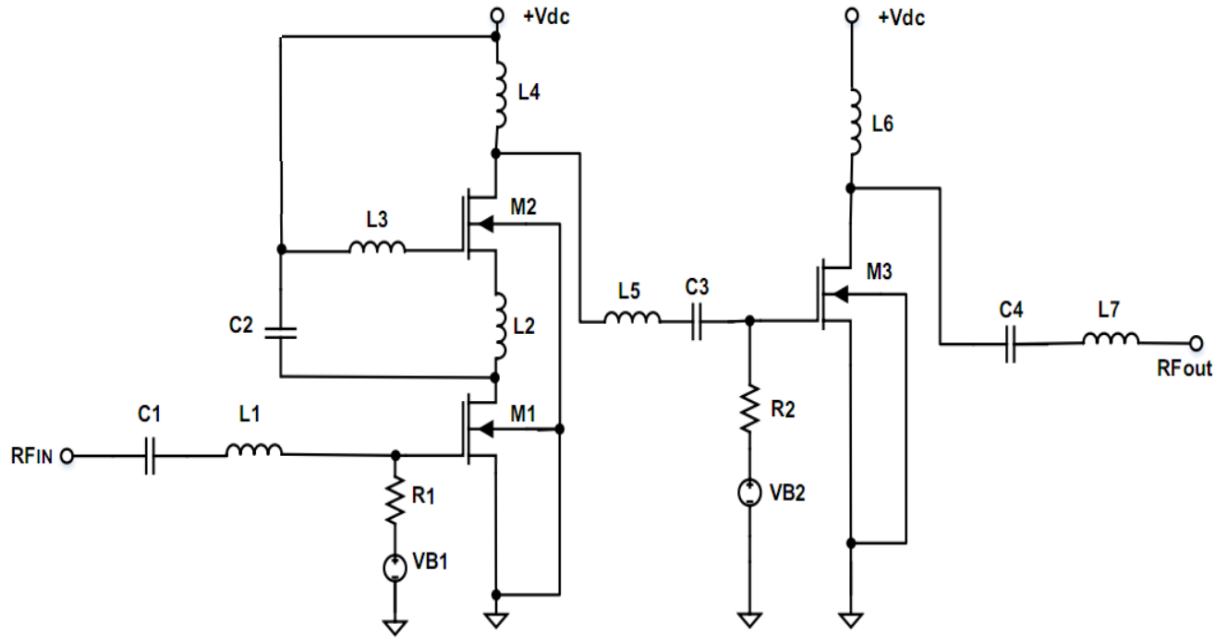

Figure 3. The proposed CMOS PA schematic.

The capacitor C1 with the inductor L1 are adjusted for a wideband input impedance matching. While the inductor L2 is added to construct a big-impedance path to prevent the signal at the required bandwidth. However, C2 and L3 establish a small-impedance path. A second phase contains a

common-source CMOS M2 employed to rise the gain and widen the bandwidth. The capacitor C3 and the inductor L5 are utilized the interstage impedance between the two stages for gain flatness over the desired frequencies of interest. The inductors L4 and L6 are the load of the first and second stages that are utilized to raise the gain on a wideband range of frequencies. Also, L6 shares the wideband output matching with the capacitor C4 and the inductor L7. The two resistance R1, and R2 are attached to bias the CMOS M1, and M3, respectively. The complete circuit component values are presented in Table 1. The proposed PA attains a high gain with the least gain flatness over a broad band of frequency. Furthermore, low power consumption with higher PAE is achieved as presented in the next section.

Table 1. Parameters value of the proposed power amplifier

Design Parameters	Values	Design Parameters	Values
M1	L = 0.12 µm, W = 70 µm	L1	1.5 nH
M2	L = 0.12 µm, W = 40 µm	L2	1 nH
M3	L = 0.12 µm, W = 50 µm	L3	370 pH
C1	1 pF	L4	4.2 nH
C2	105 fF	L5	370 pH
C3	500 fF	L6	4.2 nH
C4	450 fF	L7	630 pH
R1	200 Ω	R2	130 Ω

III. SIMULATION RESULTS AND COMPARISON

Figures 4-7 show the correspondence between the pre-and post-layout performance parameters using Cadence Spectre. The proposed PA is simulated in UMC 0.13-µm CMOS technology with a 1.2 V DC power supply, achieving a power consumption of 24.8 mW. Compared with the recent previous works is reported in Table 2.

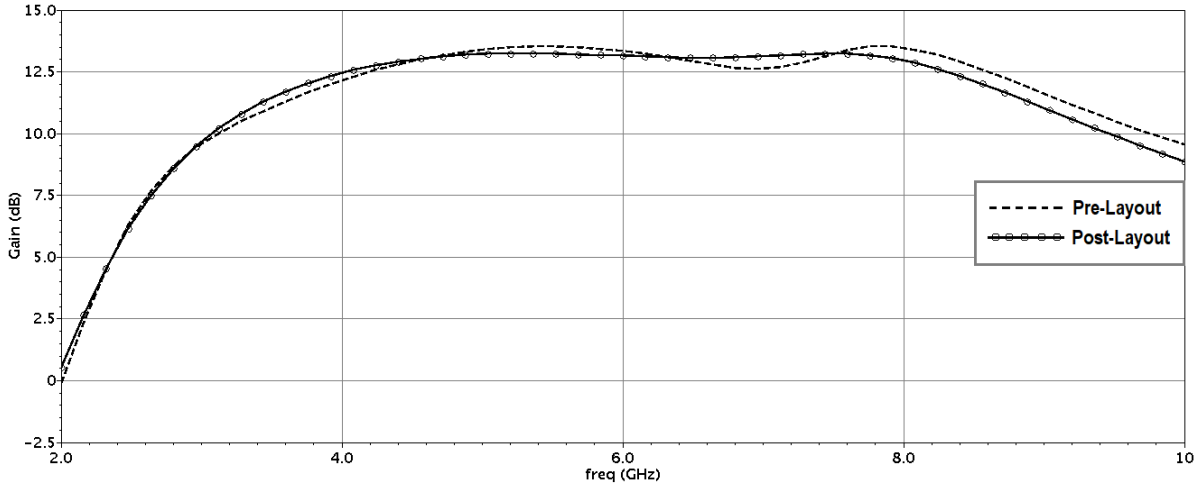

Figure 4. Pre- and post-layout S21 of the proposed CMOS PA.

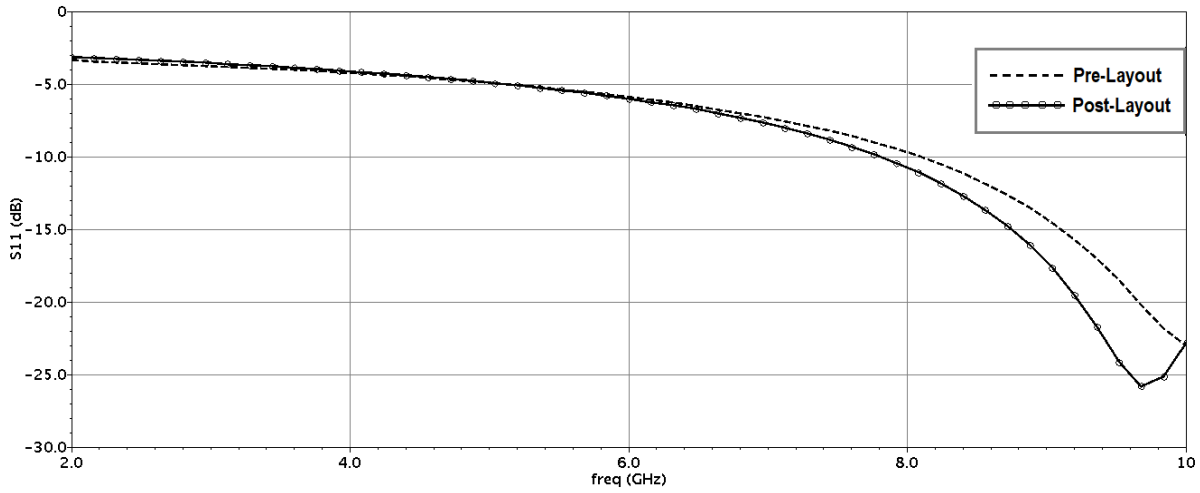

Figure 5. Pre- and post-layout S11 of the proposed CMOS PA.

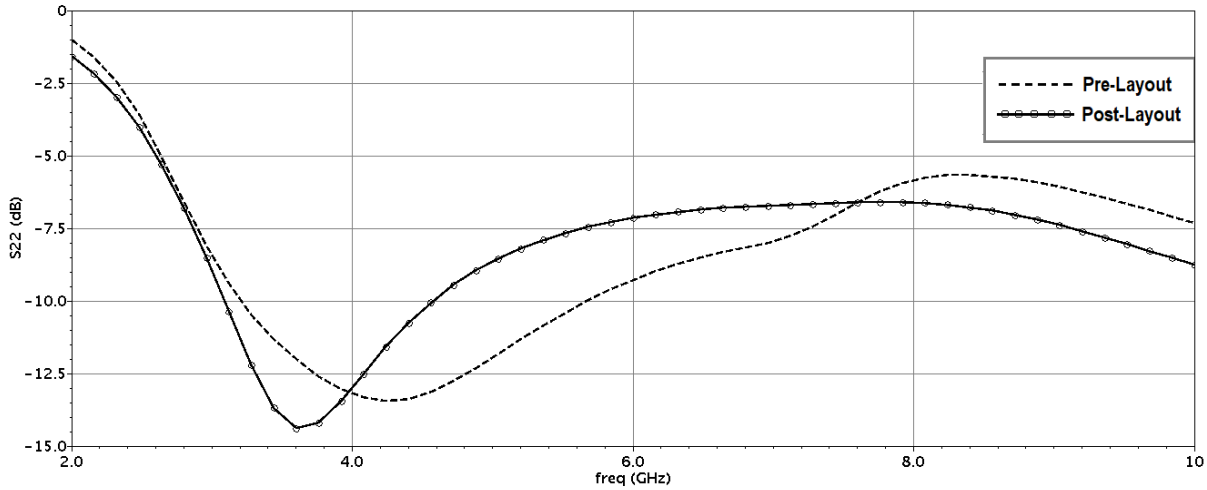

Figure 6. Pre- and post-layout S22 of the proposed CMOS PA.

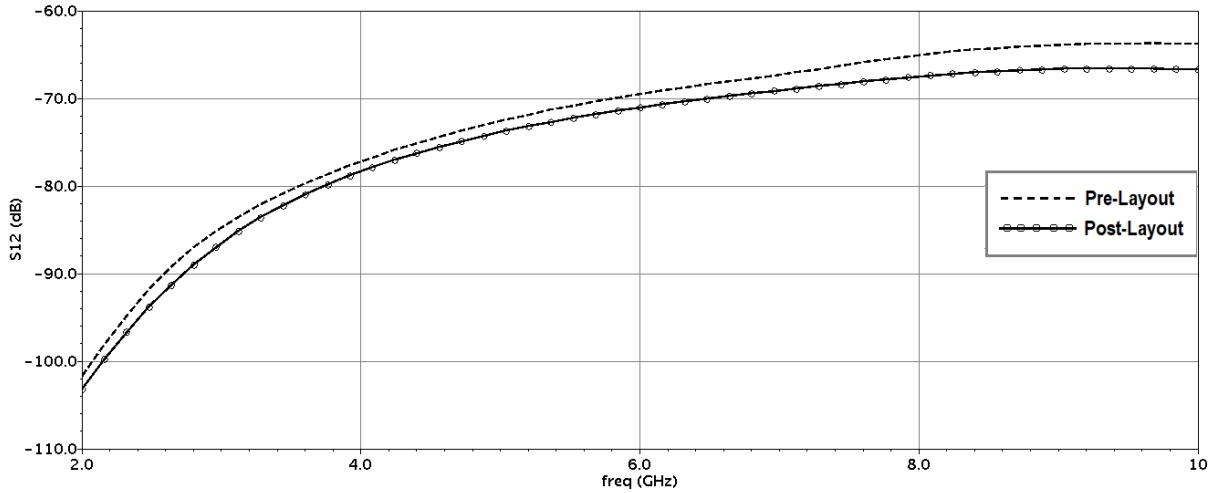

Figure 7. Pre- and post-layout S12 of the proposed CMOS PA.

The proposed PA achieves high power gain (S21) and great gain flatness of 12.7±0.5 dB through a high frequency band of 3.8-8.4 GHz as demonstrated in figure 4. The S-parameters (S11), (S22), and (S12) are demonstrated in figures 5-7. It is found that S11 is lower than -5 dB, S22 is below -6.6 dB, and S12 is less than -67 dB, within the frequency band of interest. By achieving good input, output,

and interstage matching, great PAE is obtained. Figure 8 shows that the proposed PA reaches PAE of 20.6% at 6 GHz.

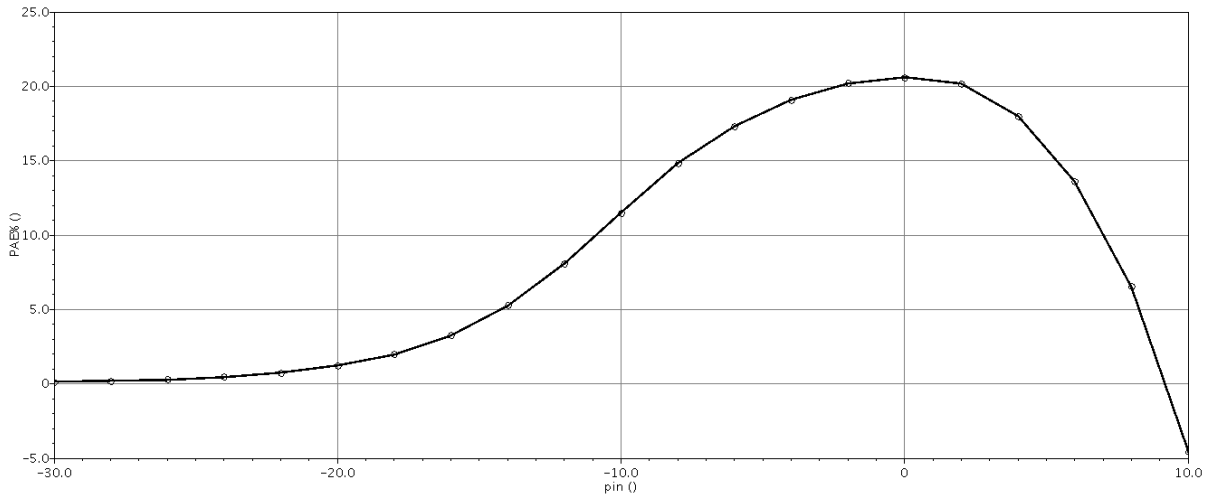

Figure 8. Post-layout PAE% of the proposed CMOS PA.

As listed in Table 2, the proposed CMOS PA attains better gain as compared with the previous work in 130 nm CMOS technology [10], [22], [28]. Also, the proposed PA demonstrates a broad operating frequency band starting from 3.8 GHz and ending at 8.4 GHz. Furthermore, the results show improved PAE as compared to those recently reported [8], [23]. The key idea of the proposed PA is utilizing a two-stage configuration with a cascode current-reused scheme in the first phase connected to a common-source structure in the second phase. This architecture is widely used in literature for obtaining a good gain with higher PAE [10], [12], [20].

Table 2. Comparison of wideband PA performance.

Reference	Process (nm)	Frequency Range (GHz)	Supply Voltage (V)	Gain (dB)	S11 (dB)	S22 (dB)	S12 (dB)	Power (mW)	PAE %	Area (mm^2)
[23] 2015	110	8-12	2.3	9±1.5	<-5	<-7	---	---	20	0.66
[9]* 2016	180	3.1-10.6	0.9	10.6±0.8	<-15.8	<-9	---	14.3	---	0.91
[29] 2016	65	3.4-4.8	4	13.65 ±0.25	<-9.4	<-16.7	<-24	---	24.6	0.51
[20] 2016	130	3.1-5.1	1.8	20.3±0.8	<-1.5	<-6	<-69.3	27.3	---	---
[8] 2017	180	3.1-6	---	10±1	<-6	<-7	<-29	30	15.5	0.67
[12] 2018	180	3-10.6	---	11.5±0.8	<-8.5	<-8	<-50	34	26	0.81
[28] 2018	130	6-9	1.2	8	<-8.5	<-9.5	---	---	23.2	0.85
[22] 2019	130	8-12	2.4	10	<-8	<-7	<-25	20	29	---
[21] 2020	180	2.2-5	1.8	15.6	<-1.3	<-10.3	<-46.5	77.3	39.6	---
[10] 2021	130	7.8-11.5	2	8±1	<-10	<-5	<-25	58	21.3	1.07

This Work 2023	130	3.8-8.4	1.2	12.7±0.5	<-5	<-6.6	<-67	24.8	20.6	0.40

The S12 represents the value of the signal in the opposite path of transmission. The higher level of S12 results in interference between the undesirable reverse signals with the required transmission signal in the forward path. This demonstrates the importance of observing the value of this coefficient. The proposed PA accomplishes the lowest level of the S12 of lower than -67 dB for the obtained frequencies spectrum of 3.8–8.4 GHz as compared to prior work [8], [10], [12], [22], [29].

The proposed PA achieves higher gain and excellent power-added-efficiency in the 3.8–8.4 GHz band while maintaining low power consumption of 24.8 mW as compared with previous work listed in Table 2. Therefore, the proposed PA is appropriate for low-power small distance coverage wireless UWB communication applications.

The layout of the proposed PA is presented in figure 9 with dimension of 750 µm × 540 µm chip area. The proposed PA occupies the lowest area and attains a higher gain with small gain flatness under a wide band of frequencies while accomplishing great PAE, and good input/output matching behaviour.

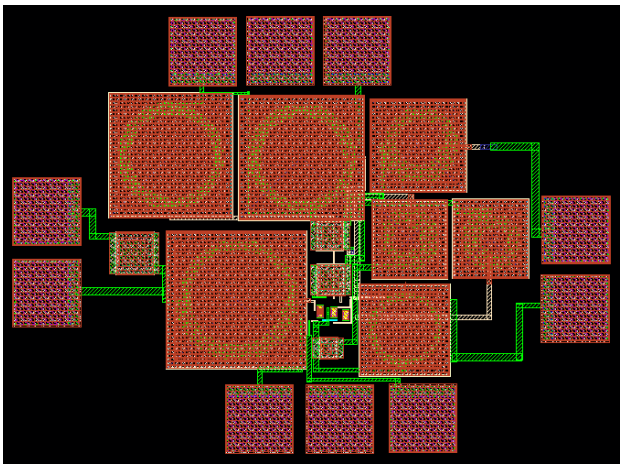

Figure 9. Layout of the proposed CMOS PA.

IV. CONCLUSIONS

The implementation of excellent performance power amplifier (PA) for UWB applications in CMOS technology has a crucial role since it offers portable devices a longer battery lifetime and better performance. The proposed PA has been designed using the current-reused cascode scheme for energy saving. The proposed technique attains a reduction of the power and area by 24.8 mW, and 0.40 mm2, respectively, compared with recent prior architectures and results in a PAE of 20.6%. Besides the power gain and gain flatness, the proposed PA accomplishes 12.7±0.5 dB within band 3.8–8.4 GHz with input and output loss of <-5 dB, and <-6.6 dB, respectively.

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