IMPACT OF TEMPERATURE VARIATIONS ON DESIGN PARAMETERS OF CNTFET

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ABSTRACT

In this paper we analyse the impact of temperature variations on design parameters of CNTFET with particular reference to the output and trans-characteristics, the output resistance, the transconductance and cut-off frequency. The analysis of CNTFET I-V characteristics allows to say that, except for the transition regions, there are very slight differences with temperature variations.

KEYWORDS: *Carbon NanoTubes, CNTFET, Modelling, Temperature Variations, I-V characteristics, Transconductance, Verilog-A.*

I. INTRODUCTION

Carbon NanoTubes, also known with the acronym **CNTs** (**C**arbon **N**ano**T**ubes), have unique electronic and mechanical properties that make them promising candidates for future nanotechnology applications [1-3].
In particular, CNTs, for their extraordinary electronic properties, are used as channel in CNTFETs (Carbon Nanotube Field Effect Transistors), contrary to MOSFETs devices, where the channel is of silicon. In this way it is possible to obtain good operation even at very high frequencies, as we have shown in our previous papers [1-11].
For conventional CNTFET we have already proposed a compact, semi-empirical model [5], in order to carry out static and dynamic analysis of A/D circuits [12-15].
In this paper we analyse the impact of temperature variations on design parameters of CNTFET with particular reference to the output and trans-characteristics, the output resistance, the transconductance and cut-off frequency.
The presentation of the paper is organized as follows. At first we present a brief review of our CNTFET model used in the proposed analysis. Then we show and discuss the simulation results together with conclusions and future developments.

II. A BRIEF REVIEW OF OUR CNTFET MODEL

An exhaustive description of our I-V CNTFET model is in [5-6]. Therefore, we suggest the reader to consult these References.
It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital circuits: in fact, the most complex part of the model is contained in Verilog A [16].

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With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as [5]:

$$I_{DS}=\frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and V_{CNT}, voltage surface, have the expressions reported in [5].
Regards to C-V model, an exhaustive description of our C-V model is widely described in [10] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are explained:

$$\begin{cases} C_{GD}=q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS}=q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (2)$$

In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances. We have achieved this goal using an empirical method exhaustively described in [5]. In this way all elements of the equivalent circuit of Fig. 1 can be determined.

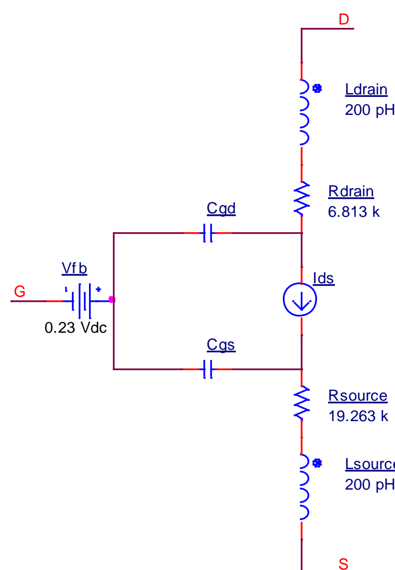

Figure 1. Equivalent circuit of n-type CNTFET.

It is similar to a common MOSFET one [17] and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_{drain} and L_{source} and the resistors R_{drain} and R_{source}, in which the parasitic effect due to the electrodes are also included.

III. TEMPERATURE VARIATIONS ON I-V CHARACTERISTICS

To investigate on the I-V CNTFET characteristics in different temperatures, we consider a single wall n-CNTFETs with a diameter of 1.509 nm and 22 nm long in the ballistic transport hypothesis.
We design a standard simulation circuit where, in static conditions, alternately we were changing V_{GS} and V_{DS} and vice versa.
We performed the analysis at 100 K, 300 K and 500 K as shown in Fig. 2 and Fig.3.

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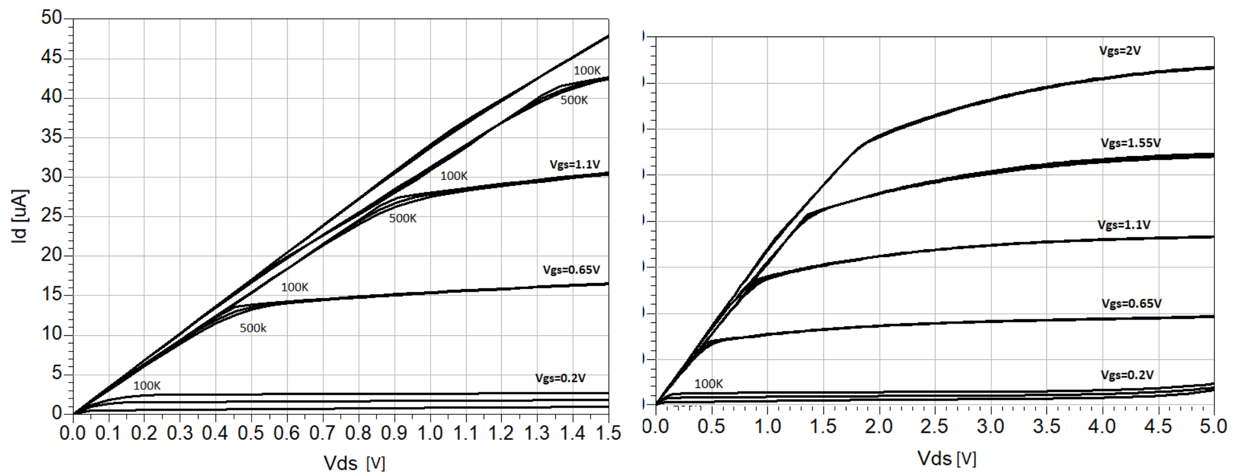

Figure 2. I_{DS} versus V_{DS} and relative zoom.

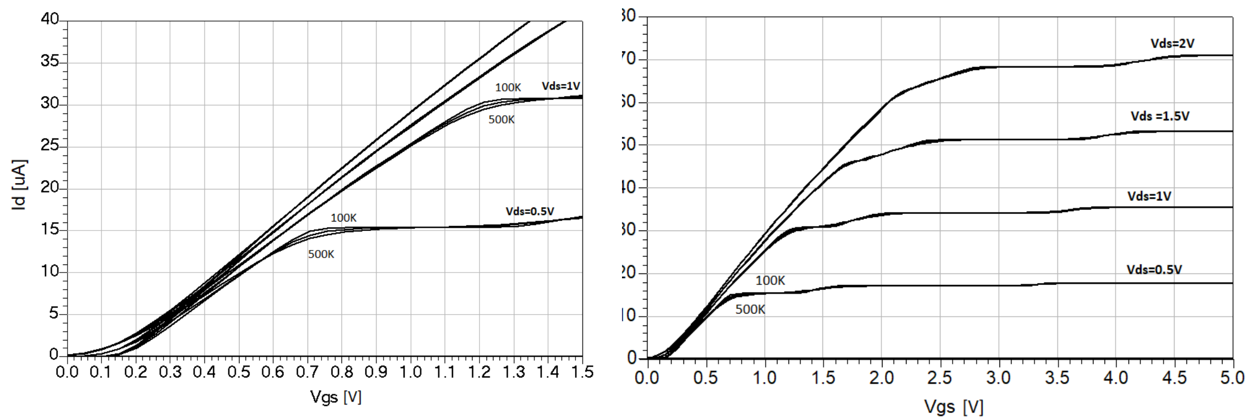

Figure 3. I_{DS} versus V_{GS} and relative zoom.

The plots on the left are zoomed on small voltages in order to underline the temperature change effects.
From the analysis of Figs. 2 and 3, we can say that the increasing temperature at lower quiescent voltages leads to a lower drain current, especially on the knee of the curve. This is a MOSFET technology common feature that guarantees a negative current feedback that prevents the device break at higher temperatures.
It can easily see that those curves suffer a negligible variation in terms of I_{DS} in the extreme conditions of 100 K and 500 K.
Moreover, these changes are often comparable with the CNTFET technological process uncertainties and almost null. The largest variation is in the knee region where we measure an I_{DS} of 13.4 uA at 500 K and I_{DS} of 15.1 uA at 100 K for V_{GS} = 0.7 V and V_{DS} = 0.5 V.

IV. Temperature Variations on Transconductance and Output Resistance

We investigate about the other design parameters of CNTFET, i.e. the transconductance and the output resistance of the device. As you can see hereafter, in these cases we discover larger differences than the previous ones so we decided to extend the analysis to intermediate temperature values (200 K and 400 K).
We adopt a circuit topology able to increase slightly an input voltage and estimate the I_{DS} changes in order to perform differential measurements.
The results of this analysis are reported in the following figures.

In particular in Fig.4 we show the CNTFET transconductance on different working conditions. Comparing these results with the I-V characteristics we can say that in higher voltage ranges (more than 1.5 V) and at higher temperature, I_{DS} increases. This inversion leads to the large variations observed in the previous figures.

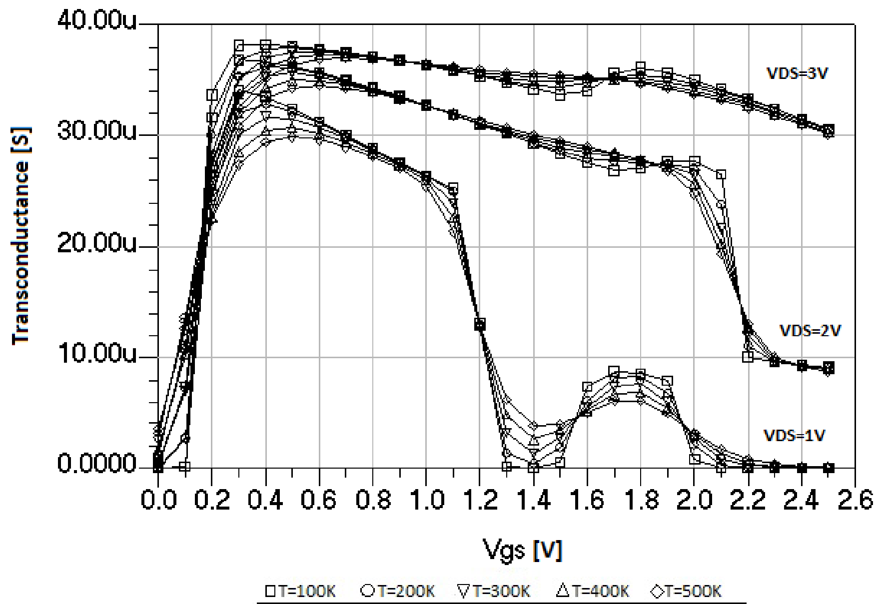

Figure 4. Transconductance on different working conditions

A plot of the output resistance, R_{OUT}, fundamental parameter in the design of integrated active loads or mirrors, is reported in Fig. 5, whose details (zooms) are shown in Figures 6 and 7.

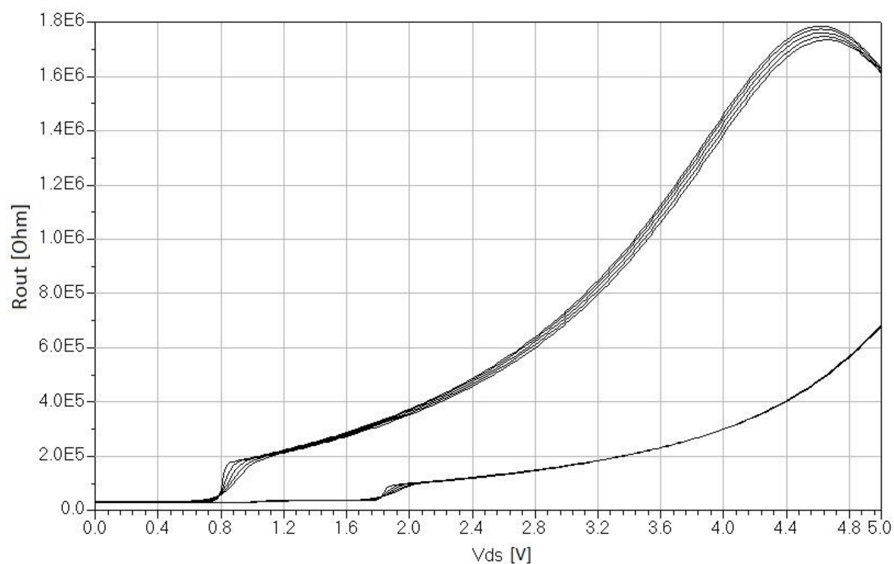

Figure 5. R_{OUT} versus V_{DS}.

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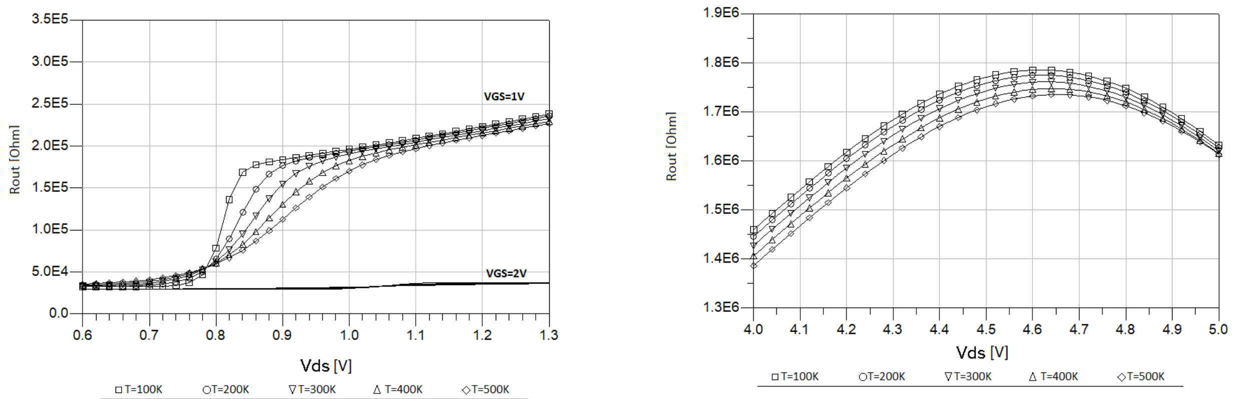

Figure 6. Zoom of R_{OUT} versus V_{DS}.

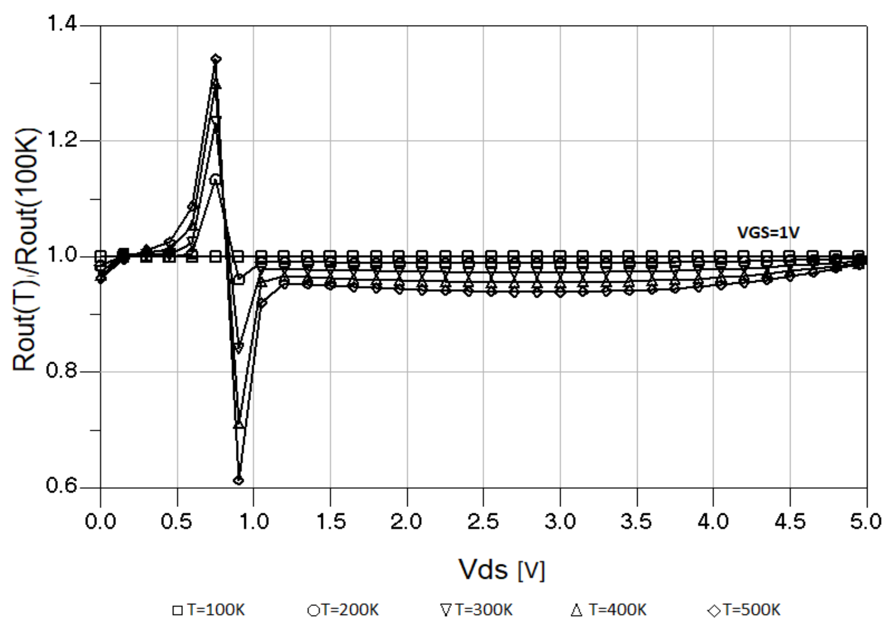

Figure. 7. R_{OUT} divided by the value of R_{OUT} at 100K.

The output impedance trend does not change in different temperature conditions.
It can also easy to recognize the two working regions of the device: the triode region with a very poor output resistance and the saturation region with an impedance next to the MOSFET technology. After the peak at 4.6 V, CNTFET enters in the tunnelling region where I_{DS} increases exponentially and R_{OUT} decreases at the same ratio.
In Fig. 6 we find the largest differences after the temperature changes. At lower temperature there is a faster transition that leads to a maximum output resistance larger than in higher temperatures.
Fig. 8 shows the simulated gain versus frequency for an inverter gate, based on CNTFET, where it is easy to see that the gain is quite independent on temperature.

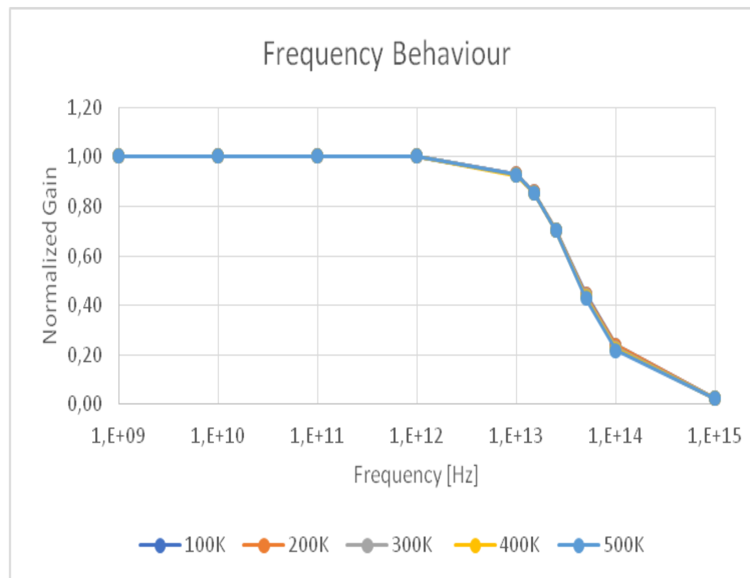

Figure 8. CNTFET frequency perfromance.

It is possible to determine the cut-off frequency as a function of temperature, as illustrated in Fig. 9.

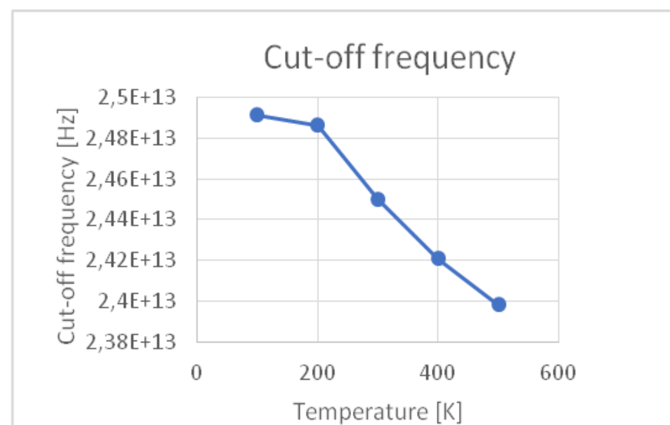

Figure 9. Cut-off frequency versus temperature.

It is clearly shown that the increasing temperature leads to a gain and a cut-off frequency both lower.

V. Conclusion and Future Developments

In this paper we analysed the impact of temperature variations on design parameters of CNTFET with particular reference to the output and trans-characteristics, the output resistance, the transconductance and cut-off frequency, using a compact, semi-empirical model, already proposed by us [5].
To investigate on the I-V CNTFET characteristics in different temperatures, we considered a single wall n-CNTFETs with a diameter of 1.509 nm and 22 nm long in the ballistic transport hypothesis.
From the analysis of CNTFET I-V characteristics, we can affirm that, except for the transition regions, we found very slight differences when temperature changes. Furthermore, the general device behaviour was found to be very MOSFET-like, thus it is possible to adapt the existing circuits to CNTFET ones without difficulties.

Actually we are studying the effect of noise [18] and of temperature in the CNTFET-based design of A/D circuits [19], considering also the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [20].

REFERENCES

[1] R. Marani, A. G. Perri: Il futuro della tecnologia: le nanotecnologie, *LA COMUNICAZIONE: NOTE, RECENSIONI & NOTIZIE,* Istituto Superiore delle Comunicazioni e delle Tecnologie dell'Informazione, Rome, **LVI**, ISSN: 1590-864X, 169 – 178, (2009).

[2] A. G. Perri: *Dispositivi Elettronici Avanzati*, Progedit Editor, Bari, Italy; ISBN: 978-88-6194-081-9, (2018).

[3] A.G. Perri, R. Marani: *CNTFET Electronics: Design Principles*, Progedit Editor, Bari, Italy, ISBN: 978-88-6194-307-0, (2017).

[4] A. G. Perri: *Modelling and Simulations in Electronic and Optoelectronic Engineering*, Research Signpost, Kerata, ISBN: 978-81-308-0450-7, (2011).

[5] G. Gelao, R. Marani, R. Diana, A.G. Perri: A Semi-Empirical SPICE Model for n-type Conventional CNTFETs, *IEEE Transactions on Nanotechnology*, **10**(3), 506-512, (2011).

[6] R. Marani, A.G. Perri: A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software, *Current Nanoscience*, **7**(2), 245-253, (2011).

[7] R. Marani, A.G. Perri: Simulation of CNTFET Digital Circuits: a Verilog-A Implementation, *International Journal of Research and Reviews in Applied Sciences*, **11**(1), 74-81, (2012).

[8] R. Marani, A.G. Perri: Modelling and Implementation of Subthreshold Currents in Schottky Barrier CNTFETs for Digital Applications, *International Journal of Research and Reviews in Applied Sciences*, **11**(3), 377-385, (2012).

[9] R. Marani, G. Gelao, A.G. Perri: Comparison of ABM SPICE library with Verilog-A for Compact CNTFET model implementation, *Current Nanoscience*, **8**(4), 556-565, (2012).

[10] R. Marani, G. Gelao, A.G. Perri: Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design, *Microelectronics Journal*, **44**(1), 33-39, (2013).

[11] R. Marani, A.G. Perri: Analysis of CNTFETs Operating in SubThreshold Region for Low Power Digital Applications, *ECS Journal of Solid State Science and Technology*, 5(2), M1-M4, (2016).

[12] G. Gelao, R. Marani, L. Pizzulli, A.G. Perri: A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Static Analysis, *Current Nanoscience*, **11**(4), 515-526, (2015).

[13] G. Gelao, R. Marani, L. Pizzulli, A.G. Perri: A Model to Improve Analysis of CNTFET Logic Gates in Verilog-A-Part I: Dynamic Analysis, *Current Nanoscience*, **11**(6), p. 770-783, (2015).

[14] R. Marani, A.G. Perri: A Simulation Study of Analogue and Logic Circuits with CNTFETs, *ECS Journal of Solid State Science and Technology*, **5**(6), M38-M43, (2016).

[15] R. Marani, A.G. Perri: A Comparison of CNTFET Models through the Design of a SRAM Cell, *ECS Journal of Solid State Science and Technology*, **5**(10), M118-M1, (2016).

[16] Verilog-AMS language reference manual, Version 2.2, (2014).

[17] P.E. Allen, D.R. Holberg: *CMOS Analog Circuit Design*, Oxford University Press, (2013).

[18] R. Marani, G. Gelao, A.G. Perri: A Compact Noise Model for C-CNTFETs, *ECS Journal of Solid State Science and Technology*, **6**(4), pp. M118–M126, (2017).

[19] R. Marani, and A.G. Perri: A Review on the Study of Temperature Effects in the Design of A/D Circuits based on CNTFET, *Current Nanoscience*, **15**(5), p. 471-480, (2019).

[20] R. Marani, A.G. Perri: Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits, *ECS Journal of Solid State Science and Technology*, **9**(2), (2020).

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