IMPLEMENTATION OF FOUR BIT FULL ADDER CIRCUIT USING HIGH SPEED MULTI THRESHOLD VOLTAGE INTERFACE CIRCUITS

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ABSTRACT
The Multithreshold low power technique proves better for reduction in power consumption without reducing the total speed of the circuit. The voltage interface circuits are essential in order to transfer the signals among circuits operating at different voltage levels. The Traditional Feedback based level converters suffer from high short-circuit power and long propagation delay due to typically slow response of the internal feedback circuitry that controls the operation of the pull-up transistors. This paper proposes level converters which employs multi-Vth CMOS technology that are optimised to have minimum power consumption, maximum voltage level and minimum delay. The level converters proposed in this paper are implemented on the 4-bit full adder circuit. The design and optimization of the level converter circuits are carried out using HSPICE software. Power and delay are reduced by approximately 15% and 30% respectively when the circuits are optimized in 0.18µm TSMC CMOS technology.

KEYWORDS*: Multithreshold Voltage Interface Circuits, high performance circuits, low power, minimum delay, level converters*

I. INTRODUCTION

The CMOS technology is developing rapidly from past decade. This development is due to the enhancements done in the CMOS technology, the technology scaling plays an important role in the enhancement of the CMOS technology [13] [15] [16]. As the increase in the technology more and more transistors are integrated on to a single chip. This increase of transistors causes more power dissipation, power density and delay. Due to this increase in the power and delay the reliability of the circuit reduces and also the package cost increases. This affects more in portable systems where the battery life drastically reduces due to above reasons [15] [16]. By scaling the supply voltage we can reduce the power consumption of the circuit but the speed of the circuit decreases. This delay in the circuit can be reduced by employing multi-V_{DD} in which different delays can be assigned to different signal processing paths within the integrated circuit.

By selectively lowering the supply voltages of gates at non critical paths and maintaining higher supply voltages at critical paths can satisfy the target clock frequency in multi V_{DD} circuit. When the transistors in the pull-up and the pull-down networks are simultaneously turned on the static dc power is consumed when a low voltage swing signal that drives a CMOS gate is connected to a higher supply voltage. The output voltage swing of the receiver degrades, thereby leading to a static dc current in the fan-out gates of the receiver. Specialized voltage interface circuits are required in order to transfer signals among these circuits operating at different voltage levels. Level converters impose

additional power consumption and propagation delay overhead in a multi- V_{DD} system [1][5][6][7][8][13]. In a multi V_{DD} system to choose the supply voltages we have to consider many factors such as path propagation delay, power and delay overhead of the level converters and the efficiency of the power supplies. The speed, power and area are important tradeoffs in the design of voltage level conversion circuits so this paper considers wide range of supply voltages to address all the tradeoffs [1][2][3][4][9]. In order to avoid the static dc current in the level converters, the conventional level converters depends on the feedback circuit for controlling the operation of the pull up transistors. Even though these feedback circuits because of slow response suffers from short circuit current and reduced speed.

To achieve desired functionality with low voltage transmitter, increase in the transistors width is required which increases the overall power consumption and the delay in the feedback circuits. This paper considers level converters based on multithreshold CMOS technology unlike conventional technique which is based on feedback, in the proposed level converters all the transistors are optimised by reducing the W/L ratios of the transistors in which the delay is reduced and the voltage swing is increased. The proposed level converters are implemented on four bit adder circuits and obtained the desired results.

The rest of the paper is organised as follows: section 2 deals with the operation of the level converters, section 3 deals with implementation of the proposed level converters on four bit adder circuit and the simulation results, section 4 deals with results and discussion, section 5 concludes the paper and section 6 lists future work.

II. LEVEL CONVERTERS

In this paper we considered two types of level converters, one depends on the feedback circuit and the other logic depends on variable threshold CMOS technology. The feedback based level converters are described in section 2.1 and the level converters that are based on the multi threshold are described in section 2.2.

2.1. Level Converters Based on Feedback circuit.

These are conventional level converters in which the level conversion is based on feedback circuit. A receiver that is driven by low voltage swing produces static dc current when pull up network of the receiver is not fully turned on, this partial on of the pull up network is caused when a low swing signal is connected to a high supply voltage [5][6][7]. To suppress this static dc current specialized voltage interface circuits are used between the low voltage driver and full voltage swing receiver.

In the standard feedback converters this static dc current is not produced as the pull up networks are not driven by the low voltage swing signal that is provided by the driver and the operation of the pull up transistors depends on the internal feedback circuit. Even though the standard level converters doesn't produce static current they suffers from high short-circuit power and long propagation delay due to the typically slow response of the internal feedback circuitry that controls the operation of the pull-up transistors [2][3][4][8].

Unlike the pull-up network transistors the pull-down network transistors in these circuits are driven by low voltage swing signals. At very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to balance the strength of the pull-up and the pull-down networks [4][9]. Because of this the speed and the power efficiency of the conventional level converters are decreased drastically at low input voltages. The standard level converter is shown in the figure 1. Here the transistors M_1 and M_2 experience a low gate overdrive voltage (V_{DDL}-V_{th}) during the operation of the circuit [4][9]. To produce more current than the transistors M_3 and M_4 the transistors M_1 and M_2 need to be sized larger. The operation of the circuit is describes as follows M_2 is turned off when the input is at 0V.. M_1 is turned on when $Node_1$ is charged to V_{DDL}. Transistor M4 is on when $Node_3$ is discharged to 0 V. Transistor M3 is turned off when Node2 is charged to V_{DDH}. The output is pulled down to 0 V. When the input transitions to V_{DDL}, M_2 is turned on. $Node_1$ is discharged, turning M_1 off. $Node_2$ is discharged, turning M_3 on.$Node_3$ is charged up to V_{DDH} turning M_4 off. The output transitions to V_{DDH}. A feedback loop, isolated from the input, controls the operation of M_3 and M_4 during both transitions of the output [2][3][4][9].

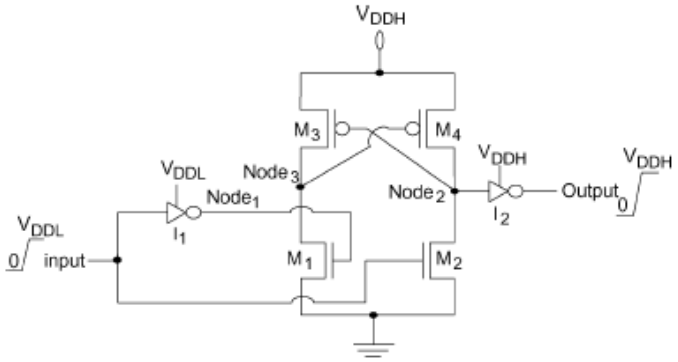

Figure 1: Standard level converter (lc1).VDDL is the lower and VDDH is the higher supply voltages.

This circuit consumes short circuit and dynamic switching power. In order compensate for the gate overdrive degradation for lower values of V_{DDL}, the sizes of M_1 and M_2 need to be further increased. Therefore increases the load of driver circuit which degrades the speed and increase the power consumption [2][3][4]. To drive the transistors M_1 and M_2 at low voltages tapered buffers are required. These tapered buffers further increase the power consumption of circuit shown in figure 1. Another level converter is shown in figure 2 in which the speed is enhanced when compared to level converter in figure 1.

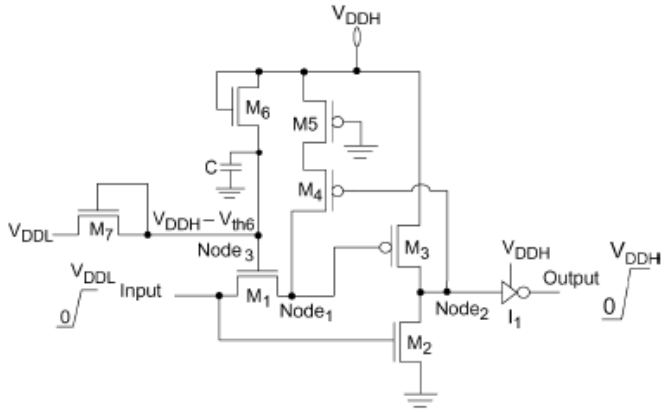

Figure 2: Level converter (lc2)

The voltage of the $Node_3$ is maintained between V_{DDL} and $V_{DDL}+V_{th}$ by transistor M_6 in order to enhance the speed of the transistor M_1. Here also tapered circuits are used to drive the circuit. The use of the tapered circuits further increases the power consumption of the level converter than the level converter shown in figure 1.

2.2. Level Converters Based on Multi-Threshold Voltage

These level converters are based in the Multi-threshold voltage CMOS technology instead of the feedback circuit. The advantage is that the static dc current can be eliminated [4] [14]. The pull up network will have high threshold voltage and will be driven by low swing signals without producing the static dc current. A multi-threshold voltage level converter is shown in the figure 3.

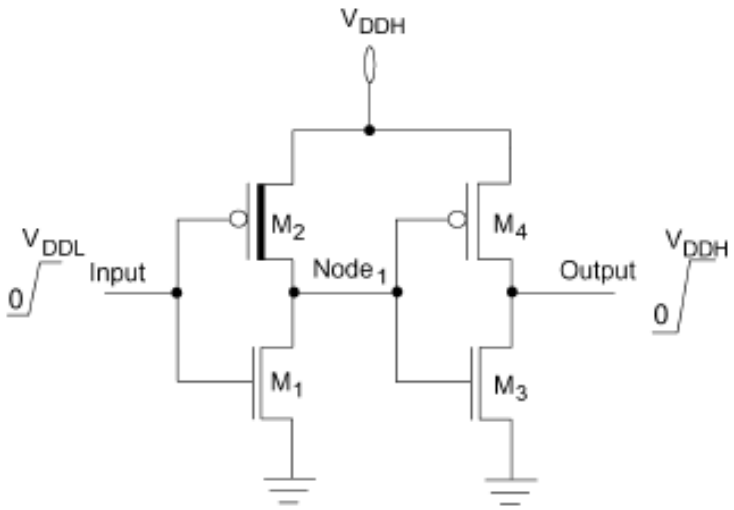

Figure 3: Level Converter with multi V_{th} (lc3). The thick line indicates a high-V_{th} device**.**

This level converter is composed of two cascaded inverters with dual-V_{th} transistors. In order to avoid the static dc current in the first inverter when the input is at V_{DDL} the threshold voltage of M_2 is increased [4]. The value of the threshold voltage of M_2 is required to be greater than V_{DDH}-V_{DDL} in order to eliminate the static dc current. The operation of the level converter shown in figure 3 is described as follows.

Transistor M_2 is turned on when the input is 0V. When Node1 is pulled up to V_{DDH} the transistor M_1 is in cut off. When the input transitions to V_{DDL} the output is discharged to 0 V and transistor M_1 is turned on. Since $V_{GS, M2}>V_{th, M2}$ transistor M_2 is turned off. Node1 is discharged to 0 V and the output is charged to V_{DDH}. This level converter has fewer transistors when compared with level converters with feedback circuit.

The short-circuit power is also reduced as this level converter doesn't have feedback compared to level converters with feedback. To achieve functionality at lower input voltages, we considered multi-V_{th} CMOS technology, with this size of the circuit is not increased compared with level converters with feedback therefore at very low values of V_{DDL}, variable threshold voltage level converter consumes lower power, occupies significantly smaller area, and smaller load capacitance on the input driver as compared to feedback based level converters. Another level converter is shown in figure 4 in which the speed is enhanced when compared to level converter in figure 3 while avoiding the occurrence of static dc current problem.

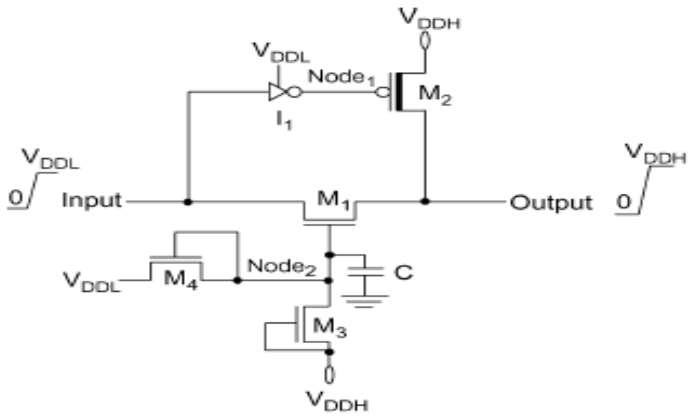

Figure 4: level converter (lc4). Thick line in the channel area indicates a high-V_{th} device

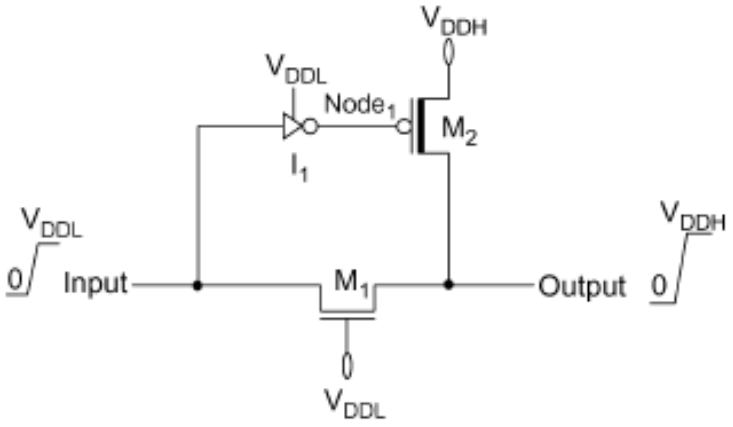

Figure 5: level converter (lc5).Thick line in the channel area indicates a high-V_{th} device

The capacitor used in the level converter shown in figure 4 stabilizes the voltage at $Node_2$ [4][10]. We also enhanced speed due to the shorter input-to-output signal propagation path and the elimination of the contention current during the output low-to-high transition.

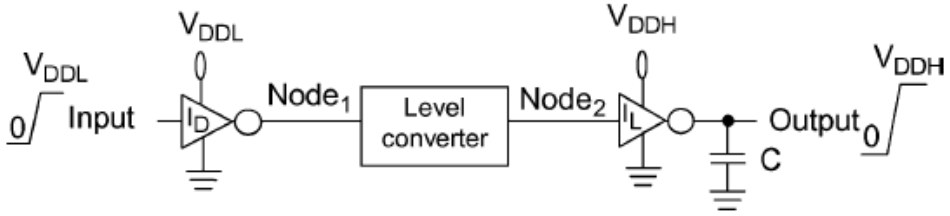

Figure 6: Simulation Setup for characterizing level converters

The simulation set up is shown in figure 6. There V_{DDL} refers to lower supply voltage and V_{DDH} refers to higher supply voltage. ID refers to input driver inverter and IL refers to the output Load driver inverter. The load capacitance is chosen in the order of pF for proper optimization and characterization.

III. IMPLEMENTATION OF MULTI-THRESHOLD LEVEL CONVERTERS FOR FOUR BIT ADDER CIRCUIT

In this section we discussed the implementation of the optimized level converters on four bit adder circuit. The adder circuit which is used in this paper was shown in the figure 7 below. It consists of four one bit adder circuits. Carry is propagated from one adder circuit to another adder circuit and the sum is obtained as $S_0S_1S_2S_3$ at the end of each adder circuit [11][12][13].

The level converters are added to the adder circuit at the end of the each adder. The adder circuit with level converters is shown in the figure 8 below. The level converters and adders at the end of the chain have more switching activity than the ones at the start of the chain. This is because the carry bit from the previous stage keeps rippling through the next stages. So, stage 4 will have more ripple than stage 3, which in turn will have more ripple than the previous stages. Thus it is good to have smaller sized transistors at the end of the chain to minimize energy consumption.

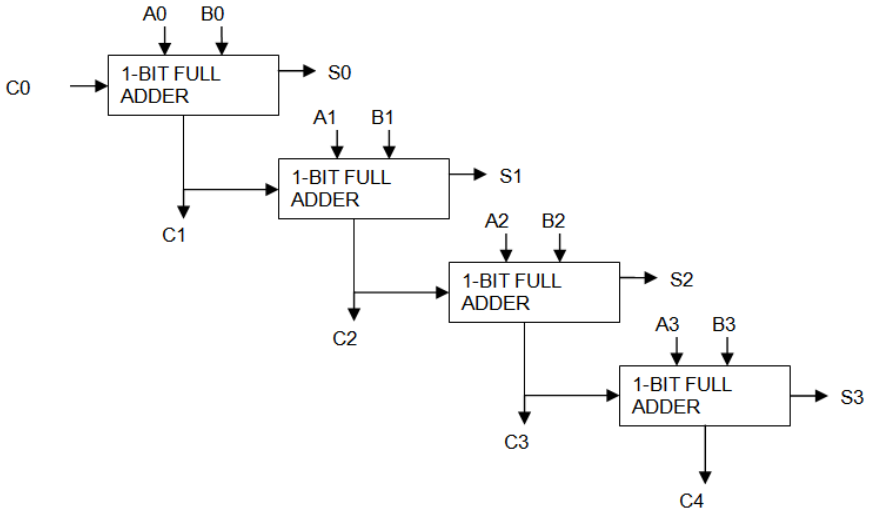

FIGURE 7: Adder Circuit without Level Converters

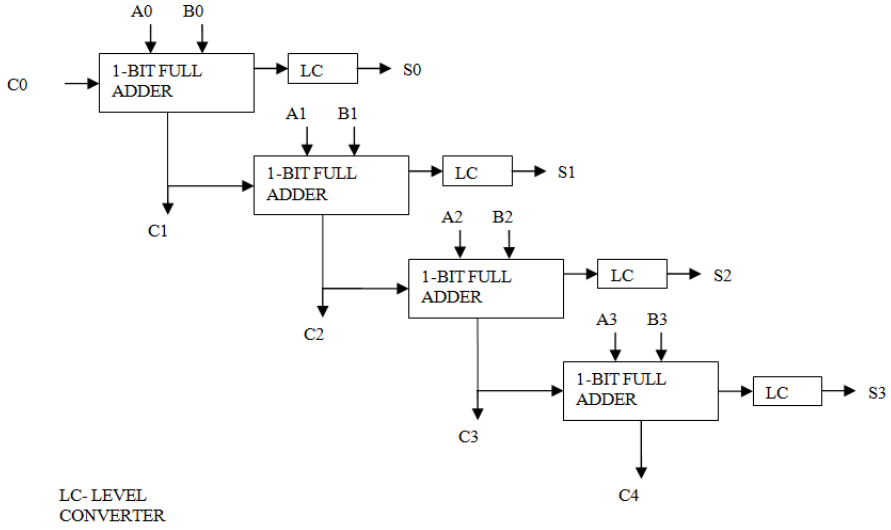

FIGURE 8: Adder Circuit with Level Converters

IV. RESULTS AND DISCUSSION

The performance of the adder circuit was evaluated with and without the level converters and was found to have minimum delay when level converters are added to the adder circuits compared to the adder circuits without level converters. The obtained Power dissipation was found to be in mW and for delay in pSec. Table 1 and Table 2 show the Comparison of Adders with and without Level Converters for Power Dissipation and Delay. Figure 9 and figure 10 show the simulated waveforms for Adders without and with level converters for V_{DDL}=0.5V. The significant changes in output potential are due to un-optimized capacitance used for load.

FIGURE 9: Plot for Simulation Output of Adders Without Level Converters

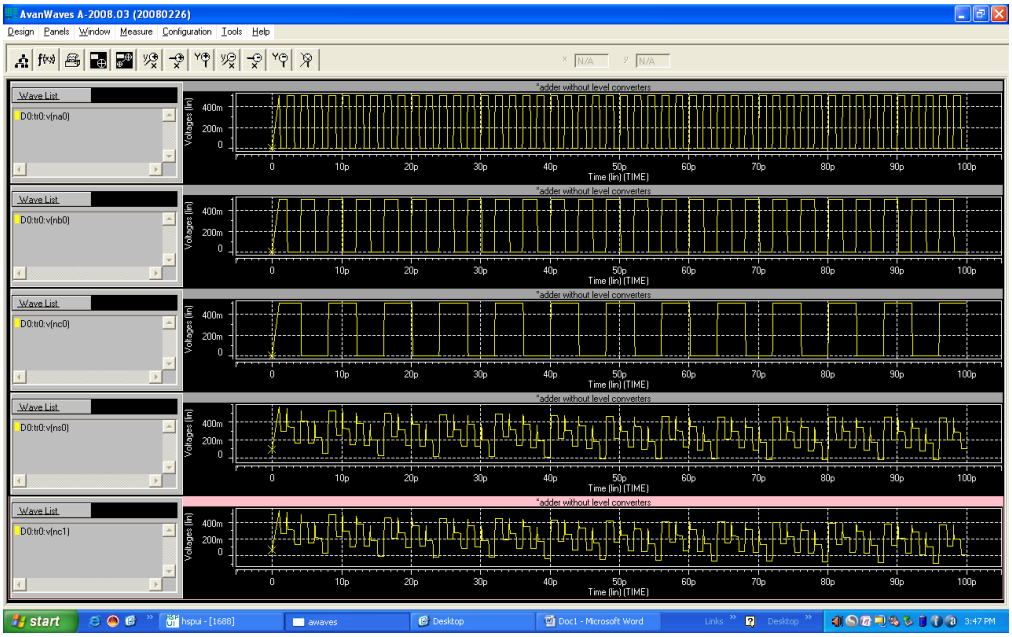

FIGURE 10: Plot for Simulation Output of Adders With Level Converters

Table 1: Comparison of Power dissipation for Adders with and without Level Converters

Circuit Design	POWER DISSIPATION	
	0.5V	1.2V
Adder without level converters	2.7613E-02	1.3852E-06
Adder with lc1	1.2469E-02	1.0210E-06
Adder with lc2	1.8805E-02	1.0077E-06
Adder with lc3	1.3852E-02	1.0023E-06
Adder with lc4	1.9799E-02	1.0020E-06
Adder with lc5	1.2338E-02	1.0037E-06

Table 2: Comparison of Delay for Adders with and without Level Converters

Circuit Design	DELAY	
	0.5V	1.2V
Adder without level converters	2.1E-12	1.00E-10
Adder with level converters	1.0E-12	1.00E-12

Figure 11 and figure 13 show the plots for Comparison of Power Dissipation for Adders with and Without Level Converters for V_{DDL}=0.5V and 1.2V respectively. Figure 12 and figure 14 show the plots for Comparison of Delay for Adders with and Without Level Converters for V_{DDL}=0.5V and 1.2V respectively.

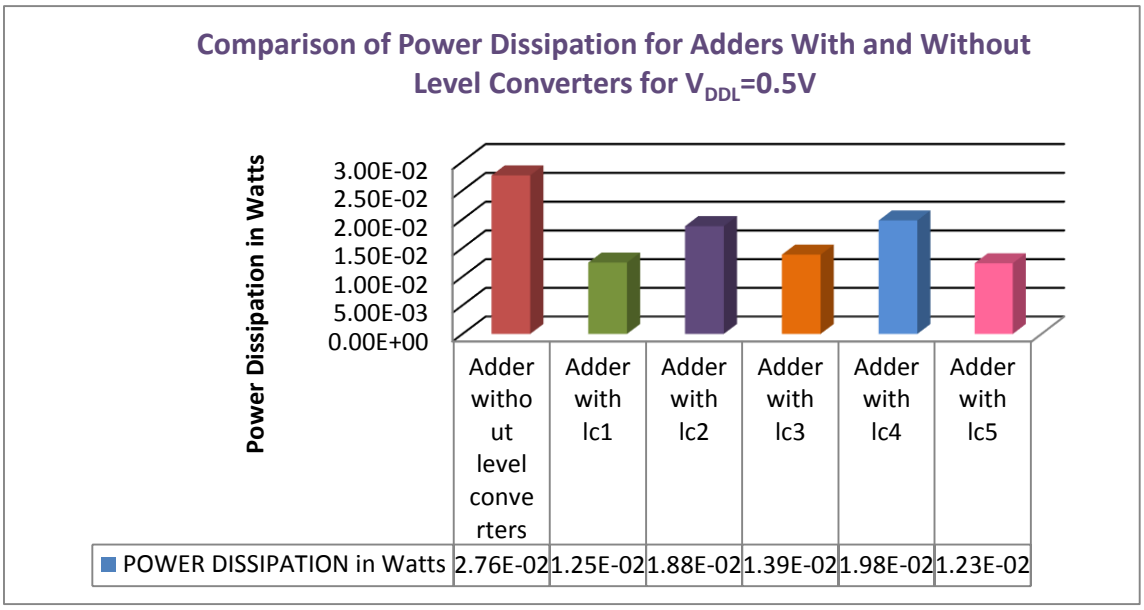

FIGURE 11: Plot for Comparison of Power Dissipation of Adders with and Without Level Converters for V_{DDL}=0.5V

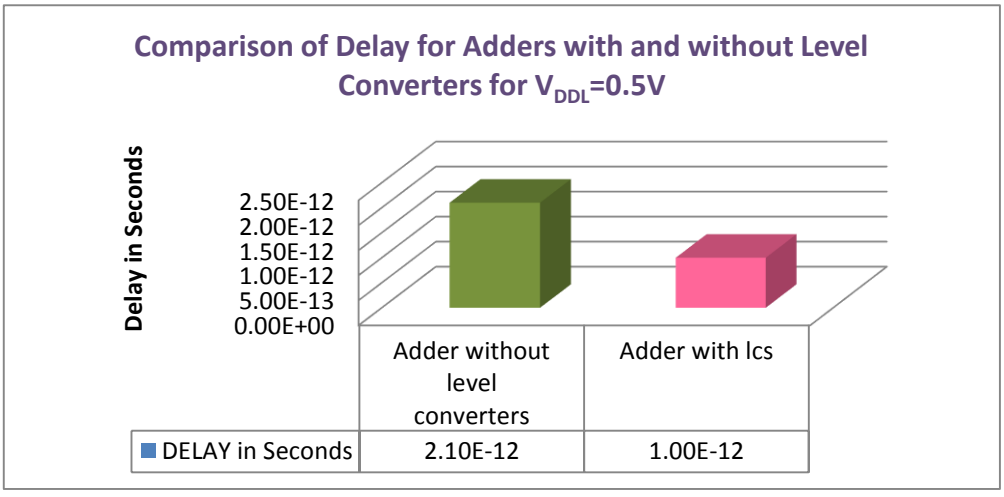

FIGURE 12: Plot for Comparison of Delay of Adders with and Without Level Converters for V_{DDL}=0.5V

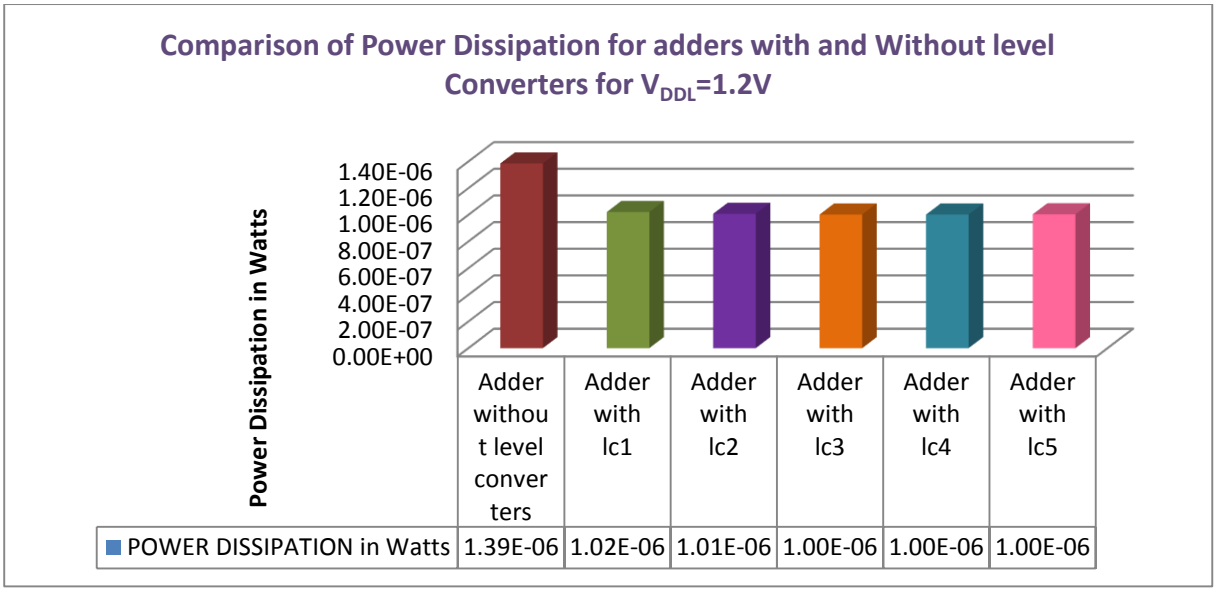

FIGURE 13: Plot for Comparison of Power Dissipation of Adders with and Without Level Converters for V_{DDL}=1.2V

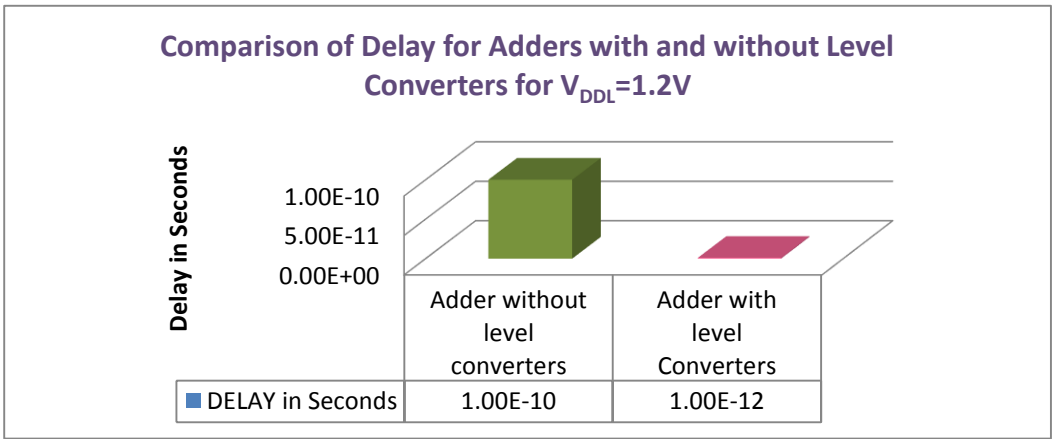

FIGURE 14: Plot for Comparison of Delay of Adders with and Without Level Converters for V_{DDL}=1.2V

From above results, it is clear that the power dissipation of adders with level converters is minimum when compared to adders without level converters, also it is less for VDDL =1.2V than 0.5V. Hence as the supply voltage decreases the power dissipation also increases. The Delay is almost same for different V_{DDL} but it decreases for adders with level converters than without them.

V. CONCLUSION

In this paper we discussed about the level converters based on feedback circuit and based on a Multi-V_{th} CMOS technology. The optimization of level converters for different values of the lower supply voltages is done for power dissipation and delay for W/L Ratio of the Multi-threshold transistors. When the circuits are individually optimized in 0.18µm TSMC CMOS technology, the adders with Multi-Threshold Level converters show significant decrease in power dissipation by 15% and delay by 50% when compared to the Adders without level converters.

VI. FUTURE SCOPE

Further these level converters can be optimized for different values of Load Capacitors for proper output voltage swing at different technologies. Also the level converters can be designed with the combination of body biasing techniques for variable threshold values [12] and Multi- V_{DD} supply voltages.

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