

EMBEDDED PASSIVES BASED WIDE BAND RADAR ABSORBER

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ABSTRACT

Wide band circuit analog Radar Absorbing Material (RAM) based on innovative embedded passives (EP) resistors is presented in this paper. The design comprises of Circuit Analog (CA) RAM for wide band operation from 2 to 9 GHz, for linear polarization. The mandatory resistors required for realization of resistive FSS are realized using the novel concept of embedded or integral passives and a large number of resistors are realized with no soldering at all, thus totally dispensing with soldering related defects and eliminating parasitic effects. Design is verified by simulation using the 3D electromagnetic simulation software, HFSS v15. The crucial FSS layer is realized as electrically thin PCB and the CA-RAM is developed as panel of size (280 x 280) mm. The weight of panel RAM is 157 gm. Monostatic Radar Cross Section (RCS) experiments are carried out on RAM to verify the design and simulation. The predicted and measured values agree closely.

KEYWORDS: Circuit Analog RAM, FSS, RAM, RAS, RCS

I. INTRODUCTION

Radar absorbing materials (RAM) find exhaustive applications in aircraft/unmanned air vehicle (UAV) stealth. RAM design and engineering assumes importance as RAM needs to be designed as load bearing structures with primary Electro Magnetic (EM) absorption characteristics. Hence, from the initial design stage, the RAM needs to be developed as radar absorbing structure (RAS) and is an interdisciplinary activity including experts from electromagnetics, structures, aerodynamics and materials.

The main challenge in RAM/RAS design is to realize ever increasing absorption bandwidths with thickness constraints which are conflicting requirements. Absorption bandwidth is quantified in terms of Radar Cross Section Reduction (RCSR) and dielectric RAM design has evolved from the conventional Salisbury screen [1], which comprises of an infinitesimally thin resistive layer with design specified surface resistivity in Ohms/square, also known as space cloth on a grounded dielectric spacer of quarter wavelength thickness. It is noted that the RCSR quantified in terms of dBsm or dB synonymous with radar reflectivity and expressed in terms of S-parameter as S_{II} . The Salisbury screen is a resonant absorber and hence is limited in RCSR bandwidth. For lower microwave frequency operation such as L,S and C bands, the Salisbury screen thickness becomes prohibitively large, which limits its application. It is to be noted that application of RAM is very crucial in these bands as the primary design method of RCSR namely, the ‘shape design’ is a high frequency technique and is not effective in these frequency bands. Hence, RCSR at these frequencies needs to be realized by RAM/RAS application alone. Octave RCSR bandwidths can be realized in multi layer Salisbury screen design known as Jaumann absorbers [2,3]. Jaumann RAMs comprise of

multiple spacecloth layers, designed for different sheet resistivities specified in terms of Ohms/square and optimized for best performance, each backed by quarter wavelength thick dielectric spacer and finally backed by the conducting ground plane whose RCS needs to be reduced. Although simple in construction, the real challenge in either Salisbury screen or the Jaumann absorber is the accurate design and realization of spacecloth(s). We have successfully addressed the design shortcoming in spacecloth in our earlier paper [4] by proposing chip resistor square grid network on electrically very thin (*thickness=5 mils*) dielectric substrates for design of spacecloths. In order to overcome the thickness limitation and derive extended bandwidths, the circuit analog RAM designs have been reported in literature wherein the purely resistive layer of Salisbury screen or the Jaumann absorber is replaced by an impedance layer – the Circuit Analog (CA) layer, whose characteristics can be analysed in terms of an equivalent inductance and capacitance in addition to resistance. Ultra wide bandwidths realized from circuit analog RAM (referred to as CA-RAM in this paper), CA-RAM designs are reported in literature [5]. The CA-RAM essentially comprises of a *resistive* Frequency Selective Surface (FSS) layer above a grounded dielectric slab. CA-RAM designs have been explored and consistently pursued in literature in the search for the most optimal design yielding best RCSR with thickness and weight constraints.

But, the real crux of design of CA-RAM lies in the realization of **resistive** FSS. Pure FSS does not absorb microwave energy and find exhaustive applications as microwave spatial filters. Most important military application of FSS is in the reduction of *out-of-band* RCSR of stealth antennas [3]. Resistive FSS has been earlier realized by using lumped discrete resistors [6, 7]. The use of lumped discrete resistors in the form of SMDs such as chip resistors has severe limitations such as the soldering related defects resulting from soldering of thousands of resistors even in a small panel RAM of size (30 x 30) cm. The reliability is of prime concern and the exorbitant cost of microwave resistors is another stumbling block in the adoption of this technology for airborne applications. Also, the inherent parasitic effects prevent accurate electromagnetic modelling and analysis. But, *resistors are crucial for realization of resistive FSS*. We have earlier addressed these issues successfully in our earlier paper [8] by using the novel concept of ***embedded passives (EP) resistors***, wherein thousands of mandatory resistors are realized integral to the substrate without any soldering at all.

In this paper, we present the design and development of a wide band panel CA-RAM using the twin concepts of double resonance and EP resistors using the Double Dipole (DD) FSS geometry. In the first section, the EM design, modelling and simulation of RAM for realizing wide RCSR bandwidth of 10 dB (minimum) from 2 GHz. to 9 GHz is described. Using HFSS simulation software, the design is optimised for realizing the desired performance. Extensive parametric studies carried out to quantify the effect of various design parameters are described. In section 2, the PCB design and fabrication of the resistive FSS layer is described giving full design details of CA-RAM which is assembled as panel RAM of size 280 x 280 mm. and is a *very thin* counterpart of Salisbury screen. In section 3, monostatic Radar Cross Section (RCS) measurements carried out on the panel RAM is described. The simulation and measurement results are compared and discussed in section 4. This is followed by conclusion and scope for future work.

II. EM DESIGN, MODELLING AND SIMULATION OF RAM

A double dipole (DD) resistive FSS based CA-RAM is designed for meeting the specifications of RCSR of 10 dBsm from 2 to 9 GHz. The schematic of the proposed DD-CA-RAM is shown in figure 1. Each unit cell of this RAM comprises of two dipoles of unequal lengths which are optimised for resonance at two frequencies to cover the required band. *The novelty of this design lies in the use of EP resistors for loading the two dipoles at the centre, for realizing the crucial resistive FSS.* This is an innovative departure from the RAM design given in [9], and the mandatory resistors are in the form of EP resistors, without any soldering at all. In figure 1, the filled black rectangles shown at the centre of each dipole is the EP resistor.

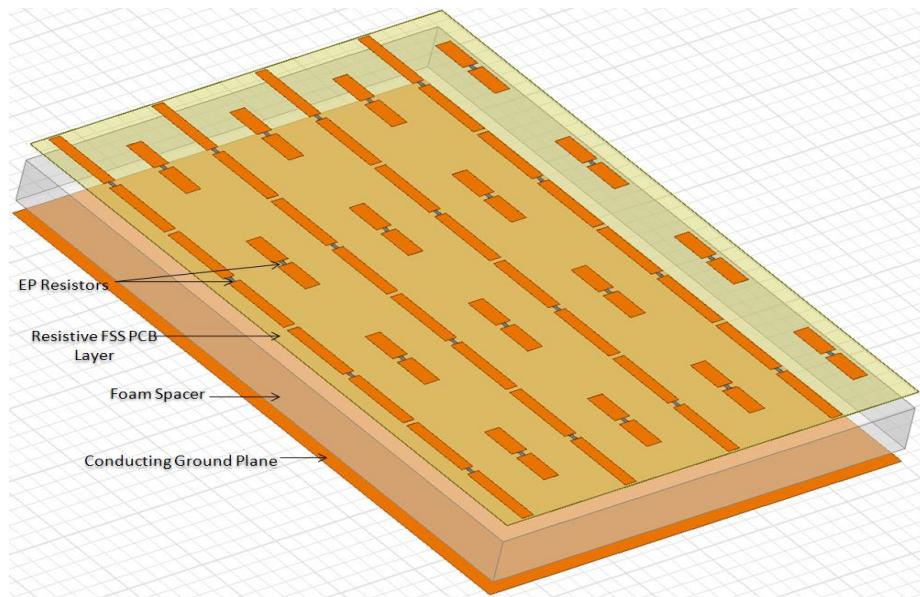


Figure 1. Schematic of double dipole EP resistors based CA-RAM.

The transmission line equivalent circuit of the DD based CA-RAM is shown in figure 2. It is noted that for thickness $<\lambda/4$, the conducting plane backed dielectric spacer behaves as inductance.

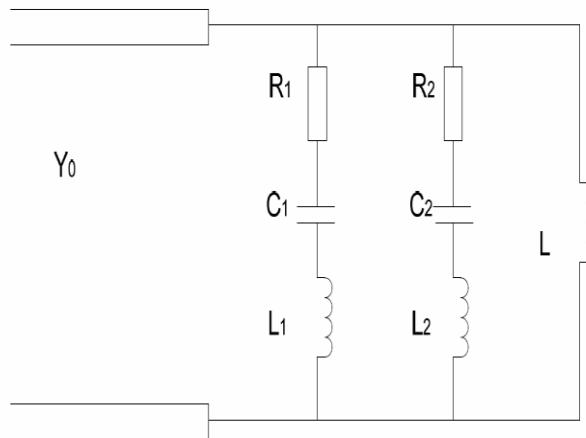


Figure 2. Transmission line equivalent circuit of DD based CA-RAM.

Figure 2 shows the equivalent circuit model comprising of a shunt connection of two resonators consisting of RLC in series. The two resonators have different resonant frequencies and are implemented in the form of dipoles of different lengths etched on a dielectric copper clad laminate. The first resonator comprises of R_1 , L_1 and C_1 in series, while the second resonator consists of R_2 , L_2 and C_2 in series.

The effective admittance at the input of the equivalent circuit is given by:

$$Y_{in} = \frac{1}{j\omega L_p} + \frac{1}{R_1 + j\omega L_1 + \frac{1}{j\omega C_1}} + \frac{1}{R_2 + j\omega L_2 + \frac{1}{j\omega C_2}} \quad \dots \dots \quad (1)$$

and the input reflection coefficient Γ is then

$$\Gamma = \frac{Y_o - Y_{in}}{Y_o + Y_{in}} \quad \dots \dots \quad (2)$$

Hence, from above equations, it is observed that there are two resonant frequencies corresponding to the two dipole FSS geometries, which can be used to design the RAM for realizing the desired wide band RCSR of 10 dB from 2 to 9 GHz.

For a dielectric RAM, which is broadband and non-magnetic, minimum thickness constraint is given by Rozanov [10] as

$$\lambda_{\max} \Gamma_0 \leq 172 d \dots \dots (3)$$

where,

λ_{\max} is the wavelength at the lowest frequency, Γ_0 is the reflection coefficient in dB and d is the total thickness of RAM. Hence, for desired RCSR and thickness, the lowest absorption frequency is constrained to a theoretical limit. Accordingly, the least thickness of a -10 dB wide-band dielectric RAM such as proposed in this paper cannot be less than (1/17) of the largest operating wavelength which is calculated to be 8.8 mm. The total thickness of RAM proposed in this paper is 12.9 mm and hence does not violate the fundamental design rules given in [10].

Using the Floquet's theorem for planar periodic surfaces such as FSS, a unit cell geometry model of DD based CA-RAM is simulated in the 3D EM simulation software, HFSS v15. The unit cell geometry model of CA-RAM in HFSS is shown in figure 3. The geometry model in HFSS comprises of the two dipole geometry based FSS loaded at the centre by EP resistors, which are modelled as pure resistances on FR4 substrate of thickness 0.2 mm. The linked master and slave boundaries are used for the four sides of the unit cell and the DD based CA-RAM is excited using the Floquet's port. De-embedding of the port is also shown. The conducting back plane is modelled as Perfect Electric Conductor (PEC). The dielectric spacer used is Rohacel foam, with $\epsilon_r = 1.03$ and $\tan\delta = 0.0003$ and thickness = 12.5 mm.

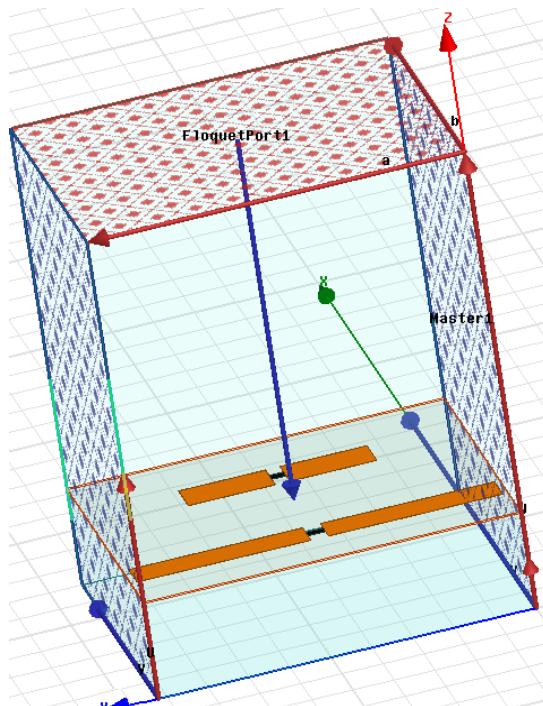


Figure 3. Unit cell DD based CA-RAM geometry model in HFSS.

The optimised simulation performance of DD based CA-RAM is shown in figure 4 for desired minimum RCSR of 10 dB from 2 to 9 GHz. for linear polarization.

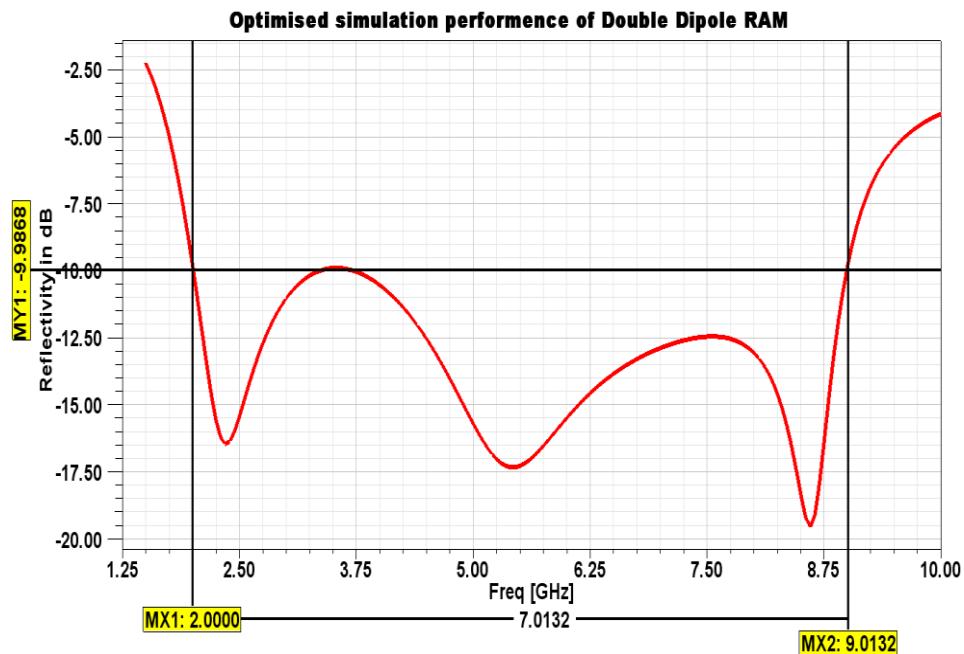


Figure 4. Optimised simulation performance of DD based CA-RAM in HFSS.

Next, parametric simulation studies are carried out in HFSS to assess the sensitivity of design to various design parameters. Figure 5 shows the simulation performance of DD based CA-RAM with varying dipole lengths of the longer dipole only. All other design parameters are kept constant. With the increase in dipole length, the RCSR bandwidth shifts to the left as expected. The optimized length of the longer dipole is 21.2 mm to meet the desired RCSR bandwidth requirements.

Length optimisation of Double Dipole RAM

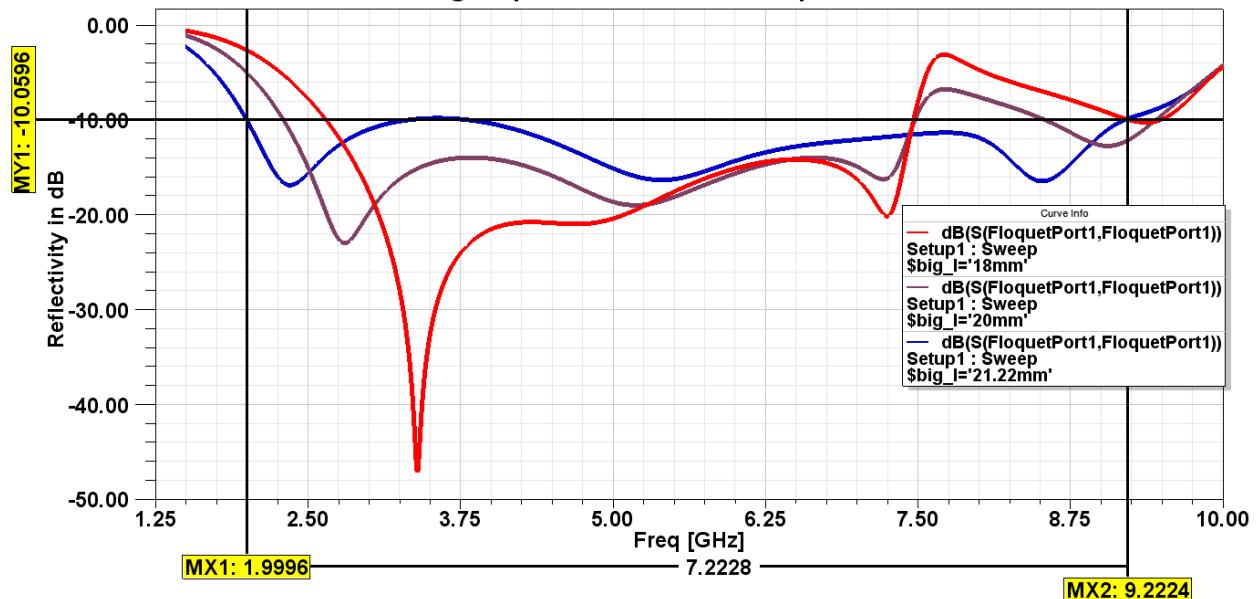
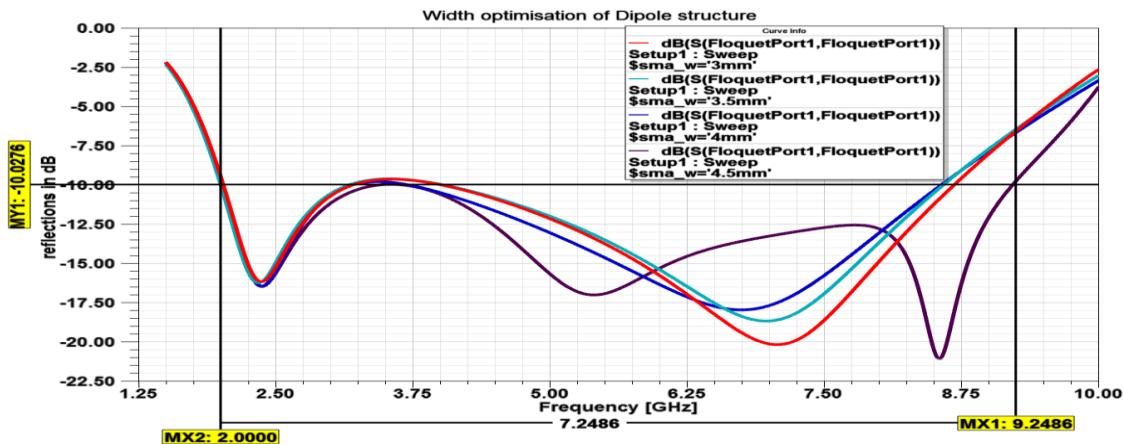
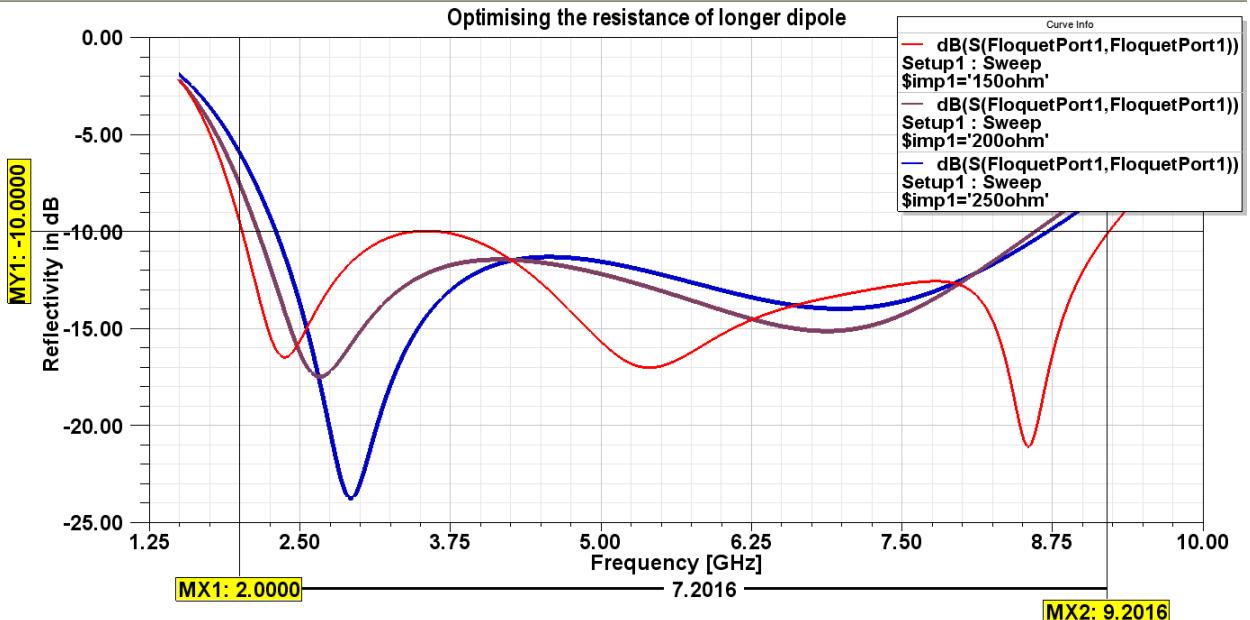


Figure 5. Parametric simulation study for various lengths of longer dipole.

Next, keeping all other design parameters fixed, optimization studies are carried out to study the effect of variation of width of the longer dipole on the RCSR performance. From figure 6, with the change in width from 3 mm to 4.5 mm, it is observed that the RCSR at 2 GHz. remains unaffected whereas the RCSR bandwidth shrinks at the higher frequency end from 9.2 GHz to 8.5 GHz. Hence, the optimised width of the longer dipole is taken to be 4.5 mm. Similar performance is observed for the change in the width of the short dipole and is incorporated in the design.

**Figure 6.** Parametric simulation studies for varying widths of longer dipole.

The EP resistor, R_1 at the centre of the longer dipole is varied to study the performance and is shown in figure 7. It is observed that 150 Ohms EP resistor gives the desired RCSR performance. Resistances of 200 and 250 Ohms result in compression of RCSR bandwidth on both the lower and higher frequency band edges. Similar effects are observed for variation of the EP resistor value of the shorter dipole and the optimized value of the EP resistor R_2 is 200 Ohms.

**Figure 7.** Parametric simulation study varying the EP resistance of the longer dipole.

The optimized design of the unit cell of DD based CA-RAM is given in figure 8a, where l_1 is the half length of long dipole = 21.2 mm ($l_1 = \lambda/2$, at first design centre frequency taken as 3.2 GHz.), l_2 = half-length of short dipole = 10.6 mm ($l_2 = \lambda/2$, at second resonant frequency = 7.5 GHz.). The unit cell of two dipoles is repeated in a rectangular lattice with horizontal spacing of the unit cell, $M = 35$ mm and vertical spacing, $N = 45$ mm. FR4 substrate of thickness = 0.2 mm with $\tan \delta = 0.002$ is used for simulation and fabrication of the EP resistors based PCB. Width of the longer dipole, $w_1 = 3.8$ mm and width w_2 of the shorter dipole is = 4.5 mm. The spacing between the dipoles is 17.5 mm. The dielectric profile of CA-RAM is shown in figure 8b. The thickness of the dielectric spacer is 12.5 mm. *As mentioned earlier, the innovative use of EP resistors for loading the dipoles to realize resistive FSS forms the novelty of this paper.*

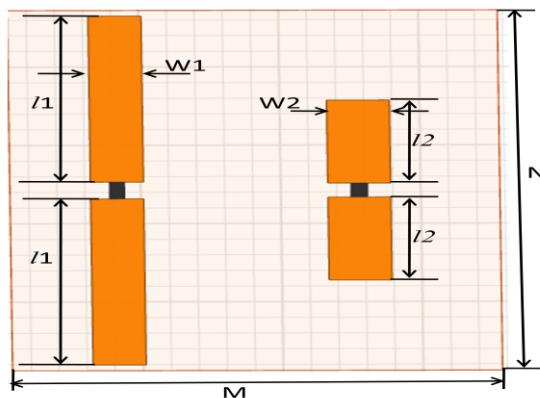


Figure 8a. Optimised design of unit cell of DD based CA-RAM.

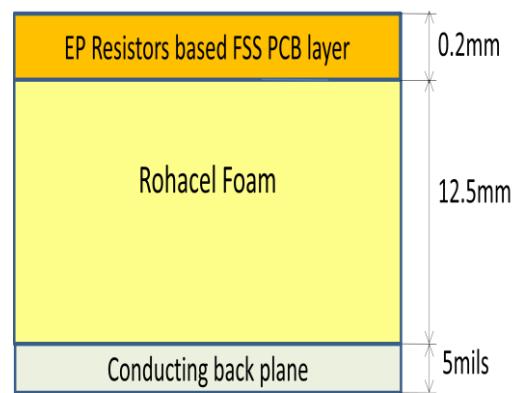


Figure 8b. Dielectric profile of the DD based CA-RAM.

III. RESISTIVE FSS PCB FABRICATION AND ASSEMBLY OF PANEL CA-RAM

The resistive FSS top layer of the DD based CA-RAM is designed as an electrically thin PCB using the PCB layout design software, Visula v2.3 and is developed on FR4 substrate of thickness 0.2 mm using conventional photolithographic technology. A commercially available resistive sheet of 100 Ohms/square is used for etching the EP resistors. The EP resistors at the centres of long and short dipoles are optimized for $R_1 = 150$ Ohms and $R_2 = 200$ Ohms respectively. It is noted that neither exotic chemicals nor a complicated fabrication process is required for design and fabrication of EP resistors.

Thus fabricated resistive FSS PCB layer is bonded to the Rohacel foam layer of thickness 12.5mm using a very thin, double sided Fixon^(R) tape. The conducting backplane comprises of a thin tin plated 3M copper foil, available in 1 ft. x 1 ft. rolls. The total thickness of RAM is 12.9 mm and the weight is 157 gm. A photograph of the assembled DD based prototype panel CA-RAM is shown in figure 9.



Figure 9. Photograph of the panel DD based CA-RAM. The grey colour filled rectangle at the centre of each dipole is the EP resistor. Size of panel RAM is (280 x 280) mm.

IV. RCS MEASUREMENTS ON PANEL RAM

RCS measurements are carried out on panel RAM in microwave anechoic chamber to verify the design and simulation. Monostatic RCS measurement set up is used for RCS measurements. The panel RAM is securely placed on an RF transparent thermocol stand on a single axis positioner and rotated in Azimuth from 0 to 360°. The conducting back plane serves as reference with which the RCS readings from RAM side are compared. High directivity standard gain horn antennas are used for transmission and reception. Continuously varying phase shifter and attenuator are used in the two sampled ports of directional couplers connected to the transmitting and receiving antenna for performing vectorial cancellation of the background at each measurement frequency. RCSR readings are taken with a frequency step size of 500 MHz in C band from 4 to 8 GHz. and at 8.5 and 9 GHz., in X-band and are available. A representative experimental RCSR plot of panel RAM is given in figure 10, for frequency of 5 GHz. for vertical polarization. It is observed that an RCSR of 15.5 dB is obtained at 5 GHz. Similar RCS plots of panel RAM are available at other mentioned frequencies in the band.

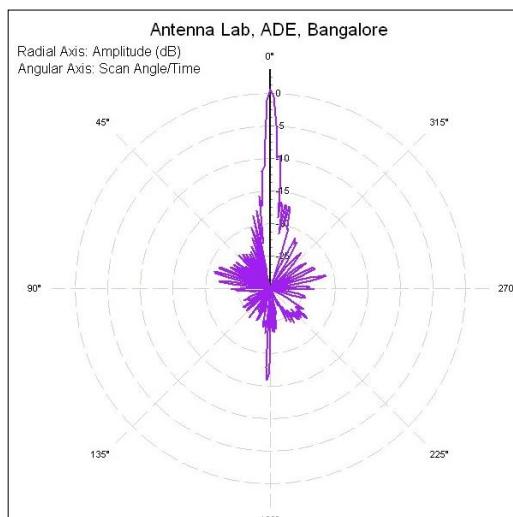


Figure 10. RCSR plot of DD based panel CA-RAM on polar chart. Frequency: 5 GHz. Polarization: VP.
RCSR= 15.5 dB.

V. DISCUSSION OF RESULTS

A panel RAM based on double dipoles with resistive FSS loaded by *innovative* embedded passives resistors is presented in this paper. The simulation results shown in Fig. 4 and measured results agree very well. Experimental RCSR of better than 10 dB has been recorded at all frequencies in the band except at 9 GHz. where 9 dB has been obtained. This is due to limitation in experimental setup. Best RCSR of 18 dB is recorded at 4.5 GHz. RCS experiments in S band namely from 2 to 4 GHz. need to be carried out. It is observed that simulated and measured results agree very well in C band and are encouraging.

i. The thickness of wide band RAM is 12.9 mm and meets the minimum thickness criterion of 8.8 mm. For similar RCSR performance, a 2 quarter wavelengths thick, 2 layer Jaumann radar absorber would require a thickness of 27.3 mm ($2\lambda/4$, $\lambda=5.4545$ cm. at 5.5 GHz.). Hence a thickness advantage of two times has been realized in this design. For better appreciation, design of a two layer Jaumann absorber for similar performance is given in figure 11.

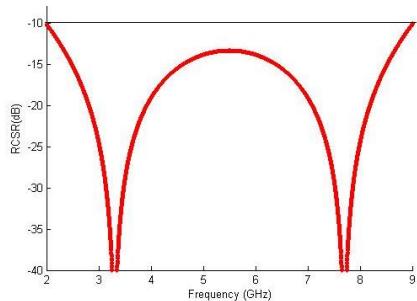


Figure 11. Two layer Jaumann RAM design for RCSR from 2 to 9 GHz.

ii. The weight of panel RAM is 157 gm. This reduced weight is realized with the use of light weight, Rohacel foam, which is an airworthy material with low dielectric constant. The crucial resistive FSS layer is realized as an electrically thin PCB with a thickness of 0.2 mm. Hence with the reduced weight and thickness, the RAM is suitable for airborne stealth applications.

iii. As mentioned earlier, the crucial and mandatory resistors essential for realizing resistive FSS have been realized integral to the substrate as embedded passives resistors which *results in a quantum improvement in reliability*. *Large number of different values of mandatory resistors can be realized on the same layer using this innovative methodology*, saving the PCB real estate with increased functionality [11-19].

iv. The CA-RAM presented in this paper can be used as RAS as both the FR4 substrate and the Rohacel foam used in RAM construction are airworthy materials. The conducting backplane can be replaced by Carbon Fibre Reinforced Plastic (CFRP) which is a structural material with good electrical conductivity, without any degradation in performance.

VI. CONCLUSION

A panel RAM based on double dipole FSS loaded with innovative embedded passives resistors is presented in this paper. The use of EP resistors has resulted in quantum increase in reliability with elimination of soldering and soldering related defects. The panel RAM is thin and wide band with reduced weight and meets the desired RCSR specifications. In the event of RAM application being the only viable RCSR design methodology in the lower microwave frequency bands such as L, S and C bands, the RAM finds applications in airborne stealth.

VII. SCOPE FOR FUTURE WORK

- i. Other resistive FSS geometries such as circular patches can be designed for realization of wide band RCSR performance from RAM.
- ii. The RAM design can be tested for conformality to curved surfaces such as cones, cylinders etc.
- ii. Different resistive FSS geometries such as Jerusalem cross patches with two-dimensional symmetry could be used for realization of circular polarization performance.

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Madhavkumar is Professor and Head of the Department of Electronics and Communication at SJCIT, Chikkaballapur. (Photograph not available at the time of publication).