ANALYSIS AND DESIGN OF SUBMICROMETER MOSFETS FOR HIGH PERFORMANCE: A REVIEW

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ABSTRACT

In this review we present the analysis and design of submicrometer MOSFETs for high performance. In particular we describe the very many second-order effects that occur or are further amplified in submicrometer MOSFETs. Then the scaling rules are examined, which make it possible to improve the speed and density of integration, fundamental requirements in the context of ULSI but which must be verified when a reduction of the MOS size. Particular attention is dedicated to the methods used to reduce the hot electron effects and, at last, we describe a submicrometer MOSFET, in which all the technological solutions adopted to improve the operating conditions of the device are highlighted.

KEYWORDS: *C.I, ULSI, Scaling Rules, Drain Engineering, Submicrometer MOSFET.*

I. INTRODUCTION

The integrated circuit (I.C.) was invented by Kilby in 1958. The first ICs were phase-shift oscillators and flip-flops, produced on a germanium substrate. Since the early 70s, the technology has produced integrated circuits with less than 30 devices per chip (SSI, Small Scale Integration), to progressively pass to MSI (Medium Scale Integration), characterized by 30 ÷ 10^3 devices per chip, to LSI (Large Scale Integration), with $10^3 \div 10^5$ devices per chip, to VLSI (Very Large Scale Integration), with $10^5 \div 10^7$ devices per chip, and to reach, since the early 1990s, ULSI (Ultra Large Scale Integration), characterized by $10^7 \div 10^9$ devices per chip [1-3].
This last type of technology mainly concerns the I.C. MOS, because they have reached the best levels in terms of integration density, low consumption and high production yields, so much so that they currently absorb 88% of the I.C. market.
The remaining part of the market belongs to I.C. bipolar (8%), while 4% concerns III-V semiconductors (MESFET and HEMT), which for now do not go beyond the VLSI. The miniaturization of devices implies a higher integration density, higher speed and therefore operation at ever higher frequencies, a reduction in power consumption and a reduction in costs.
Modern ULSI devices can switch at a speed greater than or equal to 100 Gb/s, consuming an energy (τ x P_D, where τ is the switching time and P_D the dissipated power) 6 times lower than that consumed by first I.C.
The evolution of integrated circuit technology brings devices closer to the limits imposed on their operation by fundamental physical laws.

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As a consequence, microscopic level phenomena that deteriorate the reliability of devices have replaced the spatial resolution of technological processes in determining the minimum dimensions of the structures to be integrated.
This review examines the design criteria of submicrometer MOSFETs for high performance, illustrating the problems associated with extreme miniaturization of the device and the technological solutions envisaged, with the aim of optimizing their characteristics and highlighting the reasons for adopting a particular technological solution.
The presentation is organized as follows.
At first, in Section II we analyze the second-order effects that occur or are further amplified in sub-micrometer MOSFETs, while the scaling rules are illustrated in Section III. Then the methods used to reduce the hot electron effects are described in Section IV. At last a submicrometer MOSFET, in which all the technological solutions adopted to improve the operating conditions of the device are highlighted, is presented in Section V, together with the conclusions.

II. EVOLUTION OF THE MOSFET

The rapid evolution of semiconductor electronics technology is due to the continuous demand for better performance and fierce international competition aimed at ever greater integration of devices. For MOS technology, this evolution is often measured in three-year generations: the time needed to improve memory capacity by a factor of 4 and to increase logic circuit density by a factor of between 2 and 3. This continues technological evolution is possible only through a reduction in the size of the MOS circuits, which passes through the improvement of the manufacturing technology, as well as of the lithographic technique and therefore of the maximum resolution obtainable with it. The reduction in the size of MOSFETs has been dramatic over the past three decades. Starting with a gate length of 10 μm in 1970 we gradually scaled down to 65 μm gate lengths, with a resulting reduction of 13% each year. Given the very considerable reduction in the dimensions of the devices, it is important to take into account the ever-increasing complexity of the manufacturing processes and the very many second-order effects that occur or are further amplified in sub-micrometer MOSFETs.
These effects can be classified into [4-5]:
• *Effects due to intense electric fields*:
1. effect of saturation of the speed of the carriers;
2. effects related to "hot electrons";
3. effect of carrier mobility degradation;
4. channel length modulation effect.

• *Effects of the short channel*.
In the process of miniaturization of the device, a methodology is typically proposed, which provides for the introduction of some rules, called scaling rules.
On the other hand, an improper scaling of the MOSFET dimensions alone can produce the presence or increase of the aforementioned second-order effects: just think of the significant increase in the electric field that occurs when the voltages at the device terminals are left unchanged and instead the length of the gate or the thickness of the gate oxide are reduced, with the consequent increase of leakage phenomena and of the effects of the short channel.
It is therefore of fundamental importance to carry out a correct scaling of the transistor in order to establish which parameters (geometric and/or technological) of the MOSFET can be increased and which decreased in order to improve the performance of the device itself.

III. MOSFET SCALING RULES

As far as the scaling rules [4-7] are concerned, the advantages afforded by integrated circuits, characterized by an increasingly high density of components, has prompted the designers, as already mentioned, to plan MOSFETs with ever smaller dimensions. Moreover the MOSFET, being structurally simpler than the BJT, lends itself better to a submicrometric integration.
However, if we only reduced the dimensions, without suitably modifying other parameters of the device itself, many of the properties of the MOSFET would be degraded. In fact, for example, if we reduce the length of the channel L, leaving the voltage applied between the drain and the source unchanged, the

electric field along the channel would become more intense. A stronger electric field reduces the gain, due to the saturation rate, or makes the effects due to hot carriers more intense. This problem can be solved by reducing the bias voltages, which should be scaled by the same factor by which the size of the MOSFET is reduced.
This way of proceeding has led to the formulation of a series of scaling rules, which make it possible to improve the speed and density of integration, fundamental requirements in the context of ULSI but which must be verified when a reduction of the MOS size.
The rules are not unique, as they depend on which symmetries you want to keep in the transition from the original MOS device to the one obtained with the scaling procedure. Indicating with $1/\lambda$ the scaling factor of the dimensions (λ greater than 1) and with 1/k that of the voltages (k greater than 1), we have the following MOSFET scaling rules:

PARAMETERS	**VARIABLES**	**SCALING FACTOR**
Dimensions	W, L, x_{oss}, r_j	$1/\lambda$ (reduction)
Potentials	V_{DS}, V_{GS}	$1/k$ (reduction)
Conc. Doping	N_A, N_D	λ^2/k (increase, if $\lambda > k^{1/2}$)
Electric field	$\mathcal{E}$	λ/k
Current	I_{DS}	λ/k^2
Gate delay	τ_{pd}	k/λ^2

having indicated with W the width of the MOSFET, L the length of the channel, x_{oss} the thickness of the oxide and r_j the junction depth.

The scaled values of the parameters $\mathcal{E}$, I_{DS}, τ_{pd} are obtained by replacing the scaled values of the dimensions, potentials and dopant concentration parameters in the basic equations of the MOSFET.
The parameters λ and k can be varied independently of each other, following however two main methodologies:
1) *Scaling with constant electric field,* **i.e. k = λ**
Gate size, potentials, current, and delay decrease resulting in increased device speed. However, using the basic MOSFET equations, it can be shown that the threshold voltage VT decreases by a factor of approximately 1/k. 2) *Scaling at constant voltage*, **so k = 1**
In this case the potentials remain constant and the current increases, proportional in saturation to $(V_{GS} - V_T)^2$, the time τ_{pd} decreases, thus obtaining a greater increase in the speed of the device with respect to case 1). Furthermore, this scaling is more advantageous because, if the potentials remain unchanged, the threshold voltage V_T also remains constant, thus avoiding sub-threshold dispersion phenomena which occur when V_T decreases.
Moreover, scaling at constant voltage poses serious problems of reliability, i.e. reduction of the average life time of the device, when working with very high electric fields.
MOSFETs initially operated at 5.0 V, then 3.3 V, now 2.0 V, and the prospect is to go 1.5 V down to 0.9 V. As the length L of the scaled device has decreased, the resulting increase in electric field causes the onset of the phenomenon of hot electrons, which however can be solved by adopting technological solutions that complicate the structure of the device (see LDD structure).
If only the gate length is decreased, without adopting the scaling rules, the MOSFET operates in the short channel regime.
In this situation we can state that:
- the output impedance of the MOSFET is smaller;
- the subthreshold current I_{Dst} depends on V_{DS}, while in the long-channel MOSFET model it depends on V_{GS} according to the known relationship:

$$I_{Dst} \approx e^{\frac{q(V_{GS}-V_T)}{kT}}$$

- V_T drastically decreases with gate length (short channel effect).
Ultimately, the short channel effects determine a worsening of the g_m transconductance of the device because there is a less effective control of the V_{GS} voltage on the I_{DS} current.

Moreover, a fundamental hypothesis, for the purpose of deducing the mathematical model of the MOSFET, is that the charge in the surface space charge region is solely a function of the voltage between the gate and the substrate. This assumption fails near the source and drain space charge region, where the p-n junctions, as well as the gate, affect the surface space charge.
Furthermore, when the length L of the channel is much greater than the thickness of the depletion regions, this assumption causes entirely negligible errors.
However, reducing the channel length, errors can be made in estimating the threshold voltage due to an amount of charge in the space charge region, connected to the gate, significantly smaller than that predicted by first order theory. The remaining charge is connected to the depletion regions of the p-n (substrate-channel) junction.
There is an empirical formula that allows calculating the lower limit for L, which is also valid for submicrometer devices:

$$L_{min} = 0.4\left[r_j x_{oss}\left(X_D + X_S\right)^2\right]^{1/3}$$

in which:
r_j indicates the joint depth, in µm;
x_{oxx} the thickness of the oxide, in Å;
X_D and X_S are the extent of the depletion region below the drain and the source, respectively, in µm.
The depletion regions (X_D and X_S) are reduced because the doping must be increased in the scaling process of the device.
The x_{oss} thickness of the oxide can be fabricated down to less than 50 Å, although this can be achieved through delicate and expensive processes.
The major problem is the reduction of the junction depth r_j because it implies an increase in the parasitic series resistances R_D and R_S of the device.
It is therefore necessary to understand the effects caused by serious resistances.
To this end, the concept of **mobility reduction factor θ** should be introduced.
If the electric field in the channel increases, the density of the carriers in the channel also increases and this produces an increase in the scattering of the carriers between them and with the Oxide-Silicon interface, with consequent degradation of the µ mobility.
An empirical expression modeling the degradation of mobility has been proposed in the literature:

$$\mu_{eff} = \frac{\mu_n}{1 + \theta\left(V_{GS} - V_T\right)} \quad (1)$$

where μ_n denotes the mobility of electrons in the channel when V_{GS} is equal to the threshold voltage V_T.
For an ideal MOSFET (i.e. without parasitic resistance and without mobility degradation) operating in the linear region, the drain current is given by the well-known relationship [4-5]:

$$I_{DS} = \mu_n C'_{oss} \frac{W}{L}\left(V_{GS} - V_T\right)V_{DS} \quad (2)$$

If we add the parasitic series resistances R_D and R_S to the ideal MOSFET, considering them external to the ideal device, and we also take into account the mobility degradation, Eq.(2) can be rewritten as follows:

$$I_{DS} = C'_{oss} \frac{W}{L} \frac{\mu_n}{1 + \theta\left(V_{GS} - R_S I_{DS} - V_T\right)}\left[\left(V_{GS} - R_S I_{DS}\right) - V_T\right]\left[V_{DS} - \left(R_S + R_D\right)I_{DS}\right]$$

that is to say:

$$I_{DS} = C'_{oss} \frac{W}{L} \mu_n \frac{\left(V_{GS} - V_T\right)V_{DS}}{1 + \left[\theta + C'_{oss} \frac{W}{L} \mu_n \left(R_S + R_D\right)\right]\left(V_{GS} - V_T\right)} \quad (3)$$

Eq. (3) can be written as:

$$I_{DS} = C'_{oss} \frac{W}{L} \mu_n \frac{\left(V_{GS} - V_T\right)V_{DS}}{1 + \left[\theta + \Delta\theta\right]\left(V_{GS} - V_T\right)}$$

having placed:

$$\Delta\theta = C'_{oss}\frac{W}{L}\mu_n\left(R_S + R_D\right)$$

Ultimately, the increase in the parasitic resistances R_D and R_S produces an overall increase in the mobility reduction factor θ, with consequent degradation of the transconductance of the device.
The effect is particularly noticeable for small gate lengths, as il is proportional to 1/L.
The second problem that degrades the performance of a submicron MOSFET is the presence of contact resistance R (spreading resistance of the contact).
For bipolar transistors and other devices with vertical current flow, the effective contact resistance is proportional to the specific contact resistance R_C ($\Omega \cdot cm^2$) according to the relationship:

$$R = \frac{R_C}{Area}$$

assuming the contact size is not very small.
In the case of a MOS device, however, assuming that the contact extends across the entire width W of the device, the effective contact resistance R can be calculated using the expression deduced from the one-dimensional model of the transmission lines:

$$R = \frac{\sqrt{R_C\rho_D}}{W}\coth\left(L_C\sqrt{\frac{\rho_D}{R_C}}\right) \quad (4)$$

where ρ_D indicates the layer resistance (Ω/□) and L_C the contact length.
Eq. (4) can be approximated in the following two cases, with an accuracy of about 10%:

$$R = \frac{R_C}{WL_C} \quad \text{if} \quad L_C < 0.6\sqrt{\frac{R_C}{\rho_D}}$$

or

$$R = \frac{\sqrt{R_C\rho_D}}{W} \quad \text{if} \quad L_C > 1.5\sqrt{\frac{R_C}{\rho_D}}$$

For submicrometer MOSFET it is obviously necessary to make small contacts and this leads to an undesirable increase in the parasitic contact resistance R.
Several technological processes [8-9] have been developed to solve the above problem.
The most widespread is the **technique of self-aligned salicidation** of the contact area, with which it is possible to increase the contact area.
First of all, the source and drain regions are formed by diffusion. The gate is then encapsulated with oxide. Before making the metallizations, a metal is deposited on the silicon, typically Titanium or Platinum, and it is made to react (*sintered*) with the silicon, which should have formed the contact.
The reaction produces a layer of **silicide**, i.e. titanium silicide ($TiSi_2$) or platinum, thus realizing, with the subsequent metallization step, a greater contact area with a material (silicide) more conductive than simple doped silicon.
Salicidation is a delicate and expensive process, which however drastically reduces the parasitic resistances of the MOSFET.
Typically for MOS 0.25 μm titanium or cobalt silicide is used, with particular precautions in the sputtering of the metal and in the subsequent annealing to obtain the silicide.
Please refer to the texts in the bibliography for further insights [7-9].

IV. Methods to Reduce Hot Electrons Effects: Drain Engineering

When scaling at constant potential, the electric field in the device channel increases significantly.
When it is so high that, with reference, for example, to a NMOSFET, the energy gained by the electrons between successive collisions (free path of about 100 Å) reaches energy values higher than the **impact ionization threshold energy**, these highly energized electrons (therefore called **hot electrons** [10]) generate an electron-hole pair due to the impact with other particles (in this situation the hot electrons manage to avoid phonon scattering).

One of the possible effects is that many of these electrons gain enough energy and momentum, along the direction of the silicon dioxide, to allow these electrons to overcome the potential barrier at the Si/SiO_2 interface and damage the oxide, or to create positive charges both by impact ionization in the oxide and by the formation of H^+ ions (forfeited during the various technological processes) at the gate electrode.

Since this charge can be trapped in the oxide, the main deleterious effects are a shift in the threshold voltage V_T and a decrease in the transconductance g_m of the MOSFET.

The creation of H^+ ions at the gate-silicon dioxide interface is undoubtedly one of the mechanisms that most heavily degrades the performance of the device.

In fact these ions passivate the interface creating uncompensated bonds, which can be split with just 0.3 eV of energy, creating surface states or traps, which degrade the performance of the MOSFET, as they can capture carriers.

Experimentally it has been seen that this effect is stronger at the drain, especially when the MOSFET operates in saturation and with voltage $V_{GS} \approx V_{DS}/2$.

Moreover, performing the scaling with a constant electric field, it has been observed that the aforementioned effect becomes less important for gate lengths $L \leq 0.2$ μm due to the low voltages used.

Ultimately, the phenomenon of hot electrons limits the maximum usable power supply voltage.

To deal with this problem, scaling rules have been developed aimed at keeping the maximum electric field constant, but not the average one.

Therefore, with the same progressive voltage drop between drain and source, it is necessary to increase the effective distance over which this drop occurs.

In particular, on the side of the drain, in saturation, the drain-substrate junction behaves like an inversely biased p-n junction, for which, as is known, the maximum electric field is in correspondence with the metallurgical section.

Furthermore, an electron must travel at most 4 free medium paths to acquire an energy equal to that to produce impact ionization, and become "hot".

It follows that to prevent the phenomenon of hot electrons it is necessary to act on the drain (**drain engineering**) where the maximum electric field is located (even if then the technological processes used are also applied to the source for symmetry reasons), or:

- increasing the number of collisions of the wearers, thus reducing their mean free path, or
- making the doping of the drain-substrate junction gradual, with a consequent reduction of the maximum electric field.

The first attempt at drain engineering is the **double-diffused drain** [9], a technique in which phosphorus atoms are first implanted into the substrate and subsequently arsenic atoms at a higher concentration to form the source and drain regions.

Since phosphorus diffuses faster than arsenic, phosphorus is the predominant profile near the channel edge, and the drain-substrate junction (doped with boron atoms) is not too abrupt.

The subsequent implantation of arsenic atoms substantially produces a shift towards the drain of the metallurgical section and therefore also part of the space charge region of the drain-substrate junction moves towards the drain.

In particular, if the concentration of phosphorus atoms is suitably calculated, the depletion region on the drain side can be made to comprise only the phosphorus atoms, so that the effective drain region is the one doped with arsenic atoms. Also under the gate, due to lateral diffusion, a similar doping profile is created.

In this way a reduction of about 20% of the maximum electric field is obtained, but with the disadvantage of increasing the depth of the drain-substrate and source-substrate junctions, with the consequent onset of short channel effects.

Alternatively, the **Lightly Doped Drain** (**LDD** [11]) technique is used, i.e. the drain (and source) region is created with a first more extensive diffusion of atoms at a concentration N_D^-, and then with a second diffusion at a less extensive concentration N_D^- but deeper.

The effect is always to create a gradual doping profile of the drain (and source) region in order to reduce the maximum electric field.

The decrease in the intensity of the electric fields is clearly illustrated in [11], where it shown the trend of the electric field at the SiO_2 interface as a function of the junction depth, obtained through a two-dimensional simulation, both for a conventional device and for one made with the LDD technique.
Ultimately, the LDD MOSFET is more reliable in relation to the phenomenon of hot electrons, but, however, it is slower, as the LDD structure increases the parasitic resistances: it is therefore necessary to seek a compromise between performance and device reliability.

V. SUBMICROMETER MOSFETS

Another problem associated with submicrometer MOSFETs is **the growth of oxides** with thickness varying between 40 and 100 Å. Such thin oxides are particularly vulnerable to the phenomenon of hot electrons, as well as to the presence of other spurious charges, which can even cause the phenomenon of dielectric breakdown.
The ability of the oxide to resist the aforementioned phenomena is known as **the strength of the oxide**.
The growth of thin oxides is, however, a problem that can only be solved by refining the technological processes.
Furthermore, as the size of the device is reduced, the depth of the source and drain junctions is also reduced, thus realizing surface junctions.
Moreover, since drain and source are very close, the phenomenon of **DIBL** (**Drain Induced Barrier Lowering** [4-5]) takes place, i.e. a lowering of the potential barrier on the side of the gate towards the source, due to the drain bias, allowing to a greater number of carriers to broadcast from the source region towards the channel.
This manifests itself in the form of a strong degradation of g_m, i.e. in the need for greater excursions of the V_{GS} to modulate the I_{DS}.
Moreover, the DIBL phenomenon causes a reduction ΔV_T of the threshold voltage according to the relationship [4-5]:

$$\Delta V_T \propto \exp\left(-kLr_j^{-1/3}x_{oss}^{-1}\right) \quad (5)$$

where k is an empirical constant, dependent on the technology.
Therefore, in order not to reduce too much the threshold voltage V_T, it is necessary to reduce the junction depth r_j as the device is scaled.
However, this implies an increase in the layer resistance of the source and drain diffuse regions, before salicidation.
Most deeply scaled technologies have layer resistance values ranging from 500 to 1000 Ω/□.
In particular, the surface concentration is of great importance, because the specific contact resistance depends on it.
Suitably shaping the doping, both in depth and for the length of the channel, so as to optimize the performance of the device and/or to prevent short channel effects, is possible but with very high costs and complex technological processes.
Fig. 1 shows the cross section of a submicrometer MOSFET, in which all the technological solutions adopted to improve the operating conditions of the device are highlighted.

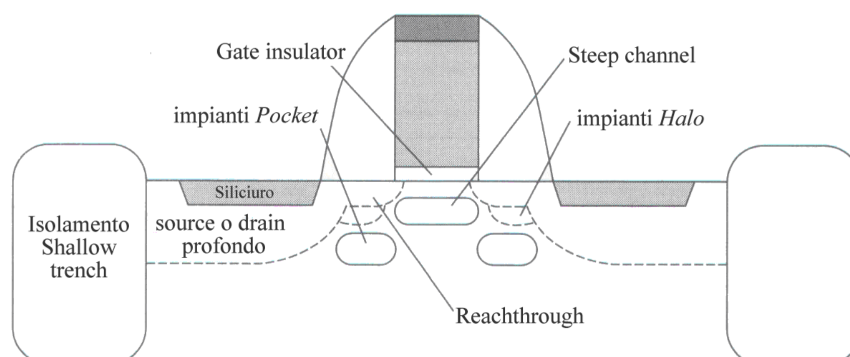

Figure 1. Cross section of a submicron MOSFET.

In particular, the silicide layers on the source, drain and polysilicon gate regions have been inserted to decrease the parasitic resistances.
The source and drain regions have been made according to the LDD technique or variants, with the aim, as already mentioned in the previous paragraph, of minimizing the effects from hot electrons.
Furthermore, the doping profile of the aforementioned regions, being n^- close to the Si/SiO_2 interface, allows to prevent the RCS of the source-substrate and drain-substrate junctions from coming into contact with each other, i.e. avoiding the *reachthrough* [4-5].
Moreover, it is advisable to keep the doping of the substrate high to avoid both the reachthrough and the body effect; its value must be chosen so as to minimize the latch-up phenomenon [4-5].
The performance of the device is improved by shaping the doping profile in and around the channel, introducing a **steep channel**, obtained with implants having the concentration peak and depth below those of the source and drain regions.
Often for these systems it is preferred to use indium instead of boron because indium has a lower diffusion coefficient than boron and therefore the depth of penetration is reduced.
The reason for introducing the steep channel is to create a concentration gradient of (positive) charges, and therefore an electric field in the channel which, by removing the (negative) charges, produces their reduction with consequent reduction of scattering and therefore an increase of mobility.
Halo implants (n^-) prevent short channel effects by shielding the channel from deeper (n^+) source and drain regions.
Pocket implants (n^-) decrease the extension of the source and drain depletion regions, thus reducing the DIBL phenomenon, i.e. reducing the dependence of the threshold voltage on the gate length L, and the dependence of the subthreshold current on the drain-source bias voltage V_{DS}.
Finally, the **shallow trenches** have the purpose of guaranteeing electrical insulation between adjacent devices and preventing the latch-up phenomenon.

VI. CONCLUSIONS

The contraction of the geometries of the devices (active, passive and interconnection lines), which characterizes the development of microelectronics, inevitably entails a worsening of the operating conditions of the structures with worrying effects on their reliability characteristics. This process is inevitable given that technology rapidly evolves towards the ultimate limits imposed on the proper functioning of the device by fundamental physical laws and that approaching this condition reduces, by definition, the safety margins of past generations of components. Furthermore, the increasingly microscopic nature of the phenomena that lead to the failure of devices and, consequently, the growing difficulty of recognizing and studying them, will lead to an increasingly systematic use of sophisticated analysis techniques for complex ULSI circuits, requiring that all large users of electronic components develop and acquire vast and diversified skills (from the chemistry and chemical-physics of processes to experimental techniques and system architecture) as well as means and equipment increasingly similar to those used up to now only by manufacturers of integrated circuits.

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