EFFICIENT REVERSIBLE MULTIPLIER CIRCUIT IMPLEMENTATION IN FPGA

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ABSTRACT

Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. The applications of reversible logic gates include ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc. This paper proposes an improved design of a multiplier using reversible logic gates. A 4x4 reversible multiplier circuit is proposed with the design of new reversible gate called RAM gate. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, and constant inputs. The design can be generalized to construct nxn reversible multiplier circuit.

KEYWORDS: *Reversible logic, Constant/Garbage input, Garbage output, Quantum cost, Reversible multiplier.*

I. INTRODUCTION

Power dissipation is an important factor in VLSI design as modern logic circuits offer a great deal of computing power in a small footprint. The combinational logic circuits dissipate heat of KTln2 joules [1] for every bit of information erased during computation, where k = 1.3806505x10-23J/K is Boltzmann constant and T is the operating temperature in degrees at which the computation is carried out. Also, as Moore predicted that the number of transistors approximately doubles in every eighteen months and if this trend continues to hold, in the near future more and more energy will be lost due to the loss of information. Charles Bennett [2] showed that energy loss could be avoided or even eliminated if the computations are carried out in reversible logic and also proved that circuit built from reversible gates have zero power dissipation. Thus reversible logic appears to be promising in future low power design applications.

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware result in energy dissipation due to information loss [3]. According to Landauer's principle, the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [3]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components [6]. In 1973, Bennett, showed that one can avoid KTln2 joules of energy dissipation constructing circuits using reversible logic gates [7].

An efficient design in reversible logic should have the following features [5]: (a) use minimum number of reversible logic gates (b) should have less number of garbage outputs (c) less number of constant inputs and (d) minimization of quantum cost. Addition and multiplication operations

are widely used arithmetic operations in many computations. High speed multiplier circuits are of particular interest in processor design [8].

In this paper, we presented a reversible 4x4 multiplier with the design of new reversible gate called RAM. The proposed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost, and this design can be generalized to construct reversible NxN multiplier.

The background work in this area is discussed in section 2, followed by the proposed RAM gate structure and multiplier design in section 3. The simulation setup is discussed in section 4. The implementation results are tabulated and compared with other implementations in section 5. Section 6 and 7 give the conclusions and future scope.

II. BACKGROUND WORK

Himanshu Thapliyal and Srinivas [9] proposed an NxN reversible multiplier using TSG gate. In this the partial products are generated using Fredkin gates and addition using reversible parallel adder designed from TSG gates and demonstrated that the multiplier architecture using TSG gate is optimized. Majid Haghparast et al., [10] presented two new 4x4 bit reversible multiplier designs which have low hardware complexity, less garbage input/output bits and less quantum cost and implementation of reversible HNG is also presented. Noor Muhammed Nayeem et al., [11] explained the use of reversible logic for designing the Arithmetic Logic Unit of a crypto processor. A reversible carry save adder using modified TSG gates and architecture of Montgomery multipliers are also discussed. Maryam Ehsanpour et al., [12] explored the reversible 4-bit binary multiplier circuit using new reversible device called modified full adder with low hardware complexity, fewer garbage outputs and constant inputs.

Sebastian Offermann et al., [13] presented synthesis of multiplier circuits in reversible logic and three methods are discussed to address the drawback of the previous approaches. Fateme Naderpour and Abbas Vafaei [14] proposed the reversible multiplier with decreasing the depth of the circuit by reducing quantum cost and garbage outputs. Anindita Benerjee and Anirban Pathak [15] presented the reversible multiplier design which has two components, reversible partial product generation circuit and reversible parallel adder circuit to minimize number of garbage output bits, gate count and quantum cost. Nidhi Syal and Sinha [16] presented a 4x4 universal reversible parity preserving reversible logic gate which matches the input parity with the output parity. It can be used to synthesis any given Boolean function and offers less hardware complexity and improved parameter efficiency.

Himanshu Thapliyal and Nagarjan Ranganathan [17] proposed a design of reversible BCD adder which is primarily optimized for the number of input bits and number of garbage outputs, results in the reduction of quantum cost and the delay. Himanshu Thapliyal and Nagarjan Ranganathan [18] presented the design of the reversible half and full subtractor based on the quantum gate implementation of the reversible TR gate. The reversible half and full subtractor shown better in terms of the quantum cost, delay and minimum number of garbage outputs. Michael Nachtigal et al., [19] presented the reversible floating-point adder that follows the IEEE 754 specification for binary floating-point arithmetic. Majid Haghparast et al., [20] proposed 4x4 bit reversible multiplier circuit, is faster and has lower hardware complexity. The use of reversible gate to construct multiplier is presented.

III. PROPOSED MULTIPLIER DESIGN

3.1. The Proposed 4x4 Reversible RAM gate

The proposed 4X4 reversible gate called RAM gate is shown in figure 1. The inputs (A, B, C, D) mapped to outputs (P = A, Q =A $\oplus$ B, R = A $\oplus$ B $\oplus$ C, S = A $\oplus$ B $\oplus$ C $\oplus$ D). The RAM gate is mainly useful in copying the signal as reversible logic has a fan-out of one.

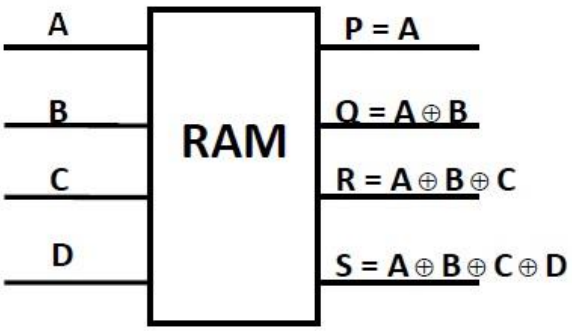

Figure 1. RAM gate

3.2. Reversible Multiplier Design

A reversible 4x4 multiplier circuit has two parts: Partial Product Generation (PPG) circuit and Multi-Operand Addition (MOA) circuit. The details of these two parts are discussed in the following sections:
The RAM gate quantum implementation is shown in figure 2. It has a quantum cost of three as it requires three CNOT gates and by making B, C and D inputs as logical low i.e., control input, then the input signal A is copied at all the four outputs as shown in figure 3.
Hence it is useful in partial product generation circuit of reversible multiplier circuit.

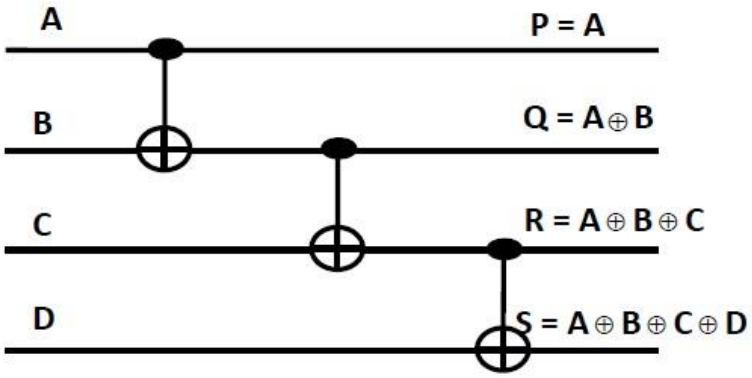

Figure 2. Quantum implementation of RAM gate

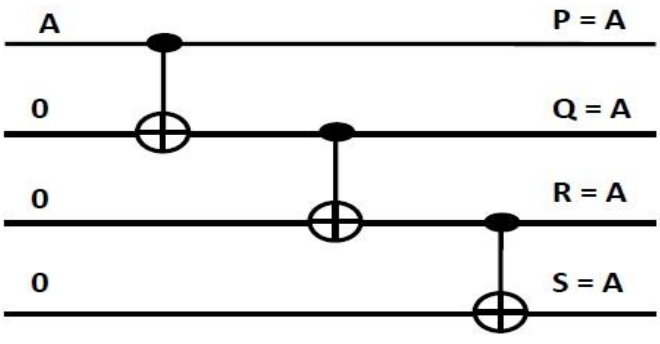

Figure 3. RAM gate as copying circuit

3.2.1 Partial Product Generation

The basic operation of 4x4 parallel multiplier is depicted in figure 4. It consists of sixteen partial products of the form Xi.Yi, where i vary between 0 and 3.

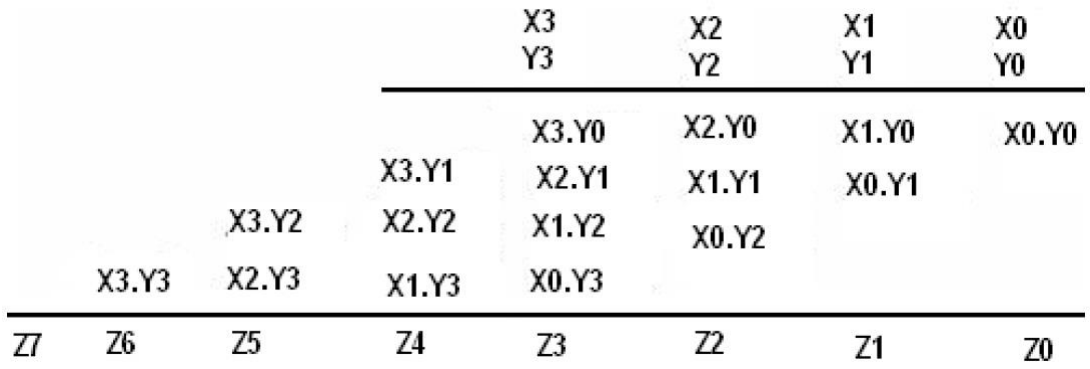

Figure 4. The basic operation of 4x4 parallel multiplier

The PPG circuit using Peres and RAM gates is as shown in figure 18. Here sixteen PG gates are used to generate sixteen partial products as shown in figure 4. The RAM gate is used as a copying gate, for each Xi input four copies are generated and totally sixteen input signals are copied using four RAM gates as shown in figure 5.

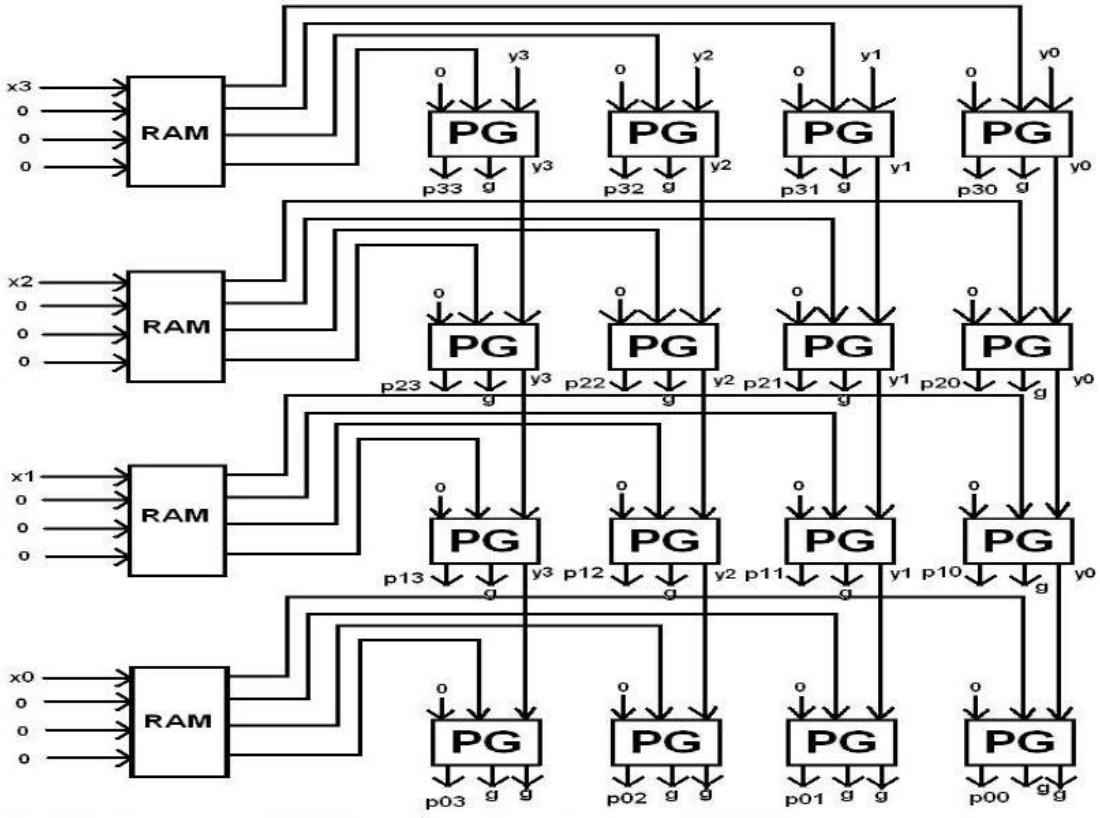

Figure 5. Proposed reversible partial products generation circuit using Peres and RAM gates

3.2.2 Multi-Operand Addition

The addition of the partial products using DPG and PG gates is as shown in figure 6. The basic cells for such a multiplier is full adder using DPG with three inputs and one constant input, two garbage outputs and half adder using PG with two inputs and one constant input, one garbage output.
The proposed reversible multiplier circuit uses eight DPG gates, four PG gates, sixteen PG gates for partial product generation and four RAM gates for fan-out creation. It is possible use FG gate as copying circuit, but it requires twelve FGs instead of four RAM gates and by using RAM gate the hardware complexity and garbage outputs are reduced.

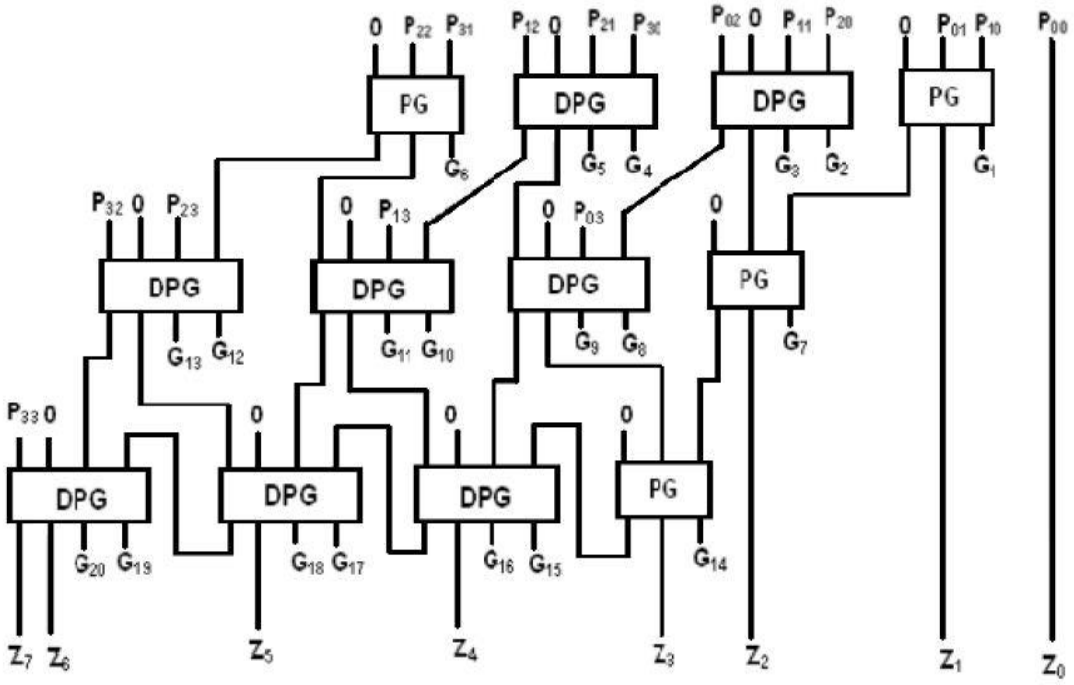

Figure 6. Reversible multi-operand addition circuit

IV. SIMULATION SETUP

The RAM gate presented above has been fully coded in VERILOG Hardware Description Language (VERILOG). Once the design is coded in VERILOG, the Modelsim XEIII 6.2c compiler [21] and the Xilinx Foundation ISA Environment 9.1i [22] generate a net-list for FPGA configuration. The net-list can then be downloaded into the FPGA using the same Xilinx tools and Texas Instruments prototyping board (see figure 7). LUT based random access memories (RAMs) and flip-flops are used to implement feedback memory.

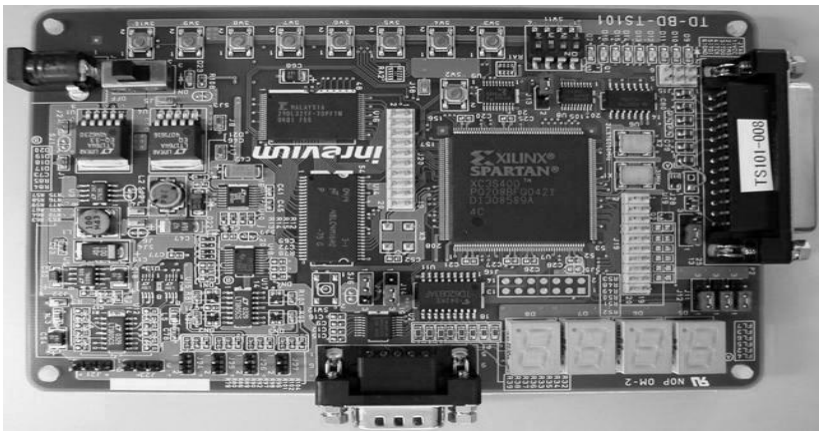

Figure 7: Xilinx Spartan3 FPGA kit

V. IMPLEMENTATION RESULTS

The proposed reversible multiplier circuit is more efficient compared to the existing circuits presented by [23], [24], [25], [26], and [27]. This can be comprehended easily with the help of the comparison results shown in table 1.

Table1. Comparison of existing and proposed reversible multiplier designs

	No. of Gates	No. of Garbage Inputs	No. of Garbage Outputs
[23]	40	52	52
[24]	42	42	49
[25]	44	44	52
[26]	28	32	28
[27]	28	28	28
Proposed	28	22	28

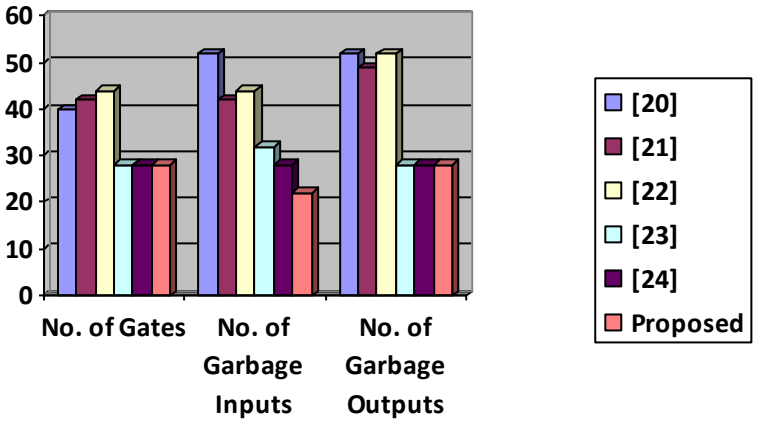

Figure 8. Comparison of proposed and existing reversible multiplier designs

The difference between proposed and existing design is mainly in the partial product generation block. In our design, a new RAM gate is used to create fan-out instead of Feynman gate in the existing designs. By using RAM gate the quantum cost and garbage outputs are reduced. It is clear from figure 8 that the proposed reversible multiplier circuit is better than the existing designs in terms of number of gates, quantum cost, garbage inputs and garbage outputs.

VI. CONCLUSIONS

In this paper a new reversible gate called RAM gate is proposed for copying the operand bits of the multiplier. This results in reducing the number of fan-out gates by 50%. This also reduces the total cost and the size of the circuit which are very important design parameters. The number of gates, garbage inputs, garbage outputs and quantum cost are analyzed. It is seen that number of gates, garbage inputs, garbage outputs and quantum cost values are less in the proposed design compared to the existing approaches.

VII. FUTURE WORK

The design can be extended to construct nxn reversible multiplier circuit. The prospect for further research includes the reversible implementation of more complex arithmetic circuits with less garbage outputs and low quantum cost.

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