LEAKAGE POWER REDUCTION OF ON CHIP SRAM CELLS

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ABSTRACT
Exponential growth of battery based porartable applications mandatory new SRAM cell but this cell stand by leakage power has become a major issue in recent trend low power fabrication with technology scaling and for high temperature operations. In this work has emphasized on low power dissipation, read/write delay and stability of SRAM cell. Paper shows the performance of a new LP12T cell. The proposed LP12T cell is compared with traditional LP10T and 6T cell on MICROWIND 3.1 simulator using BSIM4 model for 120 nm and 65nm at wide range of temperature. The average power dissipation is reduced for 120nm and 65nm respectively and the time response for read/write operation is slightly improved compared to LP 10T and 6T cell at mentioned scale.

INDEX TERMS*— Low power SRAM,power consumption, read/write delay, 12T, leakage current, standby current and SNM.*

I. INTRODUCTION

On-chip memory arrays have become widely used subsystems in many VLSI circuits, and commercially available single-chip read and write memory has reached gigabyte range, but the power consumptions and the delay in the interconnections have also increased proportionally which restricts the amount of packaging.
With the dependence of the leakage power on the number of transistors, and given the projected large memory content of future SOC (System on Chip) devices (more than 90% of the die area by 2014 [1]), it is important to focus on minimizing the leakage power of SRAM structures**.** As the CMOS process technology continues to scale to the nanometer regime,process variation and leakage current of transistors become more severe, which are further aggravated by the fluctuation of the operation conditions such as the variation of the supply voltage and/or the temperature leads to a higher chance of device malfunctioning. Furthermore, leakage is the only source of energy consumption in an idle circuit. Hence, the design of low-leakage SRAM cell is highly desirable. The paper is organized as follows Section II presents a brief functional overview of the Conventional 6T SRAM Cell, Section III explains briefly LP10T SRAM cell, Section IV Functional approach of LP 12T gives the Section V gives the simulation work performed on 6T,10T,LP10T,LP12T SRAM cell and Section VI gives conclusion of the work.

II. FUNCTIONAL APPROACH

The Conventional SRAM (CV-SRAM) cell has Six MOS transistors (‘4’ nMOS and ‘2’ pMOS), Figure1. Unlike DRAM it doesn’t need to be refreshed as the bit is latched in. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell made of one transistor and one capacitor thereby increasing the complexity of the cell [2].

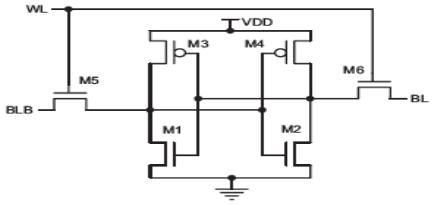

Figure 1: 6T-CMOS SRAM Bit-Cell

i) Standby Operation (Hold): When WL = '0', M5 andM6 disconnect the cell from Bit-Lines (BL and BLB). The two cross-coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are disconnected from the outside world. The amount of current drawn in this state from the power supply is termed as stand by current.
ii) Data Read Operation: Read cycle starts with pre charging BL and BLB to '1', i.e., VDD. Within the memory cell M1 and M4 are ON. Asserting the word line, turns ON the M5 and M6 and the values of Q and Q' are transferred to Bit-Lines (BL and BLB). The M4 and M6 pull BL upto VDD, i.e.BL = '1' and BLB discharges through M1 and M5. This voltage difference is sensed and amplified to logic levels by sense amplifiers.
iii) Data Write Operation: The value to be written is applied to the Bit lines. Thus to write data '0', we assert BL=0, BLB = '1' and to write data '1', the BL = '1', BLB = '0', asserted when WL = '1'.
2.1 THE P-P-N BASED 10T SRAM CELL A 10T SRAM cell, Figure2, as the name suggests, consists of 10 transistors. Out of these transistors, four are pull-up transistors (PUL1, PUL2, PUR1 and PUR2), four are pull down transistors (PDL1, PDL2, PDR1 and PDR2) and two are access transistors (PGL and PGR)[3]. The two pull-down transistors i.e. PDL1 and PDR1 are connected to VGND. ThisVGND signal is connected to ground during the read operation and VDD, otherwise. In 10T SRAM cell, the access transistors are connected to pseudo nodes (pQ and pQb i.e. nodes between two pull-up transistors) rather than the storage nodes (i.e. Q and Qb). Due to this, the storage nodes are isolated from the BLs and therefore during the read operation, the read current does not flow through the storage nodes and hence maintain the read stability. In case of the write operation, the VGND is connected to VDD and one of the bit-lines e.g. BL is grounded. Suppose the node Q is storing '1' and node Qb is storing '0'.

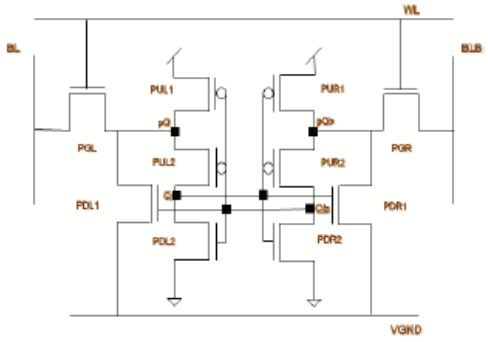

Figure 2: The 10T SRAM Cell

When a high supply voltage is provided, the node Q is pulled down to '0' due to discharging through the access and the pull-up transistor i.e. PGL and PUL2.

III. OPERATION OF LP10T SRAM CELL

The LP10T SRAM cell [5] can operates in three modes i.e. standby mode read mode and write mode. For the read and write operation the circuit (SRAM-cell) must have a good read stability, write-ability and good access time. The access time of the LP10T SRAM cell is discussed.
Read Access Time (TRA). Read access time or read delay is the time when RWL (WL-word line) is activated to the time when bit line (BL) /Bit line bar (BLB) is discharged by 50-mV from its initial high level [10]. The 50-mV differential between BL and BLB is good enough to be detected by a

sense amplifier thereby avoiding misread [9]. For read operation first we pre charged the bit lines, MN1 is ON, storage node "Qb" store a "0" and "Q" stores a "1" (assumed). When WL is activated, BLB drops through MN3/MN1.Read operation in case of LP10T SRAM cell write word line and read word lines are separated. To read "1" in LP10T SRAM cell we enabled the MN8 transistor in this case write word line is deactivated due to which MN6 turned OFF and "1" turns MN7 ON, which raise the internal voltage at contact of MN8 transistor to value higher than zero. In this sequence 50-mV differential voltage between B L and BLB is developed, which is useful to detect by sense amplifier.

Write Access Time (TWA). Write access time or write delay (TWA) is the time required for writing "0" to storage node "Qb" from the time when WWL (WL) is activated to the time when "Qb" falls to 10% of its initial high level (i.e. it's 90% swing). Similarly TWA for writing "1" to "Qb" is time when WWL is activated to them when "Qb" rise to 90% of its initial low level. This avoids miswrite in write operation of the LP10T SRAM cell (Figure 1) when WWL (write word line) line is activated and MN8 transistor is deactivated.

IV. FUNCTIONAL APPROACH OF LP10T& LP12T

We analyzed a low power full differential LP12T SRAM (Figure 4) cell and compared with the low power 10T SRAM bit-cell (Figure 3). The low power 10T SRAM cell is sized to maintain pull-up (PU) device < pass-gate (PG) device < pull-down (PD) devices. Device sized width for the LP10T SRAM cell2.WPU/ WPG/ WPD are chosen as 80nm/120nm/160nm respectively in 32nm and 100nm/150nm/200nm in 45nm technology. And the size W of (W5/6/7/8) in LP10T SRAM cell is 80nm/120nm/120nm/160nm respectively in 32nm and 100nm/150nm/200nm in 45nm technology.

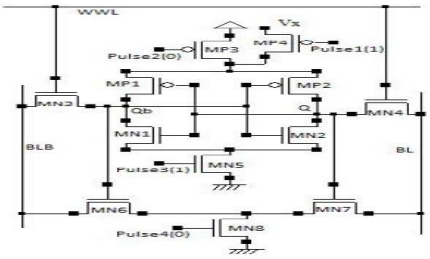

Figure 3: Low Power 10T SRAM Cell (LP10T) [2].

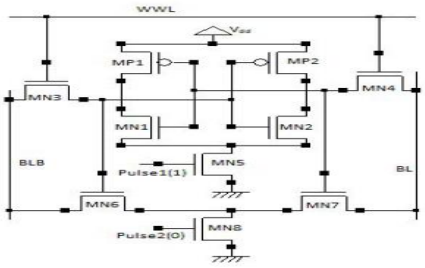

Figure 4: Low Power 12T SRAM Cell (LP12T).

And the size W of (W5/6/7/8) in LP10T SRAM cell is 80nm/120nm/120nm/160nm respectively in 32nm and 100nm/150nm/200nm in 45nm technology. The minimum length of all transistors in LP10T SRAM cell is kept to 80nm &100nm in 32nm &45nm technology respectively. In the new analyzed circuit the (12T SRAM cell) two extra transistors are used which have width equal to 80nm in 32nm technology and 100nm in 45nm technology. Thus, 10T portion of all the cell have $\beta ratio=1.33 and \gamma ratio=0.67$ where $\beta ratio=\beta drive/\beta access$ and γ ratio=βpull-down/βaccess. Typically, βratio of 1.2-3 is required to avoid read upset in conventional 6T SRAM cell [10]. The write-ability of the SRAM cell is determined by the pull-up ratio (PR) or γ ratio. Generally, $\gamma ratio \leq 1.8$ is required to maintain good write-ability [11]. The circuit diagram of LP10T and LP12T SRAM cell is depicted to Figure 3 and 4.

V. SIMULATION AND ANALYSIS

The circuit analysed in this paper is simulated by using BSIM4, 45nm and 32nm technology. For the testing of power dissipation comparison and environment, circuits have been simulated on the same input patterns. The Wave form and lay out analysis of LP10T & LP12T SRAM Cell is Indicated in Figure 4 and Figure 5, Figure 6 in 45nm and 32nm technology respectively

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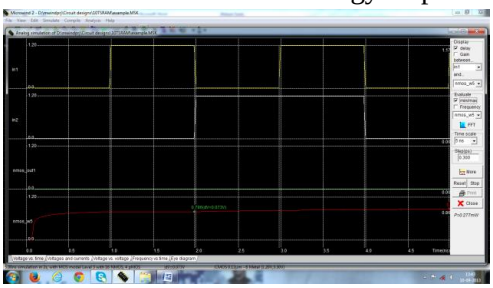

Figure 4: Waveform analysis of low power 10T Sram

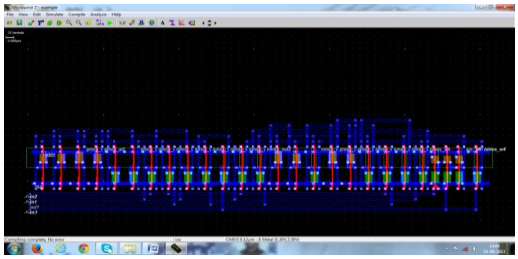

Figure 5: Layout diagram of LP10 T Sram cell

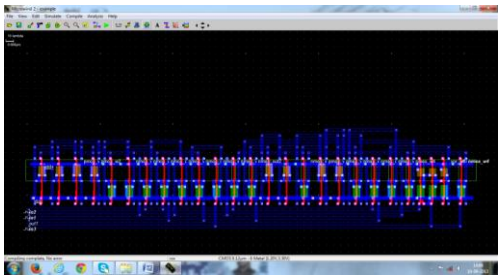

Figure 6: Layout diagram of LP12 T Sram cell

The comparison of various parameters like SNM, leakage power read margin and write margin tabulated in TABLE I, TABLEII, TABLEIII With respect to conventional SRAM Cells

TABLE I. Simulation Results with aging effect at threshold voltage 0.2v for stand-by noise margin (snm)

YEAR	***Write Margin(V)***			
	SRAM CELL			
	6T	10T	LP10T	12T
0	0.29511	0.10883	0.10829	0.10780
1/8	0.29472	0.10878	0.10825	0.10780
1/4	0.29465	0.10878	0.10824	0.10779
1/2	0.29419	0.10872	0.10818	0.10776
1	0.29403	0.10870	0.10816	0.10775
2	0.29384	0.10868	0.10814	0.10774
4	0.29361	0.10865	0.10811	0.10772
6	0.29346	0.10863	0.10809	0.10771
8	0.29335	0.10862	0.10808	0.10770
10	0.29326	0.10861	0.10806	0.10769

TABLE II. Supply voltage adjustment of sram cells for same snm =115x10^{-3}v

	With-out Aging for V_{TH}=0.2 V at 100°C			
CELL	Supply Voltage (v)	Leakage Power (nW)	Acess Time (nsec)	Write Margin (v)
6T	32.3	2.13	1.93	1.87
8T	32.3	2.13	1.92	1.83
LP10T	32.3	2.13	1.92	1.83
12T	32.3	2.13	1.92	1.83

TABLE III. Lation results with aging effect at threshold voltage 0.2v for leakage power

YEAR	***Leakage power(nW)***			
	SRAM CELL			
	6T	10T	LP10T	12T
0	32.3	2.13	1.93	1.87
1/8	32.3	2.13	1.92	1.83
1/4	32.3	2.13	1.92	1.83
1/2	32.3	2.13	1.92	1.83
1	32.3	2.13	1.91	1.83
2	32.3	2.13	1.91	1.83
3	32.3	2.13	1.91	1.83
4	32.3	2.13	1.91	1.83
6	32.3	2.13	1.91	1.83
8	32.3	2.13	1.9	1.83
10	32.3	2.13	1.3	1.83

VI. CONCLUSION

Storage devices have now reached critical performance in different applications and need to commensurate with lower supply voltage, less than 1V. At this lower operating voltage aging effects is severe and new memory circuits are potential substitution that can eliminate quiescent power loss, allowing devices to operate in lower dynamic mode. New approach is likely towards lower dynamic power and this proposed result is beneficial to observe the impact of aging of all four SRAM designs. Since LP12 T and LP10T have negligible SNM degradation and reliability compared with 6T cell, we recommend designing memory arrays by LP12T SRAM.

And also analyzes the impact of PVT variations on read/write delay and standby power. The functional results represent significant improvement in most of the design metrics over standard 6T, 10T, and LP10T SRAM cells, demonstrating its robustness and low-power operability. So that this design an attractive choice for low-power applications in scaled technology in the presence of PVT variations

REFERENCES

[1]: Martin Margala, “Low power-SRAM circuit Design,” IEEE, issue 1999.

[2]: A Islam and M. Hasan, “Leakage characterization of10TSRAMcell,”IEEEtransactiononelectrondevices, Vol.59, No.3, March2012.

[3]:Zhiyu liu and Volkan Kursun, “Characterization of a novel nine- transistor SRAM cell,” IEEE transaction on VLSI system, Volume16, NO.4, APRIL2008.

[4]:MonikaYadav,Shyam Akashe,Dr.Yogesh Goswami, "AnalysisofleakageReductionTechniqueon Different SRAMcell,"International journal of Engineer Trends and Technology, Volume2 , Issue3-2011.
[5]: Geetika Srivastava &R.K.Chauhan "Deasign of a new 10T SRAM cell for leakage reduction & stability enhancement" IEEE,VOLUME 3,Number 39 (2010) pp.225-230.
[6]: Geetika Srivastava &R.K. Chauhan "Effect of technology scale down on power reduction stretegies" ISBN-978-1-4577-0694-3 PN-717, IEEE Explorer, and conference proceeding May 2012.
[7]: R. Vattikonda, W. Wang, Y. K. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," *Design Automation Conference, 2006 43rd ACM/IEEE* , vol., no., pp.1047-1052.
[8]: A. Kerber, E. Cartier, "Reliability Challenges for CMOS Technology Qualifications With Hafnium Oxide/Titanium Nitride Gate Stacks," *IEEE Trans. Device Mater Rel.*, vol. 9, no. 2, pp. 147-162, Jun 2009.
[9]: Sanjay Kr Singh, Sampath Kumar, Arti Noor, D. S. Chauhan & B.K.Kaushik, "Deep Sub-Micron SRAM Design for DRV Analysis and Low Leakage", International Journal of Advances in Engineering & Technology, Vol. 1, Issue 5, pp. 429-436 , Nov 2011.
[10]. Seevinck, F. J. List, J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE J. Solid-State Circuits,* vol. SC-22, pp. 748-754, Oct. 1987.
[11]: Shyam Akashe1, Ankit Srivastava2, Sanjay Sharma, "Calculation of Power Consumption in 7 Transistor SRAM Cell using Cadence Tool", International Journal of Advances in Engineering & Technology, Vol. 1, Issue 4, pp. 189-194, Sept 2011.
[12]. L. C Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. IEEE Symp. on VLSI Technology Dig. of Tech. Papers.* pp. 128- 129, June 2005.

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