ELECTRICAL AND THERMAL CHARACTERIZATION OF MULTILAYER STRUCTURE DEVICES FOR FAST PC IMPLEMENTATION

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ABSTRACT

In this paper we review an analytical electrothermal model, already proposed by us, able to calculate the temperature and current distribution for any integrated device, whose structure can be represented as an arbitrary number of superimposed layers with a 2-D embedded thermal source, so as to include the effect of the package. The model allows to optimize the device layout through the solution of the non-linear 3-D heat equation. The thermal solution is achieved by the Kirchhoff transform and the 2-D Fourier transform. Moreover the model is independent on the specific physical properties of the layers, hence GaAs FETs, HBT and HEMTs can be analysed. The model has been applied to characterize the electrical and thermal performances of a multifinger GaAs FET and of a Si/SiGe Heterojunction Bipolar Transistor.

KEYWORDS: *Modelling, Electrical and Thermal Effects, Self Heating Modelling, SiGe, GaAs, RF Devices, FETs, Heterojunction Bipolar Transistors.*

I. INTRODUCTION

The general evolution of electronic devices for high frequency applications emphasizes the growing importance of the thermal problem during the design process, where analytical models for the temperature evaluation are useful tools to calculate the optimal set of geometrical parameters that minimise the device thermal phenomena.

Particularly in GaAs technology, one of the main problems to overcome is the low thermal conductivity of the semiconductor, which focuses the designer interest on the thermal optimization when good reliability has to be achieved. Nevertheless, if on one hand a great effort on the package thermal analysis and optimisation can be recognised, there is a lack of physical-based analytical electrothermal models at the device level.

The analytical electrothermal modelling of electronic devices is such a difficult problem to deal with that the analytical models that have been proposed until now are either over-simplified or rather inefficient from a computational point of view. The reason for that lies in the complex structure of an integrated device and in the non-linear thermal properties of the materials.

However, only a physical-based analytical model can give the proper physical insight in order to understand the connections between a number of geometrical and technological parameters and the device electrothermal performance. Unfortunately, an analytical model suffers the unavoidable simplifying hypothesis by which the numerical calculation can be carried out. In spite of that, the analytical model for the temperature evaluation is a useful tool during the design process to calculate the optimal set of geometrical parameters that minimise the thermal phenomena in an integrated device. Furthermore, in case of multifinger devices or thermal coupling between contiguous devices, the inaccuracy introduced by the ipothesis of uniform channel temperature can be relevant.

In this paper we review an analytical model, already proposed by us [1-5], for the solution of the 3-D steady-state heat equation with temperature-dependent thermal conductivity for a single integrated device or a given configuration of two or more devices. A weak coupling between electrical and thermal solution is implemented by calculating the device current and, hence, the dissipated power, as a function of the actual channel temperature. A multiple layer structure approximating the effect of the package has been considered as the spatial domain in which the heat equation has been solved.
The calculation time for the proposed examples has been quantified in a few minutes for the main part of the algorithm, and in less than a minute for the graphic routines, making the method suitable for a fast PC implementation.
The paper is organized in the following way: Section 2 outlines a brief review of the proposed mathematical model, whereas in Section 3 two examples of application to a GaAs FET and to a power Si/SiGe HBT are shown and the numerical results of the simulations are discussed. Finally the conclusions are illustrated in Section 4.

II. A REVIEW OF OUR ELECTROTHERMAL MODEL

The aims of our model are:

- to solve analitically the non-linear 3-D steady-state heat equation
- to take into account the dependence on temperature of the thermal conductivity
- to take into account the interaction between two neighbouring devices
- to implement the coupling between the electrical and thermal behaviour of the device to determine the actual channel temperature
- to take into account the presence of the package
- to develop a full general model useful to simulate any multilayer electronic and optoelectronic device
- fastness and accuracy
- to implement it on a Personal Computer.

The Fig. 1 shows the cross section of a typical electron device including coating, die attachment, mounting and heat sink.

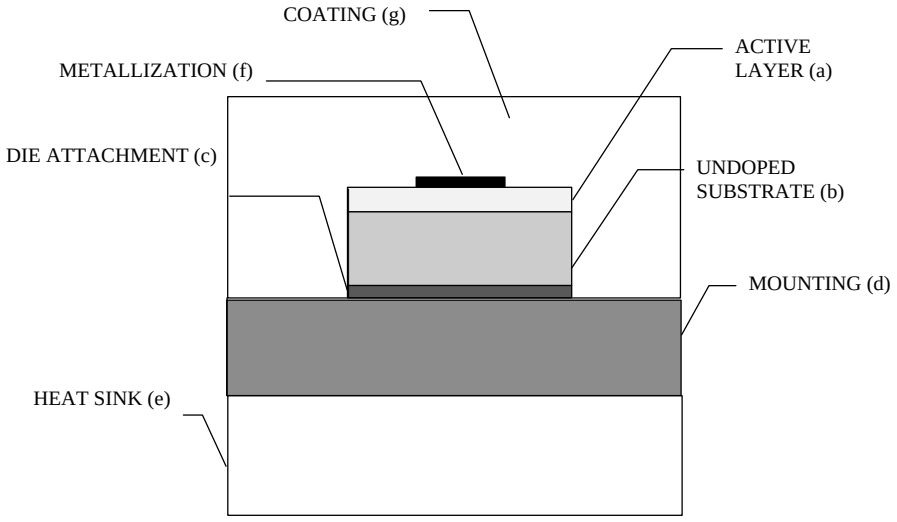

Figure 1. Typical electron device including coating, die attachment, mounting and heat sink.

In particular, the problem of the heat generation and conduction has been solved with reference to a structure, which is composed of *m* layers, and approximates a typical device with the die mounted on a substrate and covered with a cap layer.
For this structure, to determine the temperature distribution, the following non-linear steady-state heat equation has to be solved [1]:

$$\overline{\nabla}\cdot\left[k_{TH}(T)\overline{\nabla}T(x,y,z)\right]=-Q_V(x,y,z) \tag{1}$$

where $T(x,y,z)$ is the temperature field, k_{TH} is the temperature-dependent thermal conductivity and $Q_V(x,y,z)$ is the dissipated power density.
The basic assumptions of the model are:

1. the device and package structures can be represented as a set of superimposed homogeneous layers;
2. the thickness of each layer is constant;
3. the extension of the layers in the x and y directions is infinite;
4. the contact thermal resistance is neglected;
5. the thermal source is modeled as a 2-D geometrical shape $Q_S(x,y)$, located at the interface between two contiguous layers, say the k-th and the (k+1)-th.;
6. the device self-heating is due to the Joule heating and other contributions are neglected.

Eqn. (1) can be solved considering the following expression:

$$\overline{\nabla}\cdot\left[k_{TH}(T)\overline{\nabla}T(x,y,z)\right]=0 \tag{2}$$

and accounting for the heat source in the Boundary Conditions (BCs).
Dirichlet and Neumann BCs can be expressed as:

$$T_i(x,y,z)=T_{i+1}(x,y,z)\quad i=1...m-1 \tag{3a}$$

$$k_{TH1}(T_1)\frac{\partial T_1(x,y,z)}{\partial z}=0 \tag{3b}$$

$$T_m(x,y,z)=T_\infty \tag{3c}$$

$$k_{THi}(T_i)\frac{\partial T_i(x,y,z)}{\partial z}=k_{THi+1}(T_{i+1})\frac{\partial T_{i+1}(x,y,z)}{\partial z} \tag{3d}$$

$$k_{THk}(T_k)\frac{\partial Tk(x,y,z)}{\partial z}=k_{THk+1}(T_{k+1})\frac{\partial T_{k+1}(x,y,z)}{\partial z}=Q_S(x,y) \tag{3e}$$

Eqn. (3b) and (3c) refer to an adiabatic top surface and to an isothermal bottom surface with reference room temperature T_∞ respectively, whereas Eqn. (3e) refers to the interface containing the heat source. Eqns. (3a) and (3d) impose the temperature and heat flux continuity across the interfaces.
In order to linearize Eqn. (2), the Kirchhoff transformation can be applied to each layer in the following form:

$$\theta_i(x,y,z)=\frac{1}{k_{Ri}}\int_{T_\infty}^{T_i(x,y,z)}k_{THi}(\tau)d\tau\quad i=1...m \tag{4}$$

In Eqn. (4) $\theta_i(x,y,z)$ is the transformed temperature or the so-called "pseudo-temperature" of the i-th layer, $T_i(x,y,z)$ is the actual temperature, k_{Ri} is the temperature-dependent thermal conductivity $k_{THi}(T)$ evaluated at $T = T_\infty$.
Hence, Eqn. (2) is transformed into the well-known Laplace equation:

$$\nabla^2\theta_i(x,y,z)=0 \tag{5}$$

Unfortunately, applying the Kirchhoff transformation to Eqns. (3a) ÷ (3e), the non-linearity of the

problem equation is shifted to the boundary conditions. Thus, if a first order Taylor expansion for the inverse transform is considered, i.e. $T \approx \theta + T_\infty$, the resulting problem is linear in each layer.
Furthermore, to simplify the mathematical steps, the 2-D Fourier transform can be applied to Eqn. (5) in the following form:

$$\Psi_i(\alpha,\beta,z) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} \theta_i(x,y,z) e^{-j\alpha x} e^{-j\beta y} dxdy$$

This leads to the one-dimensional ordinary differential equation:

$$\frac{d^2\Psi_i}{dz^2} - (\alpha^2 + \beta^2)\Psi_i = 0 \tag{6}$$

with the following solution in each *i*-th layer:

$$\Psi_i(\alpha,\beta,z) = C_i' e^{-\gamma z} + C_i'' e^{\gamma z} \tag{7}$$

and with the transformed BCs:

$$\Psi_i(\alpha,\beta,z_{i+1}) = \Psi_{i+1}(\alpha,\beta,z_{i+1}) \tag{8a}$$

$$k_{R1}\frac{d\Psi_1(\alpha,\beta,z_1)}{dz} = 0 \tag{8b}$$

$$\Psi_m(\alpha,\beta,z_m) = 0 \tag{8c}$$

$$k_{Ri}\frac{d\Psi_i(\alpha,\beta,z_{i+1})}{dz} = k_{Ri+1}\frac{d\Psi_{i+1}(\alpha,\beta,z_{i+1})}{dz} \tag{8d}$$

$$k_{Rk}\frac{d\Psi_k(\alpha,\beta,z_{k+1})}{dz} - k_{Rk+1}\frac{d\Psi_{k+1}(\alpha,\beta,z_{k+1})}{dz} = \Im_{\alpha\beta}\left(Q_s(x,y)\right) \tag{8e}$$

In Eqn. (8e), the right-hand side is the Fourier transform of the 2-D heat source, which can be easily calculated once the geometrical shape has suitably been described. The heat source can be modeled as a rectangle located at the active layer-to-substrate interface but, to account for the non-uniform power dissipation, it is more convenient to approximate the 2-D shape as a set of elementary point sources. In order to link the power dissipation to the device current, each point source has been associated with a part of the device dissipation region assuming that the whole current can be expressed as the sum of contributions, corresponding to elementary devices. In this way the original problem results split in elementary problems in which a unit hot spot is associated with a unit device. Since the problem (6) with the BCs (8a) – (8e) is linear, it is possible to solve the elementary problem and then reconstructing the overall solution by applying the superposition of effects.
The right-hand side of (8e) for a point heat source is:

$$\Im_{\alpha\beta}\left(Q_s(x,y)\right) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} Q_0\delta(x-a)\delta(y-b)e^{-j\alpha x}e^{-j\beta y}dxdy = Q_0$$

where $\delta(x-x_0)$ is the Dirac function centered in x_0 and Q_0 is the power dissipated by the unit device. The electrothermal feedback can be implemented by evaluating the current of each elementary device at the actual channel temperature, which is approximated with the hot spot temperature.
The solution to (6) can be calculated by substituting (7) into (8a) - (8e), which leads to the linear

system:

$$M(\gamma)C(\alpha,\beta) = U(\alpha,\beta) \tag{9}$$

where $\gamma^2 = \alpha^2 + \beta^2$, $M(\gamma)$ is the $2m \times 2m$ coefficient matrix, C is the integration constants vector containing the unknowns C_1', C_1'', .., C_m', C_m'' and U is the column vector containing the Fourier transform of the heat source and having only the $(k+1)$-th non-zero entry. It has to be remarked that M is a function of γ and not of α and β separately, while this is not generally true for C and U but results in the case of point heat source.

Unfortunately, the solution to Eqn. (9) is not a trivial problem since $M(\gamma)$ is not a numeric matrix but contains the Fourier frequencies α and β as parameters. It could be possible to give a closed-form expression of (7) after solving (9) by applying the Cramer rule and substituting C_1', C_1'', .., C_m', C_m'' into (7), but just for a limited number of layers, e.g. five. However, it would be a very tedious and almost impossible operation to carry out for a large number of layers. Furthermore, Eqn. (7) has to be back-transformed involving a double integration in a large domain of a very complicated expression.

In this work the Discrete Fourier Transform (DFT) has been applied in order to show that the linear system (9) can be solved for any m and the simultaneous solution of the pseudo-temperature θ_i of all layers can be obtained.

The proposed technique consists of sampling Eqn. (9) i.e.:

$$\forall \alpha = \alpha_p, \beta = \beta_q \Rightarrow M(\gamma_{pq})C(\alpha_p,\beta_q) = U(\alpha_p,\beta_q) \tag{10}$$

which can be easily solved since it is a numeric system:

$$C(\alpha_p,\beta_q) = M^{-1}(\gamma_{pq})U(\alpha_p,\beta_q) \tag{11}$$

Thus, after substituting (11) into (7), the samples of the 2-D Fourier transform are:

$$\Psi_i(\alpha_p,\beta_q,z) = C_i'(\alpha_p,\beta_q)e^{-\gamma_{pq}z} + C_i''(\alpha_p,\beta_q)e^{\gamma_{pq}z} \tag{12}$$

where the index i refers to the i-th layer.

In order to perform the 2-D inverse DFT, which is a computationally advantageous approach, it is useful to evaluate (12) on specific surfaces, e.g. on the interfaces between contiguous layers, so as to obtain samples of the 2-D function $\theta_i(x,y,z_i)$. It can be easily shown that if the point thermal source is normalized to unit, Eqn. (9) can be solved just once and the inverse transform of (12), referred to the $(k+1)$-th, represents the normalized unit thermal profile on the source surface. It can be used to calculate the whole thermal field by multiplying it by the dissipated power of a specific elementary device and by shifting the resulting function to the device location. Updating the elementary dissipated powers and solving iteratively, the device current results consistent with the actual channel temperature.

The proposed method allows its application to a wide variety of integrated devices, provided they are described for the electric part with the appropriate I-V characteristics and its structure can be reasonably represented as set of superimposed layers.

III. NUMERICAL RESULTS AND DISCUSSION

At first the proposed model has been applied to a seven-layer structure, described in Tab. 1, with temperature-dependent thermal conductivity.

The source is supposed to be located at the interface between active and undoped layers of a multifinger GaAs FET with the following geometrical features: gate length L = 1 μm, unit gate width W_u = 100 μm, number of gate n = 5, doping density $N_D = 6.5 \cdot 10^{22}$ m^{-3}, active layer thickness a = 0.34 μm, gate-to-gate spacing S = 40 μm, source-to-gate and gate-to-drain spacing L_{cg} =1 μm.

A one-dimensional I-V FET equation [5] has been implemented to consider the feedback between the device current and the active layer temperature distribution. The most widely accepted empiric relations between FET physical parameters and temperature have also been taken into account [1].

Table 1. Physical and geometrical parameters of the considered GaAs multilayer structure.

Layer	Material	Thickness [μm]	Thermal conductivity $k_{TH}(T)$ [W/m/K]	Reference k_{TH0} [W/m/K]
Cap layer	Epoxy mold compound	500	0.4	0.4
Metallization	Gold	3	$-0.065 \cdot T + 336.67$	317
Active layer	n-doped GaAs	0.34	$52720 / T^{1.2}$	56.16
Bulk	undoped GaAs	100	$54400 / T^{1.2}$	57.95
Die-attachment	Epoxy mold compound	25	4	4
Mounting	Alumina	500	$-0.0976 \cdot T + 36.26$	36
Heat spreader	Copper	1000	$-0.075 \cdot T + 423.33$	401

In Fig. 2 the cross section of the overall thermal profile for the given device is shown. In this case the dissipated power is P = 1.18 W. The solid line refers to the temperature profile along the y-axis after the Kirchhoff transform whereas the dash-dotted line refers to the same profile before the transformation.

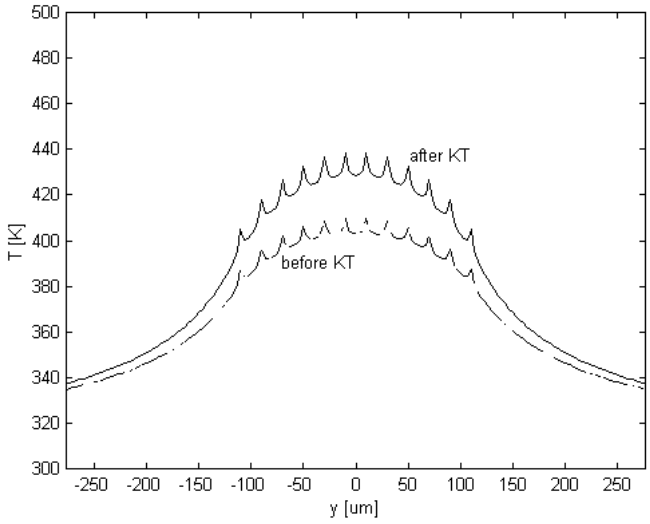

Figure 2. Cross section of the thermal profile on the source surface along the y direction: comparison between the results after the Kirchoff transform (solid line) and before the transformation (dash-dotted line).

As one can clearly see, the difference becomes relevant in the device area, which confirms that the non-linear dependence of the GaAs thermal conductivity cannot be neglected. Furthermore, as the peak temperature rises above the reference temperature (300 K) is about 140 K and the mean temperature rises in the active area is about 110 K, the linear approximation of the boundary condition leads to a 6% error, which is acceptable.

In order to study the influence of geometrical parameters of the device on its thermal performance, we have evaluated the thermal resistance R_{TH} of the device and the peak channel temperature T_p versus S, L and n, for a dissipated power P = 1 W, as shown in Figs. 3 (where n = 14), 4 (where L = 1 μm) and 5 (where L = 1 μm) respectively.

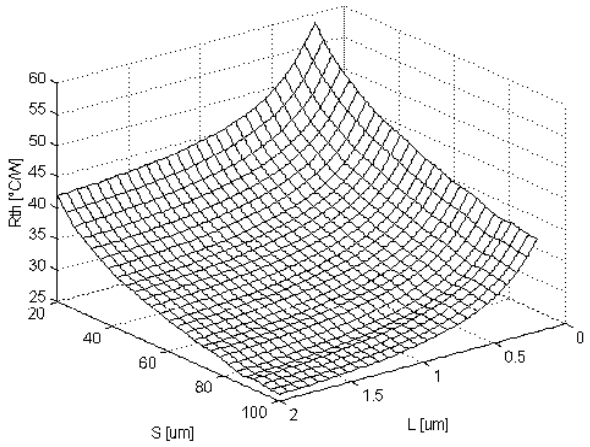

Figure 3. R_{TH} versus L and S.

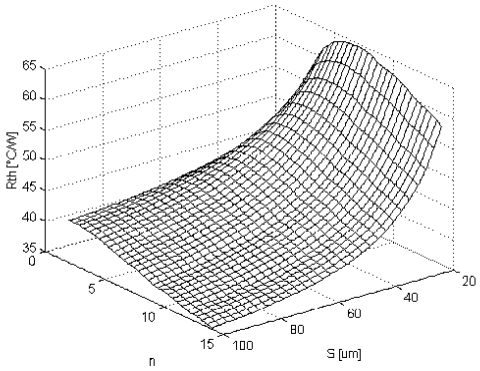

Figure 4. R_{TH} versus n and S.

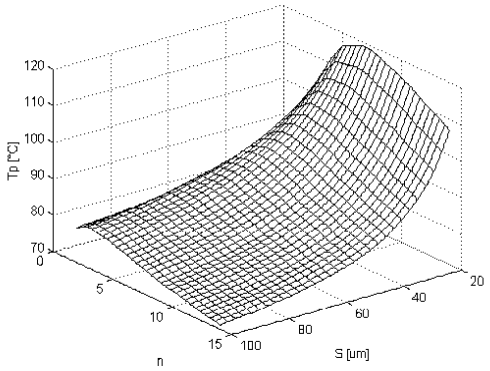

Figure 5. T_P versus n and S.

Moreover in Fig. 6 the peak channel temperature versus drain-to-source voltage is shown for a set of gate voltages. The self-heating effect becomes not negligible as the dissipated power increases, i.e. in saturation condition. The dependence of T_p on V_{DS} results to be quadratic in the considered voltage range.

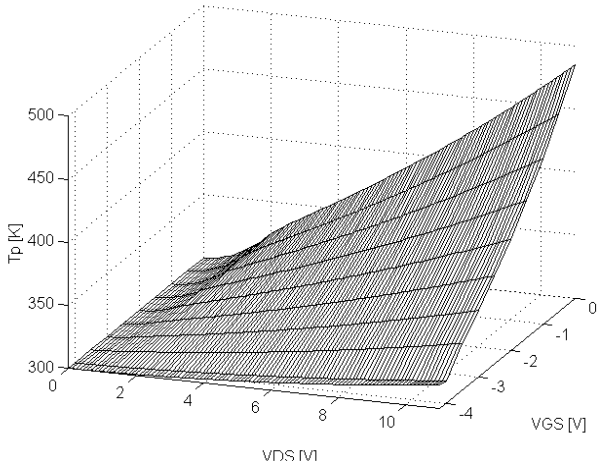

Figure 6. Peak channel temperature T_p versus drain-source voltage V_{DS} for a set of gate voltages V_{GS}.

These figures allow the designer to determine the parameter values which optimize the thermal and electrical layout.
Moreover, in order to demonstrate that the proposed method is independent on the specific physical properties of the layers, we have applied it to a typical Si/SiGe HBT structure [1], in which we have used the name Si/SiGe HBT for a device with Si as the base material and SiGe as the emitter.
In particular we have represented the device as a surface without any thickness, where X and Y are the dimensions of the periodic cell, in which we have divided the device.
The overall heat source, which is located in the depletion layer at the collector, has been divided into a set of elementary point sources located in the middle of each elementary $X \times Y$ periodic cell.
The first step is to solve the electro-thermal problem, assuming the heat generation and the current as mutually dependent for each single elementary device which is related to a single elementary heat source; finally the resulting thermal field of the whole structure is obtained by the superposition of all the elementary fields.
The transformed temperature $\theta_i(x,y,z)$ for a point thermal source can be expressed as [9]:

$$\Delta\theta(x,y,z) = \frac{Q(x_{0i}, y_{0i}, z_{0i})}{2\pi\pi_0\sqrt{(x-x_{0i})^2 + (y-y_{0i})^2 + (z-z_{0i})^2}} \tag{13}$$

where x_{0i}, y_{0i} and z_{0i} are the coordinates of the *i-th* heat point source, x,y,z is the generic position in which the temperature increase $\Delta\theta(x,y,z)$ above the reference is evaluated and $Q(x_{0i},y_{0i},z_{0i})$ is the dissipated power of the *i-th* elementary heat source.
The electro-thermal feedback can be implemented for each $X \times Y$ subsection considering that Q can be assumed as the temperature-dependent electrical power $P(\theta_i(x_{0i},y_{0i},z_{0i}))$ of the *i-th* elementary device centred in x_{0i}, y_{0i}, z_{0i} and, thus, corresponding to the *i-th* heat source centred in the same point.
The electrical power of the *i-th* elementary device is:

$$P(x_{0i},y_{0i},z_{0i}) = P(\theta_i) = I_B(\theta_i)\, V_{BE} + I_C(\theta_i)\, V_{CE} \tag{14}$$

where V_{BE}, the voltage drop between base and emitter, is temperature-independent, I_B and I_C are the base and collector currents, respectively, of the elementary cell centred in x_{0i},y_{0i},z_{0i} having temperature θ_i, and V_{CE}, the voltage drop between collector and emitter, is temperature-independent.
The dependence of the current-voltage equation, based on physical parameters, on the temperature was widely studied in the past. The parameters that have been taken into account for their thermal dependence are the electron mobility, saturation velocity, permittivity, energy band gap, threshold voltage and built-in voltage. The reader can refer to for the empirical expression of the foregoing parameters [9].
We have considered a HBT structure having X= 0.25 μm and Y= 30 μm for the emitter and X= 50 μm and Y= 300 μm for the collector.
In Fig. 7 we have reported the I_C-V_{CE} characteristics at room temperature T = 300 K, for a base current varying from 1 mA to 3 mA.
The obtained heat generated at the base-collector junction, by Eq. (14), has been equal to 0.0702 W.
Now it has been possible determined the temperature increase due to self heating effect.
Fig. 8 shows the simulated average temperature T_m at the BE junction versus time, in the time range $10^{-8} \div 10^{-3}$ s.
In the interval $10^{-6} \div 10^{-5}$ s, it clearly appears that the temperature increases more rapidly, tending to a saturation value equal to 7.85 K.

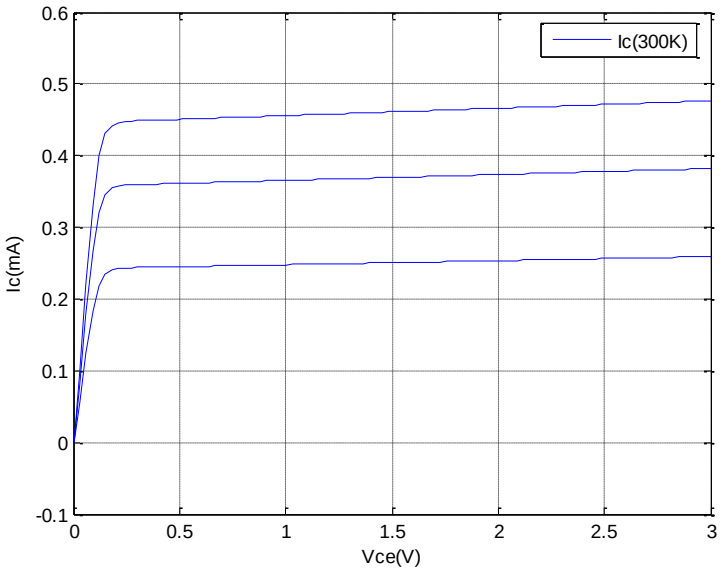

Figure 7. Simulated I_C-V_{CE} characteristics at T=300 K for a base current varying from 1 mA to 3 mA.

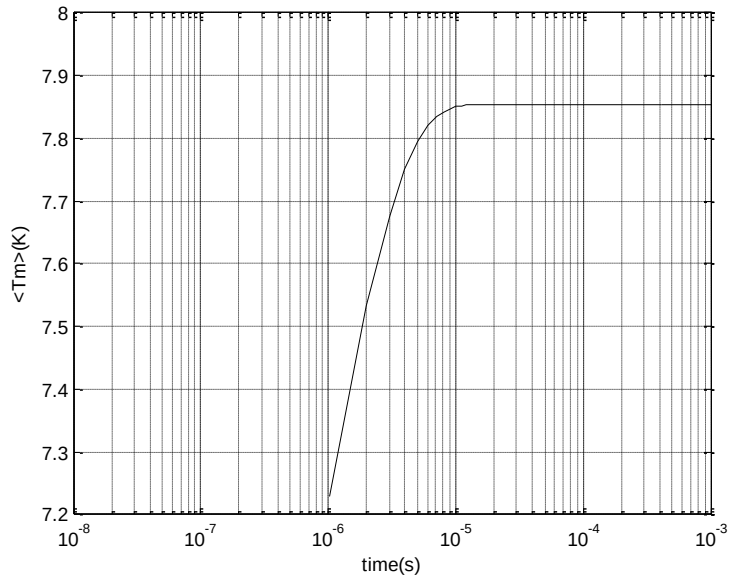

Figure 8. Simulated average temperature T_m at BE junction versus time for Si/SiGe HBT.

The electro-thermal feedback is shown in Fig. 9, in which we have reported the simulated output I-V characteristics both at 300 K (blue lines) and at 307.85 K (red lines). This figure shows the well-known degradation effect on I-V curves due to temperature increase.

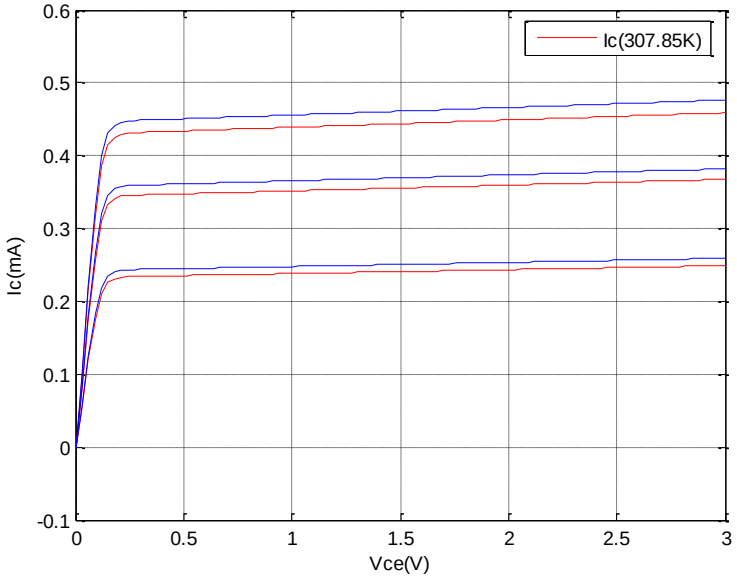

Figure 9. Simulated I-V characteristics both at 300 K (blue lines) and at 307.85 K (red lines).

We have considered a Si/SiGe HBT, whose structure is the same of the previous one, except for the dimension X of the emitter, equal, in this case, to 2.5 μm.
Fig. 10 shows the simulated average temperature T_m at the BE junction versus time. For this device the saturation value of T_m is 4.55 K and this result allows to say that the self heating is in inverse proportion to the emitter area. Moreover, as shown in Fig. 11, in which we have reported the simulated I-V curves both at 300 K (blue lines) and at 304.55 K (red lines), the device feels more the effects of temperature increase at high base currents, with a resulting decrease of device efficiency.

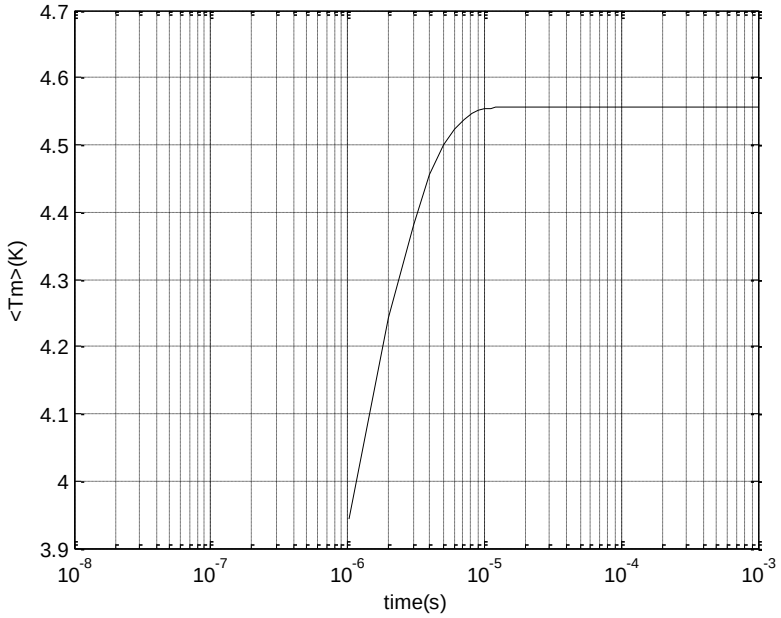

Figure 10. Simulated average temperature T_m at BE junction versus time (X=2.5 μm for the emitter).

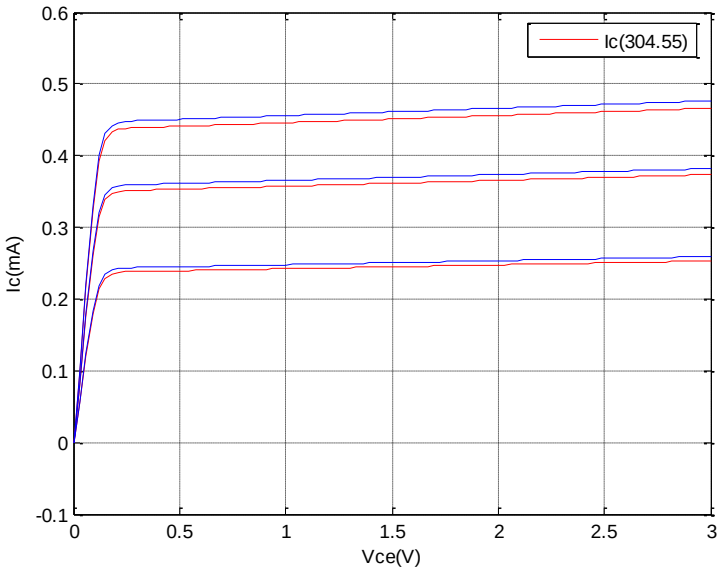

Figure 11. Simulated I-V characteristics both at 300 K (blue lines) and at 304.55 K (red lines).

Finally, in order to demonstrate the applicability of our method in case of multifinger devices or thermal coupling between contiguous devices, our model has been applied to a power Si/SiGe Heterojunction Bipolar Transistor with multiple emitter fingers [6-8], as shown in Fig. 12.

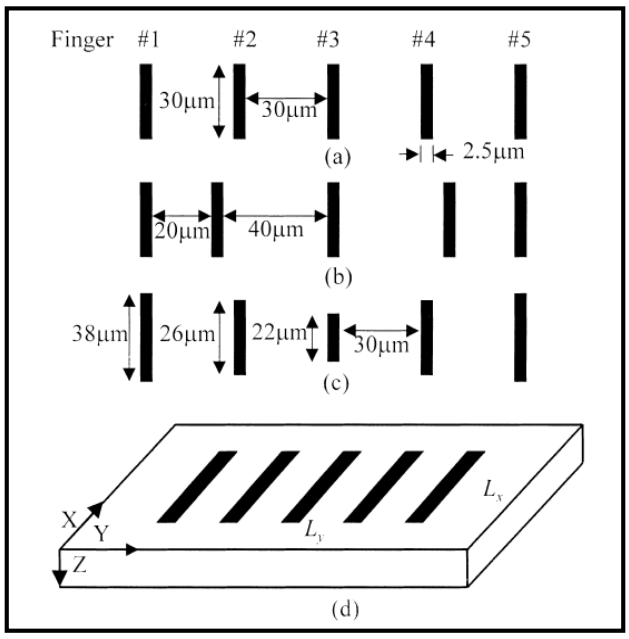

Figure 12. Possible structures of a power Si/SiGe Heterojunction Bipolar Transistor with multiple emitter fingers.

In this case, from the analysis of the various thermal profiles, it has been possible to define the electrothermal optimal layout of the considered HBT with three fingers having area 20 μm x 3 μm, spaced of 35 μm. Fig. 13 shows the relative thermal profile in the (*x*,*y*) plane, while in Fig. 14 we have reported the 3-D thermal field on the surface containing the heat source.

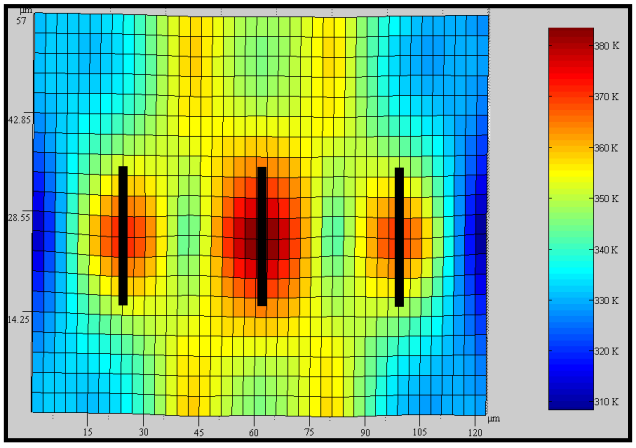

Figure 13. Thermal profile in the (*x*,*y*) plane for the power Si/SiGe HBT having optimal layout.

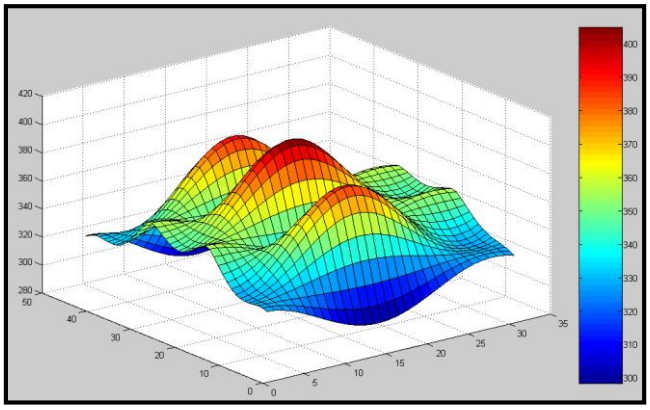

Figure 14. 3-D thermal field on the surface containing the heat source.

The calculation time for the proposed examples can be quantified in a few minutes for the main part of the algorithm, that is the temperature field of the elementary source and the current of the elementary device, and in less than a minute for the graphic routines. To perform all the simulations we have used a common Windows-based PC, equipped with a Pentium IV CPU and main memory of 1 Gbyte.

It is worthwhile to remark that the software, by which all the calculations have been carried out, has been implemented just for academic non-commercial purpose.

IV. CONCLUSIONS

In this paper we review an analytical model, already proposed by us, for the solution of the 3-D steady-state heat equation with temperature-dependent thermal conductivity for a single integrated device or a given configuration of two or more devices. A weak coupling between electrical and thermal solution is implemented by calculating the device current and, hence, the dissipated power, as a function of the actual channel temperature. A multiple layer structure approximating the effect of the package has been considered as the spatial domain in which the heat equation has been solved.

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