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# ANALOG INTEGRATED CIRCUIT DESIGN AND TESTING USING THE FIELD PROGRAMMABLE ANALOG ARRAY TECHNOLOGY

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## *ABSTRACT*

*Due to their reliability, performance and rapid prototyping, programmable logic devices overcome the use of ASICs in the digital system design. However, the similar solution for analog signals was not so easy to find. But the evolutionary trend in Very Large Scale Integrated (VLSI) circuits technologies fuelled by fierce industrial competition to reduce integrated circuits (ICs) cost and time to market has led to design the Field-Programmable Analog Array (FPAA) which is the analog equivalent of the Field Programmable Gate Array (FPGA). In fact, the use of FPAAs reduces the complexity of analog design, decreases the time to market and allows products to be easily updated and improved outside the manufacturing environment. Thus, the reconfigurable feature of FPAAs enables real time updating of analog functions within the system using the Configurable Analog Blocks (CABs) system and appropriate software. In this paper, an interesting analog phase shift detection circuit based on FPAA architecture is presented. In fact, the phase shift detection circuit will distinguish a faulty circuit from a faulty-free one by controlling the phase shift between their corresponding outputs. The system is practically designed and simulated by using the AN221E04 board which is an Anadigm product. The Circuit validation was carried out using the AnadigmDesigner®2 software.*

## *KEYWORDS*

Analog integrated circuits, design, FPAA, test, phase shift detection circuit

## I. INTRODUCTION

With the continuous increase of integration densities and complexities, the tedious and hard process of designing and implementing analog integrated circuits could often take weeks or even months [1]. Consequently, analog and mixed semiconductor designers have begun to move design methodologies to higher levels of abstraction in order to reduce the analog design complexity [2]. Also, the use of programmable circuits further facilitates the task of designing complex analog ICs and offers other advantages. In fact the use of field programmable devices decreases the time to market and allows the possibility of updating the considered circuit design outside of the manufacturing environment. Thus, field programmable devices can be programmed and reprogrammed not only to update a design but to offer the possibility of error correction [1-2].

**"**In the digital domain, programmable logic devices (PLDs) have a large impact on the development of custom digital chips by enabling the designer to try custom designs on easily-reconfigurable hardware. Since their conception in the late 1960s, PLDs have evolved into today's high-density FPGAs. In addition, most of the digital processing is currently done through FPGA circuits" [1]. However, reconfigurable analog hardware has been progressing much more slowly. In fact, the field programmable analog array technology appeared in 1980's [3-4]. The commercial FPAA did not reach the market until 1996 [1]. And the Anadigm FPAA technology was made commercially available just in 2000 [5].

An FPAA is an integrated circuit built in Complementary Metal Oxide Semiconductor (CMOS) technology that can be programmed and reprogrammed to perform a large set of analog circuit functions. Using the AnadigmDesigner®2 software and its library of analog circuit functions, a designer can easily and rapidly design a circuit that would previously have taken months to design

and test. The circuit configuration files are downloaded into the FPAA from a PC or system controller or from an attached EEPROM [6].

Modern FPAAs like Anadigm products can contain analog to digital converters that facilitate the interfacing of analog systems with other digital circuits like DSP, FPGAs and microcontrollers [1]. FPAAs are used for research and custom analog signal processing. In fact, this technology enables the real-time software control of analog system peripherals. It is also used in intelligent sensors implementation, adaptive filtering, self-calibrating systems and ultra-low frequency analog signal conditioning [6].

The paper is organised as follows. Section 2 introduces the FPAA architecture based on switched capacitor technology. We then present The AN221E04 Anadigm board in section 3. The testing importance in CMOS analog integrated circuits and the phase shifte defenition are discussed in section 4. The proposed test methodology using the FPAA technology is presented in section 6. The simulation results are given in section 6. Finally, we conclude in section 7.

## II. THE FPAA ARCHITECTURE USING THE SWITCHED CAPACITOR TECHNOLOGY

"FPAA devices typically contain a small number of CABs (Configurable Analog Blocks). The resources of each CAB vary widely between commercial and research devices" [4-7]. In this paper, we focus on Anadigm's FPAA family based on switched capacitor technology. This technology is the technique by which an equivalent resistance can be implemented by alternatively switching the inputs of a capacitor. In fact, an effective resistance can be implemented using switched capacitors. Its value depends on the capacity but changes according to the sampling frequency **(f =1/T)**. Fig. 1 illustrates how switched capacitors are configured as resistors [5-6].

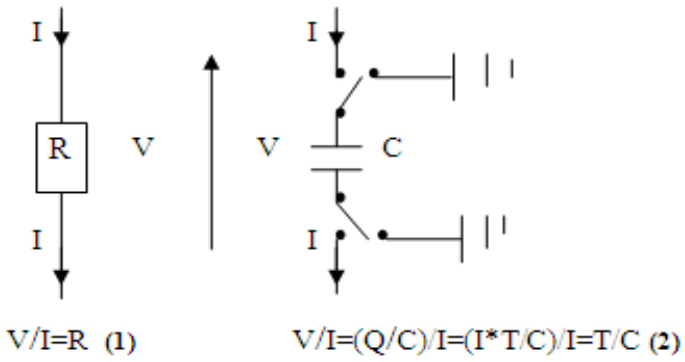


Figure 1: Switched capacitor configured as a resistor

The most important element in FPAA is the Configurable Analogue Block (CAB), which includes an operational amplifier and manipulates a network of switched capacitor technology. In the next section we present the Anadigm® AN221E04 FPAA device which is based on switched capacitor technology [6].

## III. THE AN221E04 ARCHITECTURE

The AN221E04 device consists of a 2x2 matrix of fully Configurable Analog Blocks, surrounded by programmable interconnect resources and analog input/output cells with active elements. Configuration data is stored in an on-chip SRAM configuration memory. The AN221E04 device features six input/output cells. In fact, The AN221E04 devices have four configurable I/O cells and two dedicated output cells [6]. The architectural overview of the AN221E04 device is given by Fig. 2.

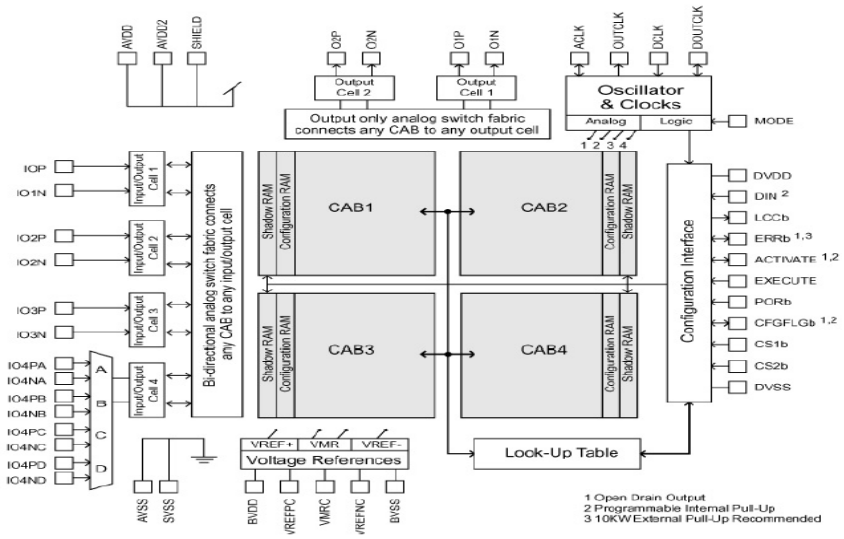


Figure 2: Architectural overview of the AN221E04 device [6]

The circuit design is enabled using AnadigmDesigner®2 software, which includes a large library of analog circuit functions such as gain, summing, filtering, etc... These circuit functions are represented as CAMs (Configurable Analog Modules) which are configurable blocks mapped onto portions of CABs. The circuit implementation is established through a serial interface on the AN221E04 evaluation board using the AnadigmDesigner®2 software, which includes a circuit simulator and a programming device. A single AN221E04 can thus be programmed and reprogrammed to implement multiple analog functions [6].

## IV. THE TESTING IMPORTANCE IN CMOS ANALOG INTEGRATED CIRCUITS

Over the past decades, Complementary Metal Oxide Semiconductor (CMOS) technology scaling has been a primary driver of the electronics industry and has provided a denser and faster integration [8-9]. The need for more performance and integration has accelerated the scaling trends in almost every device. In addition, analog and mixed integrated circuit design and testing have become a real challenge to ensure the functionality and quality of the product especially for safety-critical applications [10-11].

In fact, safety-critical systems have to function correctly even in presence of faults because they could cause injury or loss of human life if they fail or encounter errors. The automobile, aerospace, medical, nuclear and military systems are examples of extremely safety-critical applications [12]. Safety-critical applications have strict time and cost constraints, which means that not only faults have to be tolerated but also the constraints should be satisfied. Hence, efficient system design approaches with consideration of fault tolerance are required [12]. In addition, in safety-critical applications, the hardware redundancy can be tolerated to provide the required level of fault tolerance.

In fact, incorrectness in hardware systems may be described in different terms as defect, error, fault and failure. These terms are quite a bit confusing. They will be defined as follows [10-13-14-15]:

**Failure:** A failure is a situation in which a system (or part of a system) is not performing its intended function. So, we regard as failure rates when we consider that the system doesn't provide its expected system function.

**Defect:** A defect in a hardware system is the unintended difference between the implemented hardware and its intended design.

**Fault:** A representation of a defect at the abstract level is called a fault. Faults are physical or logical defects in the device design or implementation.

**Error:** A wrong output signal produced by a defective system is called an error. Error is the result of the fault and can induce the system failure.

Defining the set of test measurements is an important step in any testing strategy. This set includes all properties and test parameters which can be monitored during the test phase. In the next case study section, we consider the phase shift obtained between the fault free circuit output and the faulty one.

## The phase shift definition

Two sinusoidal waveforms having the same amplitude and the same frequency (**f=1/T**) are said in "in phase" if they are superimposed. Otherwise, if the two waves are of the same amplitude and frequency but they are out of step with each other they are said dephased. In technical terms, this is called a phase shift [16]. The phase shift of a sinusoidal waveform is the angle **φ** in degrees or radians that the waveform has shifted from a certain reference point along the horizontal zero axis. The phase shift can also be expressed as a time shift of **τ** seconds representing a fraction of the time period **T** [17]. The next figure illustrates two sinusoidal waveforms phase shifted by 90°.

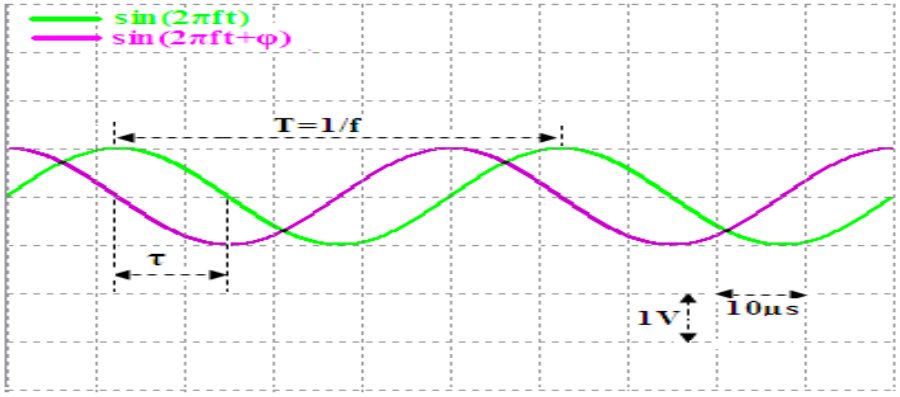


Figure 2: Two sine waves phase shifted by 90°.

The phase shift between the two sine waves can be expressed by:

$$\varphi = 2\pi\tau/T \text{ in radians} \quad (3)$$

And

$$\varphi = 360\tau/T \text{ in degrees} \quad (4)$$

Where T is the sine wave's period which is equal to 50µs and τ is the time lag between the two signals which is equal to 12.5µs. So, we can verify the phase shift value between the two signals shown above using the equation (2): $\varphi=360*12.5/50=90°$

## V. THE PROPOSED TESTING METHODOLOGY USING THE FPAA TECHNOLOGY

The proposed testing methodology is base on hardware redundancy. In fact we will distinguish a faulty circuit from a fault-free one by controlling the phase shift between the two considered outputs. The general test procedure is presented by Fig. 3.

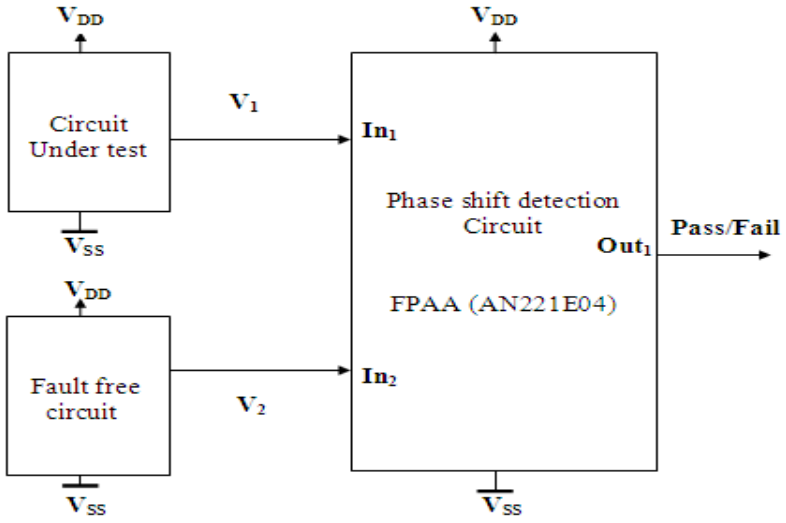


Figure 3: The proposed test approach using the AN221E04 FPAA device

Thereby, the fault detection is obtained through comparing the analog output voltage of the circuit under test ($V_1$) to a fault free one ($V_2$). If the testing circuit configured using the AN221E04 board detect a phase shift between the circuit under test output and the faulty free one we assume that the circuit under test gives a wrong signal output. Consequently, the Pass/Fail signal switches from low level (Pass) to high level (Fail) to indicate that the circuit probably contains faults.
Once the fault is detected, we precede to the correctness acts. In fact, the correctness act in our case can be done by replacing the output of the faulty circuit under test by the fault-free one. The hardware redundancy used to detect faults causing phase shift errors in the CUT can be used to correct these faults. Therefore, we have a fault tolerance architecture which assures a correct system functioning even in presence of faults. This fault tolerance mechanism is so important especially for safety-critical systems to avoid the system failure which can cause real damages.
The phase shift detection circuit is illustrated by the circuit diagram given by Fig. 4.

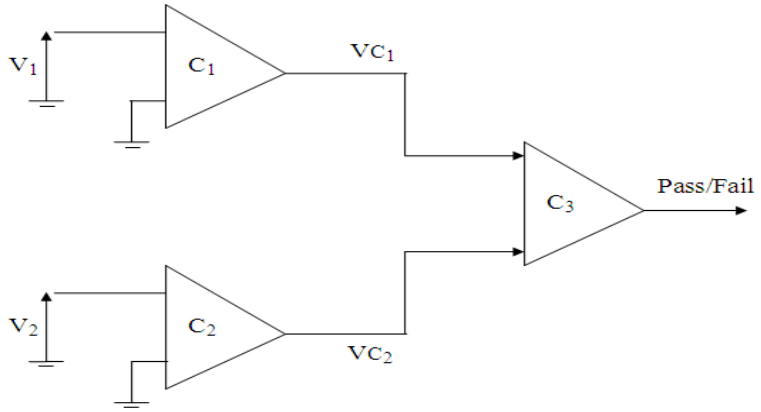


Figure 4: The bloc diagram illustrating the phase shift detection circuit

The two analog comparators $C_1$ and $C_2$ are used to compare to zero (ground) respectively the two signals $V_1$ and $V_2$. So, the output of each comparator is a digital signal which switches to the high level (VDD) when the correspondent signal is greater than zero. Otherwise it should switch to the low level (VSS). $C_3$ is a dual comparator used to compare the two digital comparators outputs $VC_1$ and $VC_2$. In fact, the Pass/Fail signal which is the output of the comparator $C_3$ switches from the low level to the high level when $VC_1 < VC_2$.

The Circuit design and implementation are enabled using AnadigmDesigner®2 software. The circuit design illustrating our test methodology is presented in Fig. 4.

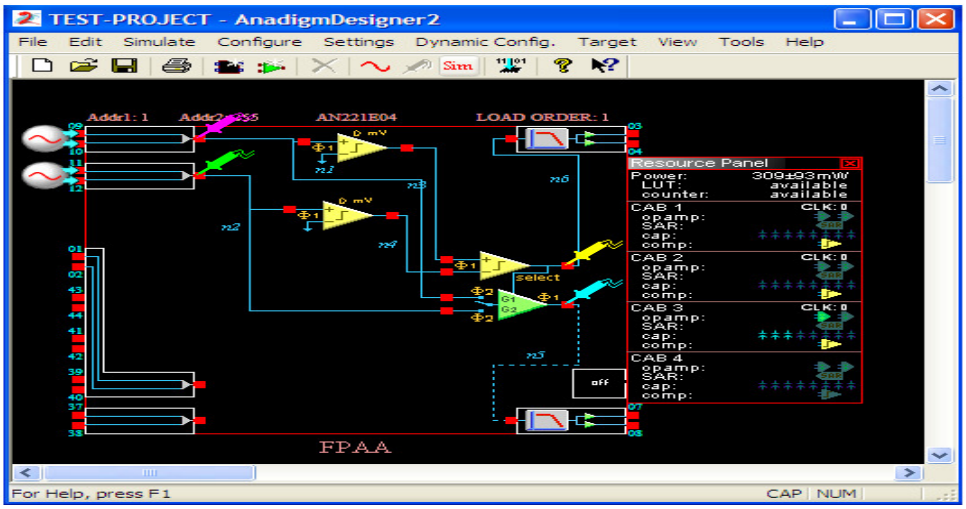


Figure 4: the phase shift detection circuit implemented using the AN221E04 FPAA device

From fig. 2, we note that the phase shift detection circuit implementation only needs the use of three CAM's which are two comparators ($C_1$ and $C_2$) and a Gain Stage with Switchable Inputs ($C_3$). As shown in the resource panel given by the same figure the circuit implementation requires the use of three CABs (CAB 1, 2 and 3).

## VI. SIMULATION RESULTS

The fault-free ($V_2$) and the faulty ($V_1$) outputs simulation are given by Fig. 5. In this case the phase shift absolute value between the two signals is equal to 30°.

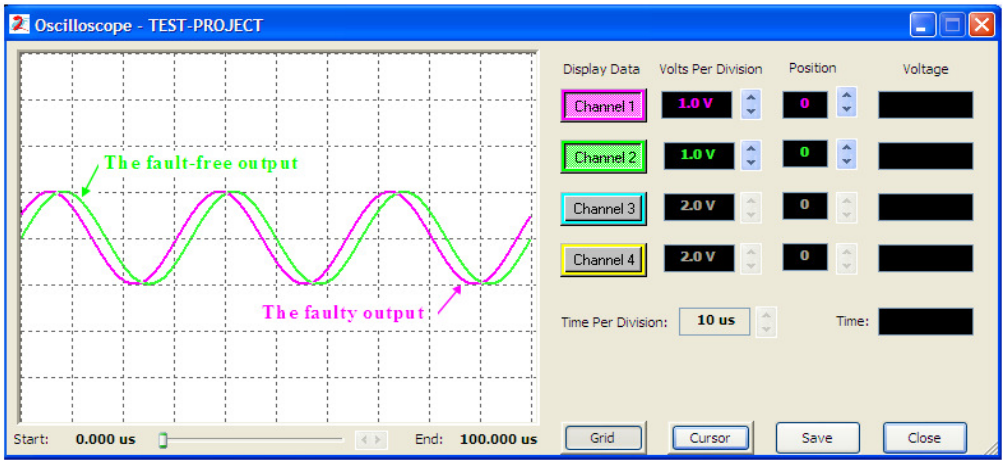


Figure 5: the fault-free and the faulty outputs simulation

Fig. 6 illustrates the fault-free and the first comparator ($C_1$) outputs simulation results. In fact, the first comparator compares the fault-free output ($V_2$) to the ground. If the considered output is higher than 0mv the comparator output switches to the high level (5V) otherwise it switches to the low level (-5V).

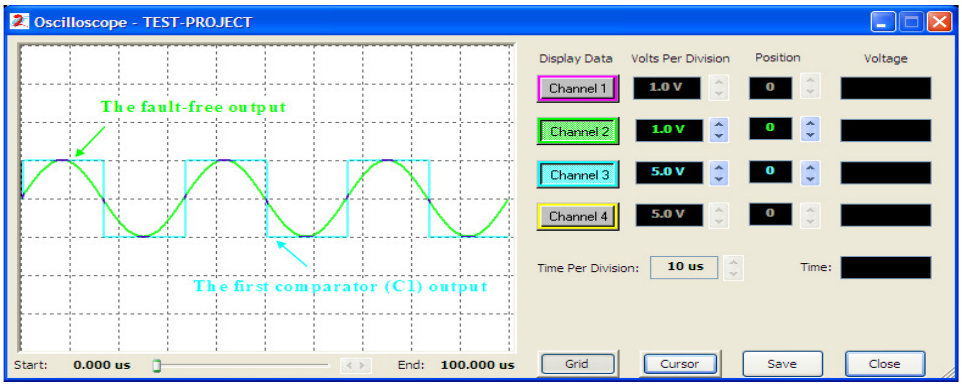


Figure 6: The fault-free and the first comparator outputs simulation results

Fig. 7 illustrates the faulty output of the circuit under test and the second comparator ($C_2$) output simulation results.

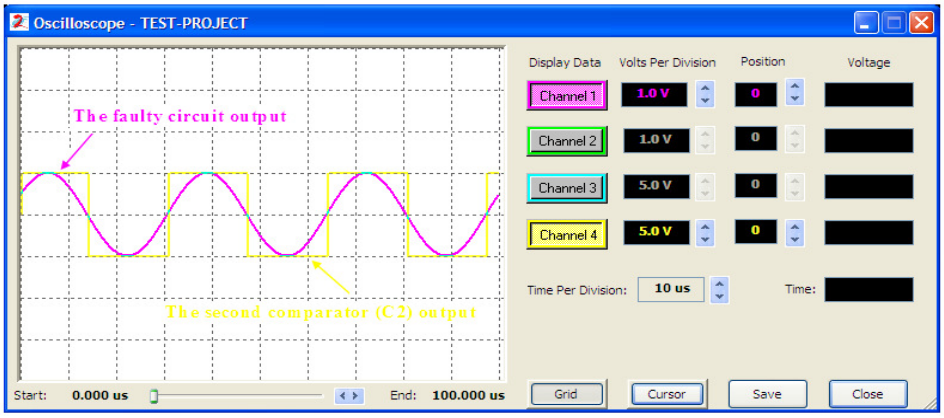


Figure 7: The faulty and the second comparator outputs simulation results

The second comparator ($C_2$) compares the output under test to the ground. If the considered output is higher than 0mv the comparator output switches to the high level otherwise it switches to the low level.
Fig. 8 presents the superposed comparator's outputs and the Pass/Fail signal which is the output of the Gain Stage with Switchable Inputs CAM ($C_3$) used as a dual comparator.

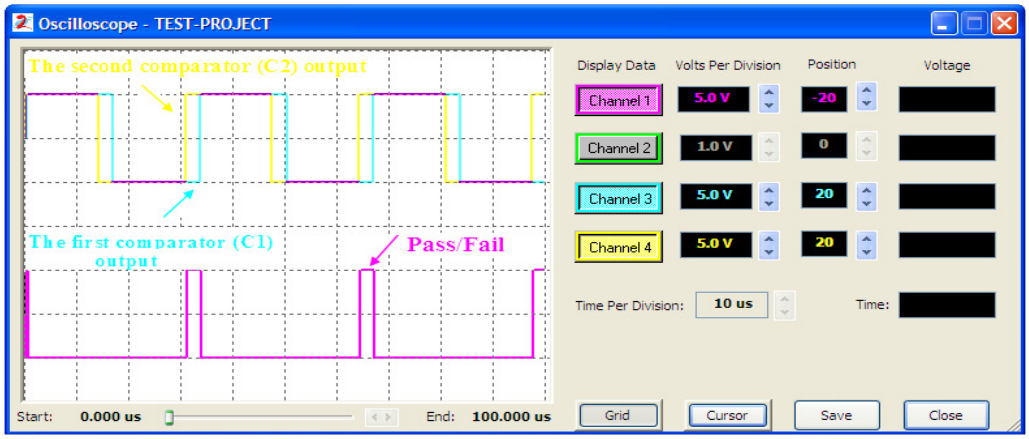


Figure 8: the comparators and the Pass/Fail outputs simulation results

Fig. 9 presents the fault-free, the faulty and the Pass/Fail outputs simulation results.

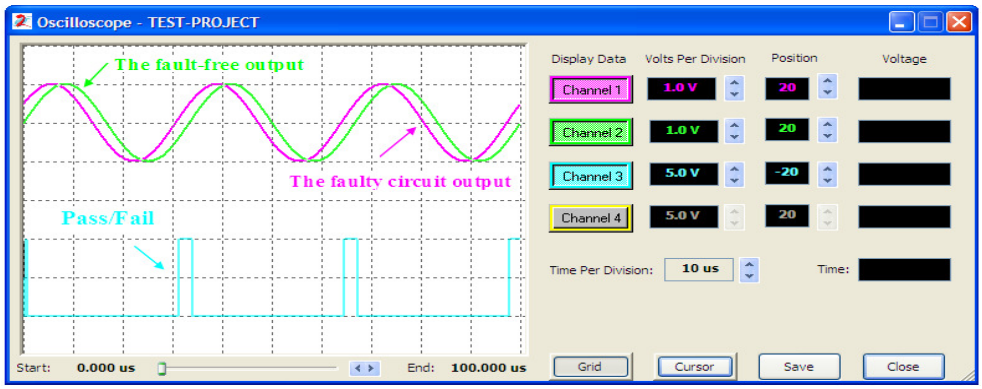


Figure 9: the fault-free, the faulty and the Pass/Fail outputs simulation results

Simulation results given by Fig. 9 ensure that the phase shift detection circuit behaves as intended. In fact, the phase shift existing between the fault-free and the faulty outputs is detected by the phase shift detection circuit. Thus, when the Pass/Fail signal passes to the high level, we assume that the output signal of the circuit under test presents a phase shift error. In addition, the information contained in the Pass/Fail signal enables us to know the exact value of the phase shift between the fault-free and the faulty outputs. Fig. 10 illustrates only the Pass/Fail signal.

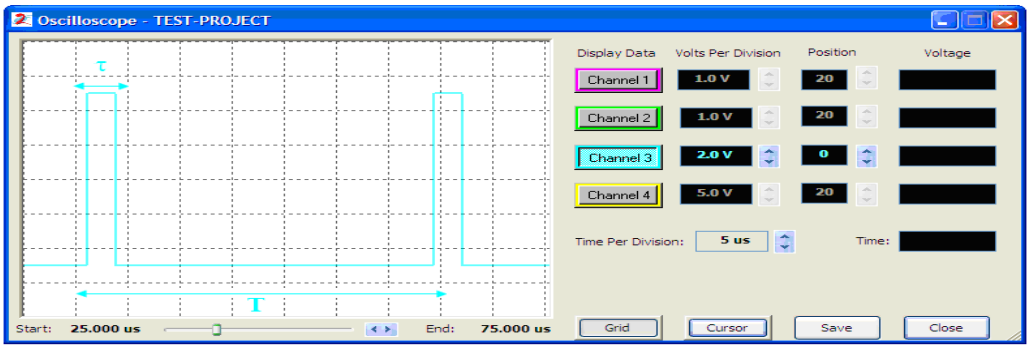


Figure 9: The Pass/Fail signal

In fact, $\tau$ and T are respectively the time high and the period of the Pass/Fail signal. The phase shift value in degree is equal to $360^* \tau /T$. In our case, the shift value obtained by simulation is equal to 360*(33.875-31.125)/(64.375-33.875)=32.45°.

## VII. CONCLUSION

In this paper, we have presented the Field Programmable Analog Arrays technology which introduces new opportunities to improve analog circuit design and signal processing by providing a method for analog systems rapid prototyping. FPAAs elevate the design and implementation process of analog design to high levels of abstraction. This reduces integrated circuit test costs and time to market.
In fact, an FPAA-based approach phase shift detection circuit is designed and simulated using AnadigmDesigner®2 software. Simulation results show that the technique is effective and prove that the analog integrated circuit design and testing become easier using the Field Programmable Analog Array technology.

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# PROCESS MATURITY ASSESSMENT OF THE NIGERIAN SOFTWARE INDUSTRY

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## *ABSTRACT*

*Capability Maturity Model Integration (CMMI) is a recognized tool for performing software process maturity and capability evaluation in software organizations. Experience with software companies in Nigeria shows that most project management activities do not follow the conventional practices. The study considered the extent to which companies make use of organizational software process in performing their software development activities. The extent to which software products are developed and documented as well as level of adherence to existing organizational software process were studied among Twenty-six (26) selected software companies in Nigeria. The selection criteria were based on: availability of personnel to provide adequate information; size of the development team; how established the companies are; and geographical distribution. Our study revealed that the software companies do not have adequate documentation of their organizational software process, and that most of the companies carry out their software development process by means of implicit in-house methods.*

***KEYWORDS:*** Software Process, Software Industry, CMMI, Nigeria

## I. INTRODUCTION

Success in software development is expected to be repeatable if the team involved is to be described as dependable. Dependability in software development can only be achieved through rigorous software development processes and project management practices. Understanding organizational goals and aspirations, is always the first step in making progress of any kind.

This study focuses on knowing the current state of software process maturity level of the Nigerian software industry. Nigeria is a strategic market for application software in the African continent. The Nigerian software industry has a strategic influence in West Africa. The bulk of the Nigerian software industry is located in the commercial capital of Lagos. According to the 2004 study by Soriyan and Heeks [13, 14], Lagos, which is widely regarded as Nigeria's "economic capital", accounts for 52 software companies representing about 49 percent of the software companies in Nigeria.

The study was conducted to determine the Capability and Maturity levels of the Nigerian software industry using the CMMI Model. The specific objectives of the study are listed below:

- Survey the software practices adopted by a good number of software companies;
- Apply the SEI Maturity Questionnaire to further gather data;
- Properly summarize and document the data collected;
- Evaluate the practices in the industry based on key process areas.
- Apply CMMI methods to determine the maturity and capability levels of the industry.

The rest of the paper is organized as follows. Section 2 reviews some literatures related to this work. Section 3 discusses the approach applied in performing the study. Section 4 discusses the findings of the study. Section five summarizes the conclusions drawn from the study.

# II. LITERATURE REVIEW

Heyworth [5] described the characteristics of projects to include bringing about a change of state in entities of concern within well planned time frames. This indicates a strong relationship between projects and processes.

A prior study comparing CMMI appraisals for different countries have been reported by Urtans [6]. The study revealed the observed trends in CMM to include the following:

- Higher maturity levels seen mostly outside the USA
- India is the leader in CMM
- China and Korea are emerging as outsourcing centers
  - Increasing number of high maturity companies
- Canada, Ireland, Australia considered for outsourcing due to native English
  - Starting to report lower levels of CMM
- The number of companies each year using CMM to assess their software management practices more than doubles every five years

According to Heeks [7, 8], production of software provides many potential benefits for developing countries, including creation of jobs, skills and income. According to him also, selling software services to the domestic market is the choice of most developing countries software enterprises, but it typically represents a survival strategy more than a development strategy. He further iterated that most information systems - including current ICT projects - in developing countries fail either totally or partially due to the notion he described as design-reality gaps.

Soriyan and Heeks [13] gave a very descriptive view of the Nigerian software industry. According to them, 43.7% of the companies had 1-5 IT professionals, 27.2% had 6-15, 23.3% had 16-50, and only 5.8% of firms had more than 50 IT professionals. Also, 51% of the companies were involved with servicing imported applications, 25% were involved with Developing and servicing local applications, while 24% were involved with servicing and developing local and imported applications. This basically reveals that most of the software companies in the industry are small, and not as much attention as expected is given to developing and servicing local applications. Virtually no attention is given to the development of software tool. Also, their work revealed that Nigerian software industry showed significant use of formal methods but with a strong tendency to rely on in-house-developed methods rather than industry standards.

The work of Paulk et al [9, 10] produced the Maturity Questionnaire (MQ) which formed the major instrument of information elicitation during the course of the study discussed in this paper. According to Ahern et al [1], Standard CMMI Appraisal Method for Process Improvement (SCAMPI) appraisals can help organizations identify the strengths and weaknesses of their current processes, reveal crucial development and acquisition risks, set priorities for improvement plans, derive capability and maturity level ratings, and even perform realistic benchmarking.

For this study we used the maturity questionnaire for eliciting information from surveyed companies, while

## 2.1. The Capability Maturity Model Integration (CMMI)

CMMI is a model for evaluating the maturity of software development process. It was developed from CMM**.** CMMI stands for Capability Maturity Model Integration. It is a method to evaluate and measure the maturity of the software development process of an organization. It measures the maturity of the software development process on a scale of 1 to 5. It was developed by the Software Engineering Institute (SEI) at Carnegie Mellon University in Pittsburgh, USA [3, 12].

## 2.2. Maturity Level

A maturity level can be said to be a well-defined evolutionary plateau toward achieving a mature software process. Each maturity level provides a layer in the foundation for continuous process improvement. In CMMI models, there are five maturity levels designated by the numbers 1 through 5.

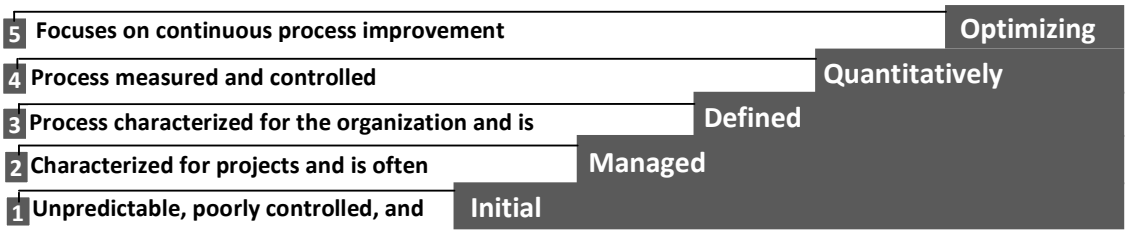



*Fig. 1: The Five Levels of CMMI [3, 12]*

Maturity levels consist of a predefined set of process areas. The maturity levels are measured by the achievement of the specific and generic goals that apply to each predefined set of process areas. The following sections describe the characteristics of organizations at each maturity level.

Maturity Level 1 – Initial: Processes are usually ad hoc and chaotic. They do not provide stable work environment. Success depends on the competence and heroics of the people in the organization and not on the use of proven processes.

Maturity Level 2 – Managed: The projects of the organization have ensured that requirements are managed and that processes are planned performed, measured, and controlled. They ensure that existing practices are retained during times of stress.

Maturity Level 3 – Defined: Processes are well characterized and understood, and are described in standards, procedures, tools, and methods.

Maturity Level 4 - Quantitatively Managed: At maturity level 4 sub-processes are selected that significantly contribute to overall process performance. These selected sub-processes are controlled using statistical and other quantitative techniques.

Maturity Level 5 – Optimizing: Processes are continually improved based on a quantitative understanding of the common causes of variation inherent in processes. Maturity level 5 focuses on continually improving process performance.
Maturity levels should not be skipped. Each maturity level provides a necessary foundation for effective implementation of processes at the next level.

- Higher level processes have less chance of success without the discipline provided by lower levels.
- The effect of innovation can be obscured in a noisy process.

Higher maturity level processes may be performed by organizations at lower maturity levels, with the risk of not being consistently applied in a crisis [3].

## 2.3. Capability Level

A capability level is a well-defined evolutionary plateau describing the organization's capability relative to a process area. Capability levels are cumulative, i.e., a higher capability level includes the attributes of the lower levels. In CMMI models with a continuous representation, there are six capability levels designated by the numbers 0 through 5.

Capability Level 0 **–** Incomplete: An "incomplete process" is a process that is either not performed or partially performed. One or more of the specific goals of the process area are not satisfied and no generic goals exist for this level.

Capability Level 1 **–** Performed: This is a process that is expected to perform all of the Capability Level 1 specific and generic practices. Performance may not be stable and may not meet specific

objectives such as quality, and cost, but useful work can be done. It means that you are doing something but you cannot prove that it really works for you.

Capability Level 2 – Managed: A managed process is planned, performed, monitored, and controlled for individual projects, groups, or stand-alone processes to achieve a given purpose. Managing the process achieves both the model objectives for the process as well as other objectives, such as cost, schedule, and quality.

Capability Level 3 – Defined: A defined process is a managed (capability level 2) process that is tailored from the organization's set of standard processes according to the organization's tailoring guidelines, and contributes work products, measures, and other process-improvement information to the organizational process assets.

Capability Level 4 – Quantitatively Managed: A quantitatively managed process is a defined (capability level 3) process that is controlled using statistical and other quantitative techniques. Quantitative objectives for quality and process performance are established and used as criteria in managing the process.

Capability Level 5 – Optimizing: An optimizing process is a quantitatively managed process that is improved, based on an understanding of the common causes of process variation inherent in the process. It focuses on continually improving process performance through both incremental and innovative improvements [3].
Fusaro et al [11] did some work on the reliability test of the SEI MQ. According to them, the Spearman-Brown formula was used to make all of the reliability estimates applicable to instruments of equal lengths. During their study, a point was noted where all of the internal consistency values for full length instruments were above the 0.9 minimal threshold. For this reason, the full length instrument was therefore considered to be internally consistent for practical purposes.

# III. RESEARCH DESIGN, METHODOLOGY AND APPROACH

This study was aimed at assessing software process maturity in the Nigerian software industry. In this section, the methodology and approach we took in carrying out this study is outlined.
The purpose of this section is to:

- Discuss the research philosophy used in this work;
- Expound the research strategy adopted in this work, including the research methodologies adopted;
- Introduce the research instruments we adopted in the carrying out the research.

Two major research methodologies were applied in performing this study. These methodologies are survey research and case study research methodologies.
Survey Research: According to our research objectives, we surveyed the software practices adopted by many of the Nigerian software companies. For this study 30 Nigerian software companies were studied. 27 of those companies were based in Lagos southwestern Nigeria, while three were based in Asaba, south-southern Nigeria. The sampling method is stratified in the sense that the majority of Nigeria's software companies were based in Lagos.
An instrument – the SEI Maturity Questionnaire (MQ) – was used to gather information about software process implementation within the companies covered. This instrument was administered to solutions developers and software project managers in the industry. This instrument served as the key data collection tool for the survey.
Case Study Research: Some of the companies were taken as case studies for more detailed investigation. A direct observation of their activities and environment was carried out. Indirect observation and measurement of process related phenomena was also performed. The companies involved were visited and observed over a period of time to see how they actually implement their software development process. Both structured and unstructured interviews were also used to solicit information. Documentation, such as written, printed and electronic information about the company and its operations were another method by which information was gathered.

In order to analyze the current situation in the Nigerian software industry, it is essential to have a validated and reliable instrument for the collection of the information required. For this reason, the SEI Maturity Questionnaire was adopted.

### 3.1 The Software Process SEI Maturity Questionnaire (MQ)

The software process maturity questionnaire (MQ) replaces the 1987 version of the maturity questionnaire, CMU/SEI-87-TR-23, in the 1994 set of SEI appraisal products. This version of the questionnaire is based on the capability maturity model (CMM) v1.1. It has been designed for use in the new CMM-based software process appraisal methods: the CMM-based appraisal for internal process improvement (CBA IPI) which is the update of the original software process assessment (SPA) method, CMM-based software capability evaluations (SCEs), and the interim profile method. The questionnaire focuses solely on process issues, specifically those derived from the CMM. The questionnaire is organized by CMM key process areas (KPAs) and covers all 18 KPAs of the CMM. It addresses each KPA goal in the CMM but not all of the key practices. By keeping the questions to only 6 to 8 per KPA, the questionnaire can usually be completed in one hour [4].

## IV. RESEARCH FINDINGS AND INTERPRETATION

In as much as the Standard CMMI Appraisal Method for Process Improvement (SCAMPI) is an appraisal method that meets all of the Appraisal Requirements for CMMI (ARC), and currently the only SEI approved Class A appraisal method, it was used in appraising the industry.

### 4.1 Evaluation of Research Findings

Out of the 30 companies surveyed, only responses from 26 companies were found useful. Responses from four companies were either inconsistent or could not be verified. As such, the evaluation of the companies was based on responses from 26 companies. 23 of these were based in Lagos, while three were based in Asaba.

In order to meet the objective of this study, the key practices were organized according to key process areas (labeled in Roman numerals). The key process areas were organized according to maturity level. Only the result for maturity level 2 is discussed this section. This is because an evaluation of the key practices at maturity level 2 suffices to arrive at a conclusion as to which maturity level the Nigerian software industry belongs.

To appraise an organization using the Standard CMMI Appraisal Method for Process Improvement (SCAMPI), the organization (Industry) is considered to have reached a particular level of maturity when it has met with all of the objectives/practices within each of the key process areas from maturity level 2 to the maturity level in question. This work shall therefore progress in that order, starting with the appraisal of the key process areas and practices found within maturity level2, until a point is reached where all the objectives/practices associated with a particular KPA are not met.

In the instrument that was administered, “Yes” connotes that the organizations perform the specified practice, while “No” means that the organization does not perform the specified practice. In the summary tables found in this section of the work:

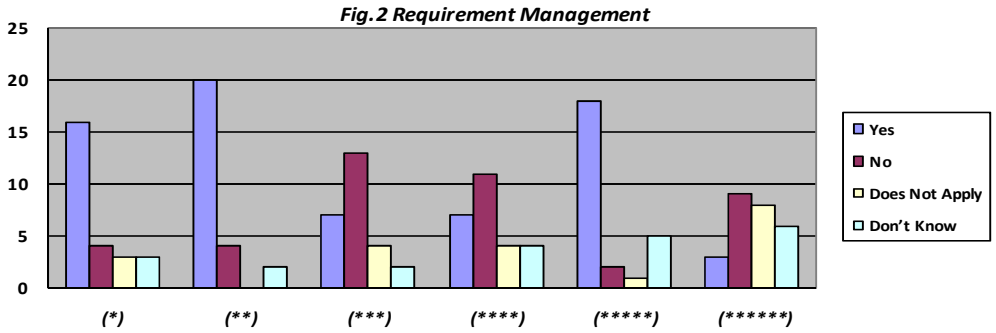
- The “Yes” column indicates the number of companies that perform the specified practice;
- The “No” column indicates the number of companies that do not perform the specified practice;
- Both the “Does Not Apply” and the “Don’t Know” column values are used in the appraisal to indicate the amount of organizational unawareness in the industry;
- Percentage values are recomputed for the number of explicit (“yes” or “no”) responses gathered, and would be used as a major appraisal factor.

## 4.2 Evaluation of the Results Obtained for Maturity Level 2 (Managed)

### *4.2.1. Requirement Management*

*Table 1: Requirement Management*

| I Requirement Management | | | | | |
|---|---|---|---|---|---|
| | QUESTIONS (Key Practices) | Yes | No | Does Not Apply | Don't Know |
| 1 | Are system requirements allocated to software used to establish a baseline for software engineering and management use? – *(*)* | 16 | 4 | 3 | 3 |
| 2 | As the systems requirements allocated to software change, are the necessary adjustments to software plans, work products, and activities made? – *(**)* | 20 | 4 | 0 | 2 |
| 3 | Does the project follow a written organizational policy for managing the system requirements allocated to software? – *(***)* | 7 | 13 | 4 | 2 |
| 4 | Are the people in the project that are charged with managing the allocated requirements trained in the procedures for managing allocated requirements? – *(****)* | 7 | 11 | 4 | 4 |
| 5 | Are measurements used to determine the status of the activities performed for managing the allocated requirements (e.g., total number of requirements changes that are proposed, open, approved, and incorporated into the baseline). – *(*****)* | 18 | 2 | 1 | 5 |
| 6 | Are the activities for managing allocated requirements on the project subjected to SQA review? – *(******)* | 3 | 9 | 8 | 6 |
| | | 45.5% | 27.6% | 12.8% | 14.1% |



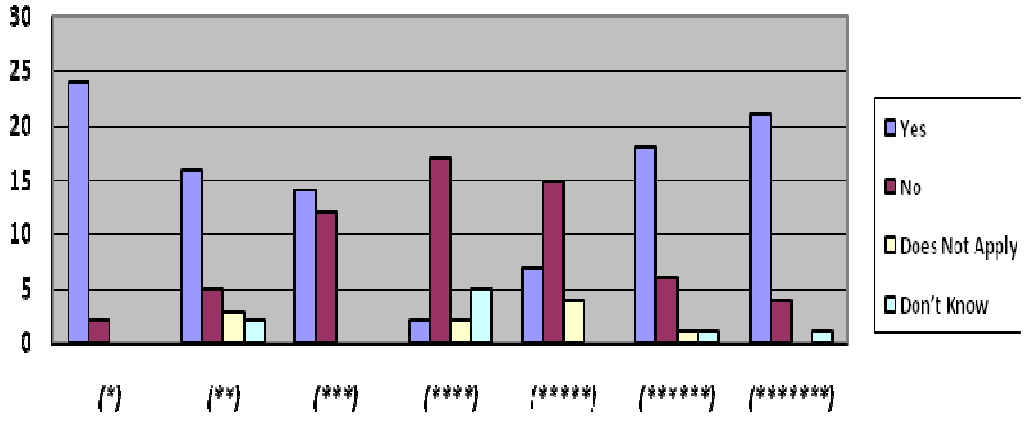

From the table above, out of the total number of people who responded explicitly as either "Yes" or "No", there was a 62.3% bias for the performance of requirement management associated practices, while 37.7% bias holds for non performance of requirement management associated practices. Basically, since industry wide, the "Yes" column contains values greater than zero; it means that at least one company performs one or more of the practices associated with the requirement management key process area.

### *4.2.2. Software Project Planning*

*Table 2: Software Project Planning*

| II<br>Software Project Planning | | | | | |
|---|---|---|---|---|---|
| | QUESTIONS (Key Practices) | Yes | No | Does Not Apply | Don't Know |
| 1 | Are estimates (e.g., size, cost, and schedule) documented for use in planning and tracking the software project? – *(*)* | 24 | 2 | 0 | 0 |
| 2 | Do the software plans document the activities to be performed and the commitments made for the software project? – *(**)* | 16 | 5 | 3 | 2 |
| 3 | Do all affected groups and individuals agree to their commitments related to the software project? – *(***)* | 14 | 12 | 0 | 0 |
| 4 | Does the project follow a written organizational policy for planning a software project? – *(****)* | 2 | 17 | 2 | 5 |
| 5 | Are adequate resources provided for planning the software project (e.g., funding and experienced individuals)? – *(*****)* | 7 | 15 | 4 | 0 |
| 6 | Are measurements used to determine the status of the activities for planning the software project (e.g., completion of milestones for the project planning activities as compared to the plan)? – *(******)* | 18 | 6 | 1 | 1 |
| 7 | Does the project manager review the activities for planning the software project on both a periodic and event-driven basis? – *(*******)* | 21 | 4 | 0 | 1 |
| | | 56.0% | 33.5% | 5.5% | 4.9% |

*Fig.3 Software Project Planning*



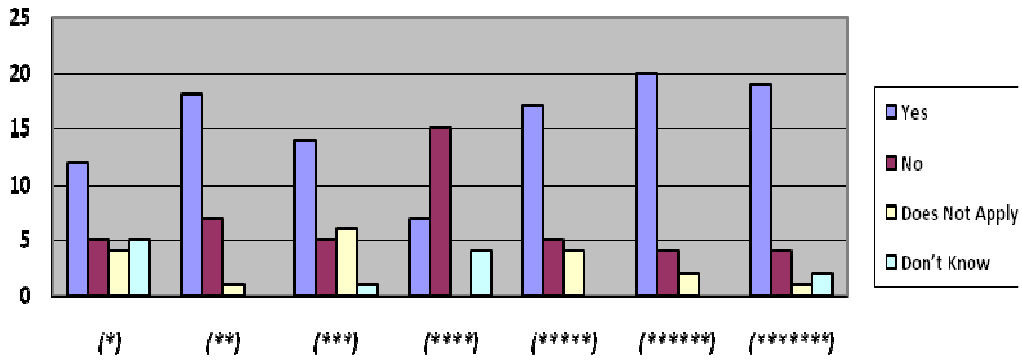

From the table above, out of the total number of people who responded explicitly as either "Yes" or "No", there was a 62.6% bias for the software project planning associated practices, while a 37.4% bias holds for non performance of software project planning associated practices. Basically, since industry wide, the "Yes" column contains values greater than zero; it means that at least one company performs one or more of the practices associated with the software project planning key process area.

### *4.2.3. Software Project Tracking and Oversight*

*Table 3: Software Project Tracking and Oversight*

| **III Software Project Tracking and Oversight** | | | | | |
|---|---|---|---|---|---|
| | QUESTIONS (Key Practices) | Yes | No | Does Not Apply | Don't Know |
| 1 | Are the project's actual results (e.g., schedule, size, and cost) compared with estimates in the software plans? – *(*)* | 12 | 5 | 4 | 5 |
| 2 | Is corrective action taken when actual results deviate significantly from the project's software plans? – *(**)* | 18 | 7 | 1 | 0 |
| 3 | Are changes in the software commitments agreed to by all affected groups and individuals? – *(***)* | 14 | 5 | 6 | 1 |
| 4 | Does the project follow a written organizational policy for both tracking and controlling its software development activities? – *(****)* | 7 | 15 | 0 | 4 |
| 5 | Is someone on the project assigned specific responsibilities for tracking software work products and activities (e.g., effort, schedule, and budget)? – *(*****)* | 17 | 5 | 4 | 0 |
| 6 | Are measurements used to determine the status of the activities for software tracking and oversight (e.g., total effort expended in performing tracking and oversight activities)? – *(******)* | 20 | 4 | 2 | 0 |
| 7 | Are the activities for software project tracking and oversight reviewed with senior management on a periodic basis (e.g., project performance, open issues, risks, and action items)? – *(*******)* | 19 | 4 | 1 | 2 |
| | | 58.8% | 24.7% | 9.9% | 6.6% |

*Fig.4 Software Project Tracking and Oversight*



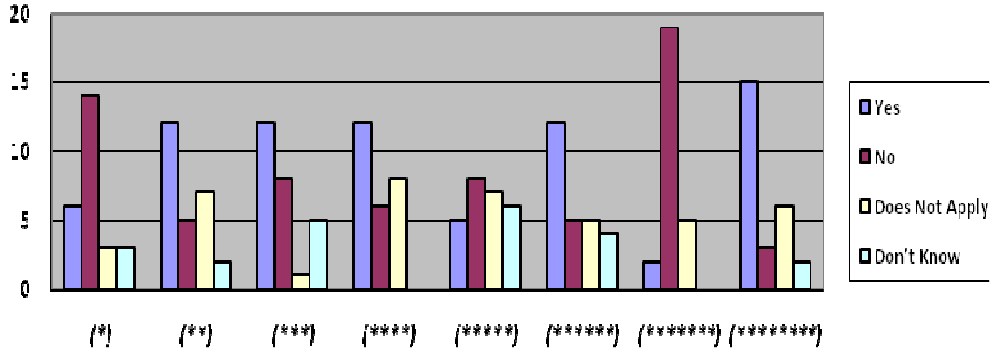

From the table above, out of the total number of people who responded explicitly as either "Yes" or "No", there was a 70.4% bias for the software project tracking and oversight associated practices, while a 29.6% bias holds for non performance of software project tracking and oversight associated practices. Basically, since industry wide, the "Yes" column contains values greater than zero; it means that at least one company performs one or more of the practices associated with the software project tracking and oversight key process area.

### *4.2.4. Software Subcontract Management*

*Table 4: Software Subcontract Management*

| IV<br>Software Subcontract Management | | | | | |
|---|---|---|---|---|---|
| | QUESTIONS<br>(Key Practices) | Yes | No | Does Not Apply | Don't Know |
| 1 | Is a documented procedure used for selecting subcontractors based on their ability to perform the work? – *(*)* | 6 | 14 | 3 | 3 |
| 2 | Are changes to subcontracts made with the agreement of both the prime contractor and the subcontractor? – *(**)* | 12 | 5 | 7 | 2 |
| 3 | Are periodic technical interchanges held with subcontractors? – *(***)* | 12 | 8 | 1 | 5 |
| 4 | Are the results and performance of the software subcontractor tracked against their commitments? – *(****)* | 12 | 6 | 8 | 0 |
| 5 | Does the project follow a written organizational policy for managing software subcontracts? – *(*****)* | 5 | 8 | 7 | 6 |
| 6 | Are the people responsible for managing software subcontracts trained in managing software subcontracts? – *(******)* | 12 | 5 | 5 | 4 |
| 7 | Are measurements used to determine the status of the activities for managing software subcontracts (e.g., schedule status with respect to planned delivery dates and effort expended for managing the subcontract)? – *(*******)* | 2 | 19 | 5 | 0 |
| 8 | Are the software subcontract activities reviewed with the project manager on both a periodic and event-driven basis? – *(********)* | 15 | 3 | 6 | 2 |
| | | 36.5% | 32.7% | 20.2% | 10.6% |

*Fig.5 Software Subcontract Management*



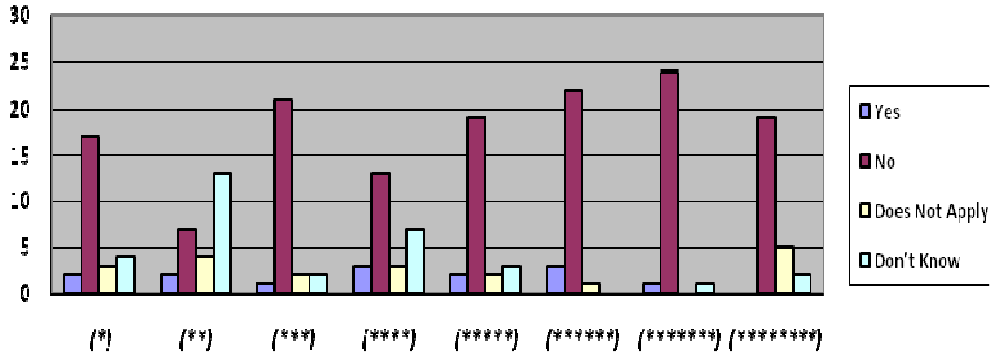

From the table above, out of the total number of people who responded explicitly as either "Yes" or "No", there was a 52.8% bias for the software subcontract management associated practices, while a 47.2% bias holds for non performance of software subcontract management associated practices. Basically, since industry wide, the "Yes" column contains values greater than zero; it means that at least one company performs one or more of the practices associated with the software subcontract management key process area.

### *4.2.5. Software Quality Assurance (SQA)*

*Table 5: Software Quality Assurance (SQA)*

| **V**<br>**Software Quality Assurance** (SQA) | | | | | |
|---|---|---|---|---|---|
| | QUESTIONS<br>(Key Practices) | Yes | No | Does Not Apply | Don't Know |
| 1 | Are SQA activities planned? – *(*)* | 2 | 17 | 3 | 4 |
| 2 | Does SQA provide objective verification that software products and activities adhere to applicable standards, procedures, and requirements? – *(**)* | 2 | 7 | 4 | 13 |
| 3 | Are the results of SQA reviews and audits provided to affected groups and individuals (e.g., those who performed the work and those who are responsible for the work)? – *(***)* | 1 | 21 | 2 | 2 |
| 4 | Are issues of noncompliance that are not resolved within the software project addressed by senior management (e.g., deviations from applicable standards)? – *(****)* | 3 | 13 | 3 | 7 |
| 5 | Does the project follow a written organizational policy for implementing SQA? – *(*****)* | 2 | 19 | 2 | 3 |
| 6 | Are adequate resources provided for performing SQA activities (e.g., funding and a designated manager who will receive and act on software noncompliance items)? – *(******)* | 3 | 22 | 1 | 0 |
| 7 | Are measurements used to determine the cost and schedule status of the activities performed for SQA (e.g., work completed, effort and funds expended compared to the plan)? – *(*******)* | 1 | 24 | 0 | 1 |
| 8 | Are activities for SQA reviewed with senior management on a periodic basis? – *(********)* | 0 | 19 | 5 | 2 |
| | | 6.7% | 68.3% | 9.6% | 15.4% |

*Fig.6 Software Quality Assurance (SQA)*




From the table above, out of the total number of people who responded explicitly as either "Yes" or "No", there was a 9.0% bias for the software quality assurance associated practices, while a 91.0% bias holds for non performance of software quality assurance associated practices. Basically, since industry wide, the "Yes" column contains a zero value at some point; it means that no company performs one or more of the practices associated with the software quality assurance key process area.

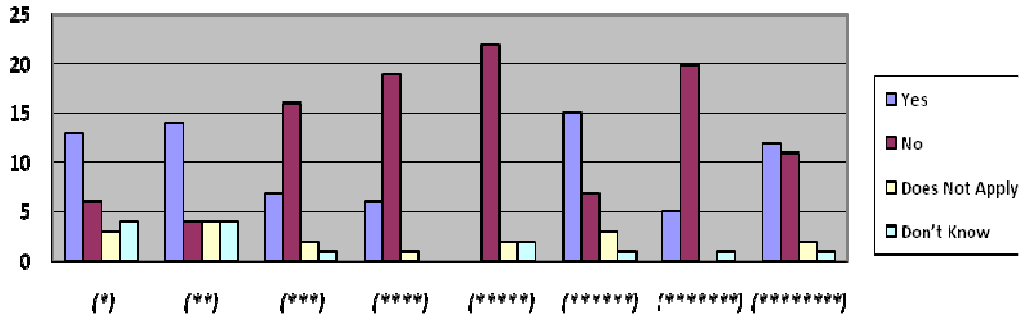
Industry wide, this is an explicit violation of the requirement for an industry to be at this current maturity level (2) under consideration.

### *4.2.6. Software Configuration Management (SCM)*

*Table 6: Software Configuration Management (SCM)*

| **VI**<br>**Software Configuration Management** (SCM) | | | | | |
|---|---|---|---|---|---|
| | QUESTIONS<br>(Key Practices) | Yes | No | Does Not Apply | Don't Know |
| 1 | Are software configuration management activities planned for the project? – *(*)* | 13 | 6 | 3 | 4 |
| 2 | Has the project identified, controlled, and made available the software work products through the use of configuration management? – *(**)* | 14 | 4 | 4 | 4 |
| 3 | Does the project follow a documented procedure to control changes to configuration items/units? – *(***)* | 7 | 16 | 2 | 1 |
| 4 | Are standard reports on software baselines (e.g., software configuration control board minutes and change request summary and status reports) distributed to affected groups and individuals? – *(****)* | 6 | 19 | 1 | 0 |
| 5 | Does the project follow a written organizational policy for implementing software configuration management activities? – *(*****)* | 0 | 22 | 2 | 2 |
| 6 | Are project personnel trained to perform the software configuration management activities for which they are responsible? – *(******)* | 15 | 7 | 3 | 1 |
| 7 | Are measurements used to determine the status of activities for software configuration management (e.g., effort and funds expended for software configuration management activities)? – *(*******)* | 5 | 20 | 0 | 1 |
| 8 | Are periodic audits performed to verify that software baselines conform to the documentation that defines them (e.g., by the SCM group)? – *(********)* | 12 | 11 | 2 | 1 |
| | | 34.6% | 50.5% | 8.2% | 6.7% |

*Fig.7 Software Configuration Management (SCM)*




From the table above, out of the total number of people who responded explicitly as either "Yes" or "No", there was a 40.7% bias for the software configuration management associated practices, while a 59.3% bias holds for non performance of software configuration management associated practices. Basically, since industry wide, the "Yes" column contains a zero value at some point; it means that no company performs one or more of the practices associated with the software configuration management key process area. Industry wide, this is an explicit violation of the requirement for an industry to be at this current maturity level (2) under consideration.

# V. RESULT AND DISCUSSION

The result of the study is expressed in terms of Software Process Maturity Assessment and Capability Assessment of the industry. The capability assessment is done based on individual KPAs while the maturity assessment is based on a specific collection of KPAs for each maturity level.

## 5.1. Software Process Maturity Assessment

From the foregoing data in section 4, it can be deduced that due to the explicit violation of the requirement that at maturity level 2, an organization/industry has achieved all the specific and generic goals of the maturity level 2 process areas, it suffices to conclude that the Nigerian software industry does not belong to the SEI CMMI Maturity level 2. Hence, it suffices to conclude that the Nigerian software industry is at the SEI CMMI Maturity Level 1.

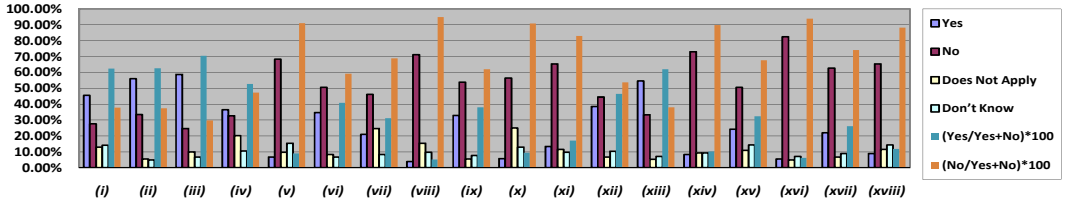
## 5.2. Key Process Area Capability Assessment

The project management practice in the Nigerian software industry was evaluated based on the key process areas identified by the adopted SEI Maturity Questionnaire. Table 7 below gives a high level summary of the data collected from the research. The percentage values for the number of explicit "yes" or explicit "no" responses gathered are shown in the columns "(Yes/Yes+No)*100" and "(No/Yes+ No)*100" respectively.

*Table 7: Summary of Collected Data*

| S/N | Key Process Area (KPA) | Yes | No | Does Not Apply | Don't Know | | (Yes/Yes+No)*100 | (No/Yes+No)*100 |
|---|---|---|---|---|---|---|---|---|
| 1 | Requirements Management – ***(i)*** | 45.51% | 27.56% | 12.82% | 14.10% | | 62.28% | 37.72% |
| 2 | Software Project Planning – ***(ii)*** | 56.04% | 33.52% | 5.49% | 4.95% | | 62.58% | 37.42% |
| 3 | Software Project Tracking and Oversight – ***(iii)*** | 58.79% | 24.73% | 9.89% | 6.59% | | 70.39% | 29.61% |
| 4 | Software Subcontract Management – ***(iv)*** | 36.54% | 32.69% | 20.19% | 10.58% | | 52.78% | 47.22% |
| 5 | Software Quality Assurance – ***(v)*** | 6.73% | 68.27% | 9.62% | 15.38% | | 8.97% | 91.03% |
| 6 | Software Configuration Management – ***(vi)*** | 34.62% | 50.48% | 8.17% | 6.73% | | 40.68% | 59.32% |
| 7 | Organization Process Focus – ***(vii)*** | 20.88% | 46.15% | 24.73% | 8.24% | | 31.15% | 68.85% |
| 8 | Organization Process Definition – ***(viii)*** | 3.85% | 71.15% | 15.38% | 9.62% | | 5.13% | 94.87% |
| 9 | Training Program – ***(ix)*** | 32.97% | 53.85% | 5.49% | 7.69% | | 37.97% | 62.03% |
| 10 | Integrated Software Management – ***(x)*** | 5.77% | 56.41% | 25.00% | 12.82% | | 9.28% | 90.72% |
| 11 | Software Product Engineering – ***(xi)*** | 13.46% | 65.38% | 11.54% | 9.62% | | 17.07% | 82.93% |
| 12 | Intergroup Coordination – ***(xii)*** | 38.46% | 44.51% | 6.59% | 10.44% | | 46.36% | 53.64% |
| 13 | Peer Reviews – ***(xiii)*** | 54.49% | 33.33% | 5.13% | 7.05% | | 62.04% | 37.96% |
| 14 | Quantitative Process Management – ***(xiv)*** | 8.24% | 73.08% | 9.34% | 9.34% | | 10.14% | 89.86% |
| 15 | Software Quality Management – ***(xv)*** | 24.18% | 50.55% | 10.99% | 14.29% | | 32.35% | 67.65% |
| 16 | Defect Prevention – ***(xvi)*** | 5.49% | 82.42% | 4.95% | 7.14% | | 6.25% | 93.75% |
| 17 | Technology Change Management – ***(xvii)*** | 21.98% | 62.64% | 6.59% | 8.79% | | 25.97% | 74.03% |
| 18 | Process Change Management – ***(xviii)*** | 8.79% | 65.38% | 11.54% | 14.29% | | 11.85% | 88.15% |

Fig.8 Summary of Collected Data




The conclusions arrived at in the succeeding subsections are based on the data drawn from table 7 above.

### *5.2.1 Requirements Management (RM)*

The Nigerian software industry performs requirement management practices to a good degree. The rudiments for basic requirement management are well carried out, even though it is nowhere near perfection at this point in time. The industry can still do with a whole lot of improvement, especially with requirement management quality assurance. The Requirement Management KPA can be said to be at the SEI CMMI Capability Level 1.

### *5.2.2 Software Project Planning (SPP)*

The software project planning KPA is performed in almost the same degree as the Requirement Management KPA. There however seem to be very little organizational policy for planning software projects. The Software Project Planning KPA can also be said to at the SEI CMMI Capability Level 1.

### *5.2.3 Software Project Tracking and Oversight (SPTO)*

Projects are actively tracked in the Nigerian software industry. The reason for this has been identified to be mainly due to cost management. SPTO can be said to be at the SEI CMMI Capability Level 1

### *5.2.4 Software Subcontract Management (SSM)*

The Nigerian software industry does not involve so much in subcontracting activities. Most subcontracting activities performed are usually on a small scale. Not so much of written organizational policy exists for managing software subcontract, and the measures for managing software subcontracts are not well developed. The SSM KPA can be said to be at the SEI CMMI Capability Level 1.

### *5.2.5 Software Quality Assurance (SQA)*

The performance of SQA activities are at the very minimum in the Nigerian software industry. Findings revealed that for most of the time, SQA activities are not planned, verified, reviewed, nor resolved. They do not follow written organizational policy, lack adequate funding, and lack adequate basis for measurement. SQA KPA can be said to be at the SEI CMMI Capability Level0.

### *5.2.6 Software Configuration Management (SCM)*

The performance of SCM practices in the Nigerian software industry seems to be rather low. Organizational policies supporting SCM practices were difficult to come by. SCM KPA can be said to be at the SEI CMMI Capability Level 0.

### *5.2.7 Organization Process Focus (OPF)*

Most software companies in Nigeria seem to focus too much on the product to be developed. They don't have time to work on the process required to build the product. The SPF KPA can be said to be at the SEI CMMI Capability Level0

### *5.2.8 Organization Process Definition (OPD)*
Most software organizations in Nigeria have very poorly defined software process structure. Some don't even have at all. As expected, this would be at Capability Level 0.

### *5.2.9 Training Program (TP)*
Even though some software organizations are intensive about staff training, the trend does not cut across board. Most pressing is the issue of most software organizations not having any written organizational policy to meet the training needs of its members of staff. This KPA is also at Capability Level 0.

### *5.2.10 Integrated Software Management (ISM)*
Most software organizations do not have well defined organizational software process and therefore do not have a structure to pattern after. This KPA is also at the SEI CMMI Capability Level 0.

### *5.2.11 Software Product Engineering (SPE)*
Most software companies in Nigeria do not involve in SPE practices. This KPA is at Capability Level 0.

### *5.2.12 Intergroup Coordination (IC)*
Even though intergroup coordination seems to be relatively high in the industry, it is not even nearly as high and integrated into the system as it should be. IC KPA is at Capability Level 0.

### *5.2.13 Peer Reviews (PR)*
Peer review practices seem to be actively carried out in software organizations in Nigeria. There is however still much gap to be filled. This KPA is at Capability Level 0.

### *5.2.14 Quantitative Process Management (SPM)*
Quantitative process management seems to be unpopular with the software industry. This is mainly due to the total absence or lack of adequate organizational software process. It is at Capability Level 0.

### *5.2.15 Software Quality Management (SQM)*
The practice of SQM practices in the Nigerian software industry does not seem to be so much on the high side. The seeming lack of written organizational policy calls for a lot of concern and craves for attention. This also falls under the SEI CMMI Capability Level 0.

### *5.2.16 Defect Prevention (DP)*
As important as this KPA is, its practices are not more popular than a few others thus far mentioned. Adequate quality assurance and written organizational policies to support this KPA seem to be wanting. This KPA also falls under the SEI CMMI Capability Level 0.

### *5.2.17 Technology Change Management (TCM)*
This KPA does not seem to be getting much attention. Most software organizations in Nigeria do not have any plan for managing technology changes. This KPA falls under the SEI CMMI Capability Level 0.

### *5.2.18 Process Change Management (PCM)*
Just like most of the other process oriented KPA, the practices associated with PCM are not much favored by the lack of or inadequate organizational software process. Neither documented procedures nor written organizational policies seem to exist for supporting the PCM practices. Its capability level falls in the SEI CMMI Capability Level 0.

### 5.3. Discussion

Results from this study are in consonance with results from studies by other scholars. The study of Soriyan and Heeks [13, 14] shows that the Nigerian software industry is not so inclined to formal, well documented and standardized methodologies. The formalized methods used when there is any are usually developed in-house. According to Urtans [6], India, China, Japan, Korea, Australia, and Canada reported the highest number of appraisals and seem to have the highest maturity rankings. Besides these countries, most other countries are either on or fall below maturity level 3. Virtually all developing countries (to which Nigeria belongs) are in software maturity levels between 1 and 2. India happens to be one of the highest exporter of software and hence have software as one of its major sources of revenue [2, 6]. The Indian software industry attributed their success to strict adherence to the CMMI. The Nigerian software industry can experience the same monumental development following the same route other successful industries have been through.

## VI. CONCLUSION

To achieve the objective of this work, the Software Engineering Institute (SEI) Capability Maturity Model Integration (CMMI) for software process improvement was employed. The SEI Maturity Questionnaire (MQ) was the primary instrument used for eliciting data from respondents. Survey (using the MQ), and Case Study combined research methodologies were applied across thirty software organizations in Nigeria. The required data was successfully collected, verified, collated and evaluated. The Standard CMMI Appraisal Method for Process Improvement (SCAMPI) appraisal method was applied in the appraisal of the industry. The result of the appraisal was then summarized, indicating maturity level, capability levels, and project management practices based on the CMMI Key Process Areas (KPA).

The result revealed that the Nigerian software industry is very deficient in so many areas. This includes virtually all the Key Process Areas (KPA) in the SEI Maturity Questionnaire. The appraisal also revealed that the software process of the Nigerian software industry is at the maturity level 1, which is the very base level. While clamoring for a drastic improvement, this result should however not be so alarming as many industries in the world (even in developed countries) have not yet exceeded maturity level 2. The capability level for the identified key process areas were also identified to toggle between 0 and 1.

The scalability of the SEI CMMI model makes it adaptable to any kind and size of software development organization or industry. All that is required is the identification of a need to develop, grow, or mature the organizational software process. Once this need has truly been identified, the discipline required for climbing up the ladder of software process maturity will be imbibed.

## ACKNOWLEDGEMENT

We acknowledge all individuals and companies that have contributed in making this study possible. Due to issues of privacy as regarding the organizations and personnel involved, names will not be mentioned. We say a very big thank you to you all.

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## Biography

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# TAKING THE JOURNEY FROM LTE TO LTE-ADVANCED

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## *ABSTRACT*

*This paper addresses the main features of the transition from the Long Term Evolution standard (LTE) to its successor Long Term Evolution-Advanced (LTE-A). The specifications of the new release have taken several years and included thousands of temporary documents. The output, thus, would be tens of volumes of details. Turning this number of volumes into a single manuscript is a very useful resource for many researchers. One paper of this length must therefore choose its contents wisely if it has to do more than just scratching the surface of such a complex standard.*

## *KEYWORDS*

*Long Term Evolution Advanced (LTE-A), Multiple-Input-Multiple-Output (MIMO), Bandwidth Aggregation, Coordinated Multi-Point (CoMP) and Relaying*

## I. INTRODUCTION

Following the transition from Global System for Mobile Communications (GSM) to Universal Mobile Telecommunications System (UMTS) in wireless mobile systems [1], in 2009,the International Telecommunication Union (ITU) decided to come up with challenging requirements for its next 4th Generation (4G) standard, namely; International Mobile Telecommunications Advanced (IMT-Advanced) [2-5]. Not surprisingly, this upgrade aims at breaking new grounds in extremely demanding spectral efficiency needs that would definitely outperform their predecessors of legacy systems. Average downlink data rates of 100 Mbit/s in the wide area network and 1 Gbit/s for local access are being the most challenging ones [6].

Remarkably, the ITU is the key player in the whole wireless standardization process. It is the body behind the "G" in all new emerging standards, that is; the 2G, the 3G, and the forthcoming 4G [3], [5]. Interestingly, these are not standards as such, they are simply frameworks, and within those frameworks, several bodies submit different candidate technologies. Up until Dec.2010, it appeared there are only two candidate technologies for IMT-Advanced[1], i.e. LTE-A and its rival IEEE 802.16m standard [2], [7].

It is worth mentioning that IMT family members, i.e. 3G and 4G, both share the same spectrum; hence there is no 4G spectrum, there is IMT spectrum, and it is available for 3G and 4G technologies [8], [9]. Furthermore, Mobile Wimax and Ultra mobile broadband (UMB) share, to a certain level, the same radio-interface attributes for those of LTE given in Table 1. All of them, namely; mobile Wimax, UMB, and LTE, support flexible bandwidths, FDD/TDD duplexing, OFDMA in the downlink and MIMO schemes. However, there are a few differences among them. For instance, the uplink in LTE is based on SC-FDMA compared to OFDMA in Mobile Wimax and UMB. The performance of the three systems is therefore expected to be similar with minor differences [8], [10].

[1] ITU has recently redefined its 4G to include LTE, Wimax, and HSPA+. These standards were, for years, considered as pre-4G technologies and by no means meet the 4G targets previously stipulated by ITU [17].

**Table 1**. Main LTE air interface elements.

| | |
|---|---|
| Bandwidth | 1.25-20 MHz |
| Duplexing | FDD, TDD, half-duplex FDD |
| Mobility | 350 Km/h |
| Multiple access | Downlink:OFDMA<br>Uplink: SC-FDMA |
| MIMO | Downlink: 2x2, 4x2, 4x4<br>Uplink: 1x2, 1x4 |
| Peak data rate in 20 MHz | Downlink:173 and 326 Mb/s for 2x2 and 4x4 MIMO, respectively.<br><br>Uplink: 86 Mb/s with 1x2 antenna configuration |
| Modulation | QPSK, 16-QAM and 64-QAM |
| Channel Coding | Turbo code |
| Other Techniques | Channel sensitive scheduling, link adaptation, power control, ICIC and hubrid ARK |

## II. THE PATH TOWARDS LTE

In order to meet the growing traffic demands, extensive efforts have been made in the 3rd Generation Partnership Project (3GPP) to develop a new standard for the evolution of 3GPP's Universal Mobile Telephone System (UMTS) towards a packet-optimized system referred to as Long-Term Evolution (LTE) [11]. The project, which started in November 2004, features specifications for new radio-access technology revolutionized for higher data rates, low latency and greater spectral efficiency. The spectral efficiency target for the LTE system is 3 to 4 times higher than the current High Speed Packet Access (HSPA) system [11]. These challenging spectral efficiency targets required pushing the technology envelope by employing advanced air-interface techniques such as low Peak-to-Average Power Ratio (PAPR), orthogonal uplink multiple access based on Single-Carrier Frequency Division Multiple Access (SC-FDMA), multi-antenna technologies, inter-cell interference mitigation techniques, low latency channel structure and Single-Frequency Network (SFN) broadcast to determine LTE [12], see Table 1.

Remarkably, in the standards development phase, the proposals go through extensive scrutiny with multiple sources evaluating and simulating the proposed technologies from system performance improvement and implementation complexity perspective. Therefore, only the highest-quality proposals and ideas finally will be counted in the standard. The system supports flexible bandwidths, offered by Orthogonal Frequency Division Multiple Access (OFDMA) and SC-FDMA access schemes. In addition to Frequency Division Duplexing (FDD) and Time Division Duplexing (TDD), Half-Duplex FDD (HD-FDD) is allowed to support low cost User Equipment (UE) [12], [13]. Unlike FDD, in HD-FDD operation a UE is not required to transmit and receive at the same time, thus avoiding the need for a costly duplexer in the UE [8].

The system is primarily optimized for low speeds up to 15 km/h. However, the system specifications allow mobility support in excess of 350 km/h at the cost of some performance degradation [12]. The uplink access is based on SC-FDMA that promises increased uplink coverage due to low PAPR relative to OFDMA. The system supports downlink peak data rates of 326 Mb/s with “4 × 4”multiple-input multiple-output (MIMO) within 20 MHz bandwidth [11-14]. Since uplink MIMO is not employed in the first release of the LTE standard, the uplink peak data rates are limited to 86 Mb/s within 20 MHz bandwidth. Similar improvements are observed in cell-edge throughput while maintaining same-site locations as deployed for HSPA. In terms of latency, the LTE radio-interface

and network provide capabilities for less than 10 ms latency for the transmission of a packet from the network to the UE [15].

## III. THE PATH TOWARDS LTE-A

This section gives precise as well as concise overview of LTE-Advanced main features. Those were initially considered by 3GPP as solution proposals, and lately have been agreed upon as core features in LTE-A. They are: Bandwidth aggregation, Enhanced uplink multiple access, Higher order MIMO, Coordinated Multipoint (CoMP) and Relaying.

### 3.1. Bandwidth Aggregation

With a goal of 1 Gbit/s, it is clear that this will not be met out of existing channel bandwidths. At the moment, LTE supports up to 20 MHz, and it is understood that the ability to improve spectral efficiency much beyond the current LTE performances is very much unlikely, and therefore the only way to achieve that higher data rates is to increase the channel bandwidth. 40 and 100 MHz have been set as the lower and upper bandwidths limits for both LTE-Advanced and IMT- Advanced, respectively [6], [7], [16]**.** The problem with 100 MHz is that the spectrum is scarce, and 100 MHz of adjacent spectrum is simply not available in most cases. Hence, to solve this problem, ITU has decided to do bandwidth aggregation between different bands [4]. This means that spectrum from one band can be added to spectrum from another band. Figure1 shows a contiguous aggregation, where two 20 MHz channels have been taken and put side by side. In this case, this can be done by means of a single transceiver. But in the case where additional spectrum is not adjacent to the channel in use, then we are talking about spectrum aggregation among different bands which require multiple transceivers. The terminology used to describe this is called a component carrier, which is currently one of the six bandwidths defined for LTE. However, it is possible to aggregate different numbers of component carriers, but the maximum size of a component carrier will be limited to 110 resource blocks, which corresponds to 19.8 MHz for LTE [9].

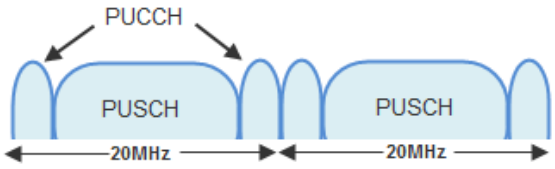



Figure 1. Contiguous aggregation of two 20 MHz uplink component carriers

Clearly, there are a lot of spectra around, namely; 22 FDD frequency bands for LTE as well as a number of bands for TDD [2], [6], [8], [10]. This means there are a lot of possibilities for aggregating different bands. However, the challenge is which bands should be picked considering the geography of the deployment.
To help with this problem, 3GPP has identified twelve scenarios which are most likely to be deployed [13], and the challenge here is to investigate the requirements for issues like spurious emissions, maximum power and all the issues that emanate from combining different radio frequencies into one device.

### 3.2. Enhanced Uplink Multiple Access

The next major feature is the enhancement in the uplink access scheme. LTE is based on SC-FDMA, that involves the flexible features inherent to Orthogonal Frequency Division Multiplexing (OFDM) plus the low PAPR of single carrier systems [10].
Figure 2 shows an example of various SC-FDMA schemes. An uplink 20 MHz bandwidth is shown. At the edge of this channel, there is the control channel (PUCCH), which operates one

resource block, or 180 KHz. Somewhere within the bandwidth, is the shared channel (PUSCH) which uses the SC-FDMA modulation. And there are three possibilities here; the first two graphs from the upper side are inherent to LTE. However, the new technique that has come in with LTE-Advanced is called clustered SC- FDMA, where the spectrum is not fully occupied as indicated at the bottom of figure 2. The reason is to provide more flexibility in the uplink when the channel is frequency selective. Notably, the problem with SC-FDMA is picking a contiguous block of allocation. Thus, if a channel displays a certain variation in performance across frequency, then, decision should be made about where to allocate the signal.

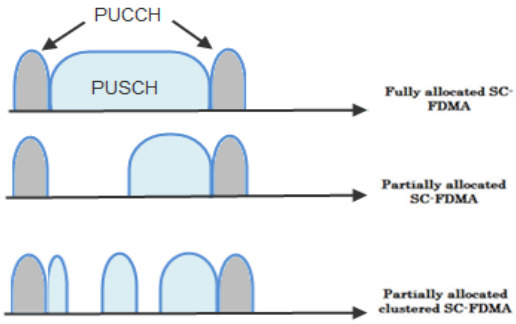



Figure 2 Various SC-FDMA schemes

The advantage of the clustered approach is that the same allocation in terms of bandwidth can be taken and split up into different slices within the overall channel bandwidth, and this is where the concept of clustering comes in. It has a slight degradation on PAPR performance, but it is significantly better than the alternative, which is to use pure OFDM, as in other systems like Wimax [7]. Pure OFDM allows the highest flexibility in the uplink, but it also suffers from very high PAPR. So the concept of clustered SC-FDMA is an excellent trade-off between OFDM flexibility and low PAPR of the original SC-FDMA.

### 3.3. Multiple-Input Multiple-Output (MIMO)

The next major feature of LTE-Advanced is higher order MIMO transmission. Historically, the following limits were established by Release-8 LTE [12]: the downlink has a maximum of four layers MIMO of transmission, while the uplink has a maximum of one - for -one mobile. So this together with the fact that the UE has received diversity means we could support “4x2” MIMO in the downlink and in the uplink there is no MIMO as such from a single mobile device. Now with LTE-Advanced, the situation is considerably different. There is general consensus of supporting up to eight streams in the downlink with eight receivers in the UE. This will give a possibility of “8x8” MIMO in the downlink. And in the uplink, the UE is capable of supporting up to four transmitters, thereby offering a possibility of up to “4x4” transmissions. The additional antennas can also be used, say, for beamforming and the overall goal is to increase the data rates coverage capacity of the cell.

### 3.4. Coordinated Multi-Point (CoMP)

In traditional MIMO systems, shown in figure 3, there is a transmitting unit in which a base station with more than one antenna going through a channel to a receiving unit having more than one receiver. However, with coordinated multi-point, the difference is that at the transmitting end the two entities are not necessarily physically located, although they are connected with some form of a high-speed data connection. Accordingly, in the downlink, this allows for coordinated scheduling and beamforming from two different locations. This implies that the system is not fully utilized as the data required to be transmitted to the UE only needs to be present at one of the serving cells. That is, some amount of partial coordination has taken place. However, if we go for coherent combination, also known as cooperative MIMO, then it is possible to do more advanced transmission whereby the data which is being transmitted to the UE is coming from

both locations, and it is coordinated at the UE with pre-coding techniques in order to maximize the signal-to-noise ratio (SNR).The challenge of this approach is that there is need to have a high-speed symbol level data communication between both transmitting units, as indicated by the vertical black arrow in figure3.

Within LTE, there is the concept of the "X2" interface [11], which is a mesh-based interface between the base stations. By this mechanism, this physical link is the one to be used for sharing the base band data. One way of looking into coherent combining is soft combining or soft handover; which is widely applied in Code Division Multiple Access (CDMA) systems, except that the data being transmitted is not identical from both base stations. They are two different data streams which are then coordinated in such a way to allow the mobile device to receive both simultaneously. In the uplink, the use of coordination between the base stations is less advanced because when there are more than one device in different places, there will be no realistic mechanism for sharing data between the two transmitting devices. Therefore, in the uplink, the concept is more limited to the earlier version of the downlink, which is to coordinate on scheduling.

### 3.5. Relaying

A relaying its simplest form is otherwise referred to as a repeater; a device which receives the transmissions within the channel of interest at its input, amplifies them and then retransmits to the local area. It is also used for improving the coverage, although with no substantial capacity improvement [16]. Recently, the concept of relaying is to take this a stage further by decoding the transmissions which is fed into the cell of interest and instead of only retransmitting the amplified inputs to the rest of the cell or the targeted area, it would selectively retransmit a portion of the transmission. Relaying is possible at different layers in the protocol. The most advanced one being layer three relaying, in which the relay node would pick out only the traffic for the mobile device within its vicinity and retransmit the signal. This is carried out without transmitting any other signals for mobile devices which may be in the macrocell but are not associated with the relay node. Therefore, this makes a kind of selective repeater where the problem of adding interference to the network is reduced on the downlink. On the other hand, in the uplink the relay node is not connected to the network via some form of cabled backhaul, which is the case with the macro cell. Hence, it is possible to deploy a relay node at some distance from the macrocell or serving node without having to deal with any cabling problems in order to get the backhaul.

For instance, in a situation where coverage is sought-after, say, some remote locations down a valley, it is possible to employ a multi-hop relay whereby a signal will be sent from the serving cell to the relay node down to the UE. Accordingly, the signal coming from the UE would be transmitted up to the relay node, which is now in the form of backhaul, which would transmit this signal back to the base station using the same channel as used for the downlink in a TDD system, or the complementary channel in an FDD system [9]. The reason it is possible to do this in an OFDM system is that it is possible to split the channel into different parts. No need to use the whole channel for all transmissions. Thereby, a cell could allocate half of the uplink resource blocks to relay backhaul traffic and the other half to UEs in the macro network.

This means the OFDM provides the flexibility to do this form of in-channel backhaul, which otherwise would be impossible in a CDMA system unless a new channel is introduced.

There are different ways in which relaying could be used, but they basically fall into a couple of major areas, one is to do selective improvements to coverage. Also there are other aspects of relaying which would appear to provide throughput advantages within the macrocell. In fact, a lot of work still needs to be done on relaying and there is consensus on how this particular feature will be deployed. In some ways, we could look upon relaying as a more advanced form of repeating where we may have one or two of these types of devices in a macrocell. However, there are other schools of thought which suggest that a macrocell might support hundreds of relay nodes in order to provide much higher level of capacity in such a way that is similar to the concept of Femtocells, except that the whole system will be coordinated from the centre.

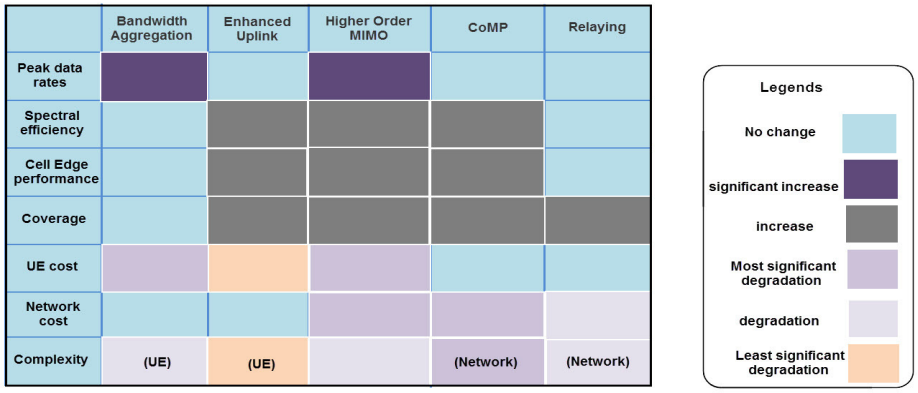
In general, there is a fact that we are looking at many different types of cells now, from Macro to Pico to Femtocells and recently these relay nodes; and what is happening within the radio environment is a much higher level of hierarchy within the scope of the different base stations. This creates a hierarchical, rather than a homogenous, network where each cell is at the same level in the hierarchy and they are all one big sort of mosaic of coverage, thus leading to the concept of a hierarchical network where we have umbrella types of coverage having much smaller coverage areas with different techniques. This, however, presents some real challenges to the whole radio management. And the subject of radio resource management is a major item which continues to develop as the radio environment becomes more complex.

Heterogeneous network is not an item as such in LTE-Advanced, but the fact that Femtocells will be coming along soon in these relay nodes means that there will be a substantial need to research and develop mechanisms to enable these more complex radio networks to function efficiently. It is worth mentioning here that the key difference between Femtocells and traditional cells is the backhaul and the fact that these devices are not centrally managed. However, most people would tend to think of Femtocells as being smaller versions of Picocells. But if we think of it in terms of backhauling and planning, they are, in fact, extremely different in the way they interact with the network. Also, there are other factors such as cost and the performance expectations, and so on. Femtocells are one of the elements in the heterogeneous network which are being developed in the standards and by the time LTE-Advanced comes along; they will definitely be part of the landscape.

## IV. PROS AND CONS OF LTE-ADVANCED DEPLOYMENT

In order to summarize the overall picture of LTE-Advanced, Table 2 shows a list of attributes of the five main features of LTE-A. The table provides answers to the following arising questions: what do these features provide in terms of performance and what is the cost of deploying them?

**Table 2**. Pros and Cons of LTE-Advanced system deployments.




Beginning with bandwidth aggregation, which is a very obvious key player here, it is primarily aimed at peak data rates with no substantial change in spectral efficiency, although we may get some benefits from the fact that a larger instantaneous channel is available to multiple users. Cell edge performance as well as coverage would not change. However, when it comes to the cost, particularly in the UE, there would be substantial issue in bandwidth aggregation, if it is non-contiguous and the mobile device had to support more than one transceiver, or in the worst case, up to five different transceivers. Clearly, this translates to a significant cost increase. On the network side, it is unlikely that there would be any significant cost change since the base station is typically stand-alone in terms of different frequency bands. Whereas there would be an increase in overall network complexity, and this is mentioned here, primarily on the UE side. Looking at enhanced uplink, the clustered SC-FDMA, there is no appreciable change in peak data rates. This is because if the peak data rate is required, a whole channel has to be allocated, and

therefore clustering has no meaning. But the intention behind this technique is to take the advantage of the frequency- selective channel; thus, offering a benefit of spectral efficiency, although it is not a major change over what we have today. Similarly, there may be some advantages in cell edge performance. However, with regard to overall coverage, it is hard to know whether or not there would be a coverage support.

In terms of UE cost, it is unlikely that it would be significant. Concerning network cost, it is uncertain to have any impact and some minor increase in UE complexity. Considering the higher order MIMO, the expectations for peak data rates are driven by some of these "8x8" downlink or "4x4" uplink antenna configurations. Also, there will be benefits in terms of spectral efficiency, cell edge performance and coverage through the different techniques. MIMO is not a single subject. Notably, in basic LTE, there are seven different transmission modes in the downlink, all varying from traditional type up to closed loop MIMO. With the introduction of more antennas in LTE-Advanced, there are many different ways we could use these antennas depending on the particular radio environment. Hence, it is impractical to attribute a particular benefit to one particular scenario. It very much depends on whether the system is developed to take advantage of a particular scenario. But in general, higher order MIMO should lead to increases in the average in cell edge and coverage performance.

However, when it comes to the cost, clearly in the mobile device if we have to implement multiple transceivers in the UE to support these different streams, there is a big impact in terms of the product cost. Going from one to two and to four transmitters is a big issue. It is interesting to note that LTE, in its basic form, does not support uplink MIMO. It is a single transceiver approach, while LTE-Advanced will be taking advantage of up to four transceivers. Accordingly, there could be a big impact on the cost of the mobile device. On the network side, there would be an increase, though it may not be as noticeable as on the mobile side, because most networks on the base station side already have probably two antennas at the moment and some maybe four. But certainly there would be an increase. And then in the overall complexity of the system, there would be an increase as well. Regarding the coordinated multi-point, it is not likely to have any impact on peak rates, but again, similar to MIMO, there might be expectations on spectral efficiency improvement, cell edge performance and coverage. UE cost, unlikely to have any impact at all, but on the network side, CoMP could be a big issue, and that is primarily because of the need for the high speed backhaul between the different base stations. With regard to complexity, certainly, there will be a major increase in complexity in terms of real time management of all these coordination among the base stations.

Finally, considering relaying, it is unlikely to have any effect on peak rates or efficiency, but some improvements in cell edge and coverage are possible; as those are the main areas that are being targeted by relaying. And no impact, obviously, on the cost of UE, as the UE should view a relay network in the same way as it views the standard network. But, there would be an increase, obviously, in network cost; because the relay nodes need to be deployed. Not the least is the issue of network complexity which is higher than standard networks due to the management of the relay nodes.

## V. CONCLUSIONS

LTE-Advanced is 3GPP's submission to the ITU radio communications sector; IMT-Advanced program. It is important to differentiate between IMT-Advanced, which is the ITU's family of standards, and LTE-Advanced, which is the 3GPP candidate submission. LTE-Advanced clearly is an evolution of LTE, and it is approximately two years behind. In terms of standardization, however, trying to predict the deployment date for LTE-Advanced is much harder, because we are trying to extrapolate from something that is already somewhere in the future. However, IMT-Advanced deployment is still several years away whereas deployment of HSPA Evolution (HSPA+) and LTE is already ongoing.

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# DESIGN & DEVELOPMENT OF AUTONOMOUS SYSTEM TO BUILD 3D MODEL FOR UNDERWATER OBJECTS USING STEREO VISION TECHNIQUE

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## *ABSTRACT*

*The objective of the paper was to design and development of a stereo vision system to build 3D model for underwater objects. The developed algorithm first enhance the underwater image quality then construct 3D model by using iterative closest point (ICP) algorithm. From the enhanced images feature points are extracted and feature based matching was done between these pair of images. Epipolar geometry was constructed to remove the outliers between matched points and to recover the geometrical relation between cameras. Then stereo images were rectified and dense matched. Then 3D point was estimated using linear triangulation. After the registration of multi-view range images, a 3D model was constructed using a Linear Triangulation technique.*

***KEYWORDS:*** *Underwater image, ICP algorithm, 3D model*

## I. INTRODUCTION

Generating a complete 3D model of an object has been a topic of much interest in recent computer vision and computer graphics research. Many computer vision techniques have been investigated to generate complete 3D models. Underwater 3D imagery generation is still challenge due to their many unconventional parameters such as refractive index of water, light illumination, uneven background, etc. Presently there are two major approaches. First is based on merging multi-view range images into a 3D model [1-2]. The second approach is based on processing photographic images using a volumetric reconstruction technique, such as voxel coloring and shape-from-silhouettes [3]. Multi-view 3D modeling has been done by many active or passive ranging techniques. Laser range imaging and structured light techniques are the most common active techniques. These techniques project special light patterns onto the surface of a real object to measure the depth to the surface by a simple triangulation technique [4, 7]. Even though active methods are fast and accurate, they are more expensive. However, relatively less research has been done using passive techniques, such as stereo image analysis. This is mainly due to the inherent problems (e.g., mismatching and occlusion) of stereo matching. The quality of underwater images are poor as they suffered from strong attenuation and scattering of light. To overcome these problems this paper has been contributed to first enhance underwater images and applying passive method to build 3-D Model.

The work first employs image enhancing technique to reduce the effect of scattering of light and attenuation and also improves the contrast of the images. In order to remove the mismatches between pair of stereo images, this methodology computes epipolar geometry and also performs dense matching to get more features by employing rectification process. Multi-view range images are obtained using stereo cameras and turntable. The developed computer vision system has two inexpensive still cameras to capture stereo images of an object. The cameras are calibrated by a projective calibration technique. Multi-view range images are obtained by changing the viewing direction to the object. We also employ a turntable stage to rotate the object and to obtain multiple range images. Multiple range images are then registered and integrated into a single 3D model. In order to register range images automatically, we employ Iterative Closest Point (ICP) algorithm to integrate multiple range images into a single mesh model using volumetric integration technique.

Error analysis on real objects shows the accuracy of our 3D model reconstruction. Section 2 presents the problem and solution of the images in underwater conditions. Section 3 presents range image aquition methodology, Section 4 presents a 3D modeling technique of merging multi-view range images. Finally, section 5 concludes the paper.

## II. PROBLEMS IN UNDERWATER & SOLUTION

To capture the images in underwater conditions, two underwater cameras with lights enabled were mounted on a stand. Underwater imaging faces a major problem of light attenuation which limits the visibility distance and degrades the quality of the images such as blurring or lacking of structure in the regions of interest. The developed method uses efficient image enhancement algorithm. We implemented the program with Matlab. The method is comprised of three main steps:

- **Homomorphic filtering:** The homomorphic filter simultaneously increases the contrast and normalizes the brightness across the image.
- **Contrast limited adaptive histogram equalization (CLAHE):** The histogram equalization is used to enhance the contrast of the image.
- **Adaptive Noise-Removal Filtering:** A Weiner filter is implemented to remove the noise produced by equalization step.

## III. RANGE IMAGE ACQUITION AND CALIBRATION

We employ a projective camera model to calibrate our stereo camera (MINI MC-1). Calibration of the projective camera model can be considered as an estimation of a projective transformation matrix from the world coordinate system (WCS) to the camera's coordinate system (CCS). We employ a turntable to take range images while stereo cameras are stable. We set up an aquarium to take images in underwater condition. We mount MC-mini underwater cameras on a stable stand and keep an Model on a turntable. The lab setup to do experiment is as shown in fig. 2. Our system makes use of camera calibration, so we employ Tzai stereo camera calibration model to calibrate our stereo cameras. We use 8X9 check board (as shown in Fig. 1) to calibrate the cameras.

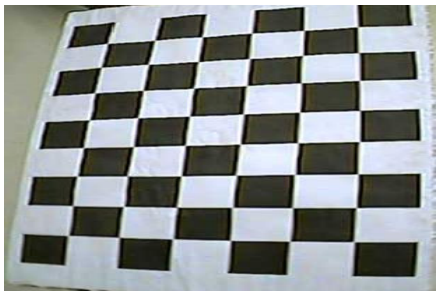

Fig.1 Check board for camera calibration

We got internal camera parameters (K1 & K2) as a result of calibration process. These internal camera parameters are useful in estimating metric 3-D reconstruction so that we can get the approximate dimensions of the object.

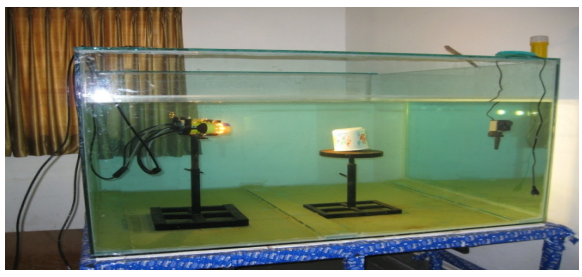

Fig. 2 Lab setup for the experimentation

# IV. 3-D MODELING METHODOLOGY

This section describes the complete overview of the developed system flow chart. The methodology is as shown in the fig. 3.

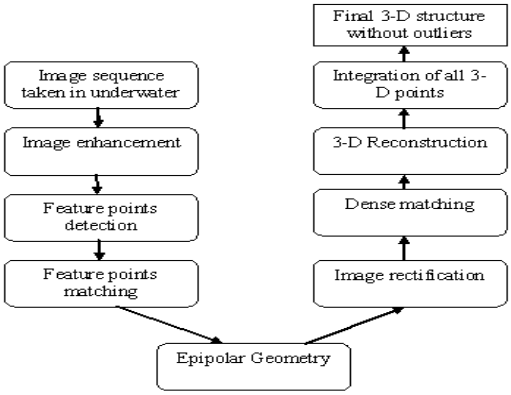


Fig.3: Developed 3-D Modeling methodology

## 4.1 Extraction of 2D feature points and Correspondence matching

The work is with large scaled underwater scenes, where illumination is frequently changing and to find a set of stable features which are useful for later stage of estimating 3-D points. Therefore, a feature based approach, namely Scale Invariant Feature Transform (SIFT) which is developed in OpenCV library is used in this work. Images are represented by a set of SIFT feature as shown in Fig 3. Although, there are some newly derived techniques that can return faster or more efficient result, the developed method chooses the SIFT, because of its invariance to image translation, scaling, partial invariance to illumination changes. Key Points after getting from SIFT are then compared between every consecutive pair of images and the matching points are used to calculate the epipolar geometry between cameras. The epipolar geometry is used to further discard false matches. The feature based approaches look for features in images that are robust under the change of view points, illumination, and occlusion. The features used can be edge element, corners, line segments, gradients, depending on the method.

## 4.2 Computation of Epipolar geometry

The epipolar geometry provides us with a constraint to reduce the complexity of correspondence matching. Instead of searching the whole image or region for a matching element, we only have to search along a line. Even when the matching is already found by other methods, epipolar geometry can be applied to verify the correct matches and remove outliers. The epipolar geometry is used for two purposes:

a) To remove false matches from SIFT matching and
b) To recover the geometrical transformation between 2 cameras from the computation of the fundamental matrix.

## 4.3 Fundamental matrix estimation

To estimate the fundamental matrix (F), Random Sampling Consensus (RANSAC) was used. The library of OpenCV provides functions to estimate Fundamental matrix using Lmeds and RANSAC. To estimate the fundamental matrix, equation (1) can be deduced and rewriting it in the following way

$$Uf = 0 \quad (1)$$

$$f = \left(F_{11}, F_{12}, F_{13}, F_{21}, F_{22}, F_{23}, F_{31}, F_{32}, F_{33}\right)^T \quad (2)$$

$$U = \begin{pmatrix} {}^{I}X_1 {}^{I}X'_1 & {}^{I}X_1 {}^{I}Y'_1 & {}^{I}X_1 & {}^{I}Y_1 {}^{I}X'_1 & {}^{I}Y_1 {}^{I}X'_1 & {}^{I}Y_1 & {}^{I}X'_1 & {}^{I}Y'_1 & 1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ {}^{I}X_n {}^{I}X'_n & {}^{I}X_n {}^{I}Y'_n & {}^{I}X_n & {}^{I}Y_n {}^{I}X'_n & {}^{I}Y_n {}^{I}X'_n & {}^{I}Y_n & {}^{I}X'_n & {}^{I}Y'_n & 1 \end{pmatrix} \quad (3)$$

### 4.4 Rectification & dense matching

Both stereo pairs are rectified - Rectification transforms a stereo image pairs in such a way that epipolar lines became horizontal, using the algorithm presented in [Isgrò, 1999]. This step allows an easier dense matching process. As our developed system has constructed 3-D structure of the object from multiple views, if there is more number of feature points then 3-D structure will be more accurate. So, to get more number of feature points we employ dense matching process. Depth information about the objects present in a rectified pair of images: far objects will have zero disparity and the closest objects will have maximum disparity instead. Figure 4 shows the corresponding matching features removing outliers.

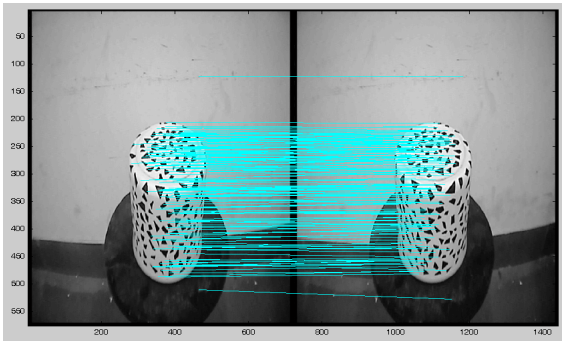

Fig. 4 Corresponding matching without outliers

After the matching image points have been discovered using dense matching, the next step is to compute the correspondent 3D object points. The method of finding the position of a third point knowing the geometry of two other known reference points is called triangulation. Since the two matching points are just the projected images of a 3D object point, then the 3D point is the intersection between two optical rays passing through the two camera centers and two matching image points. The matching points are converted into metric representation using the intrinsic parameters of camera calculated as a result of the camera calibration process. By projecting the points into 3D space and finding intersections of the visual rays, location of object points can be estimated. This process is referred as triangulation. After removing outliers, the final result is a 3D point cloud which can be interpolated to construct the 3D model of the object.

### 4.5 Outliers removal

Once the set of 3D points has been computed, the final step is to remove the isolated points, which are the points with less than 2 neighbors. A point is considered a neighbor of another if it is within a sphere of a given radius centered at that point. This final process is an effective procedure to detect any remaining outliers as outliers generally generate isolated 3D points as shown in Fig. 5.

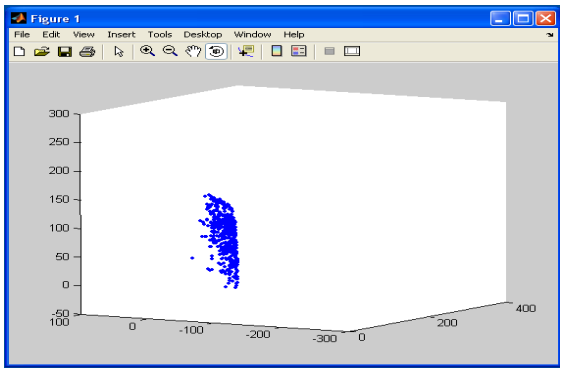


Fig. 5 Partial 3-D reconstruction of two images

We set some threshold to remove the 3-D outlier points. If any point is not having any neighbor within that threshold then that point is considered as outlier and it has to be removed from the 3-D point set. Otherwise the 3-D model is not accurate. The remaining 3D points are stored as a partial reconstruction of the surface. In this manner we calculate the remaining 3D points for the rest of the object views, and using Iterative Closest Point (ICP) algorithm, those 3D points are registered to the common coordinate system. Then those point clouds are interpolated to construct the surface. Once we get the surface of the object then that 3D model can be texture mapped so that the final 3D model of the object looks like actual object.

### 4.6 Integration of all the 3-D points

Using the above methodology, all the partial 3-D structures of the object are obtained and integrated into the common coordinate system using Iterative Closest Point (ICP) algorithm. Thus we got proper 3-D point cloud of all the views. Once we get point cloud then those points were interpolated and surface was put on the point cloud to get the 3-D model of object as shown in Fig. 6.

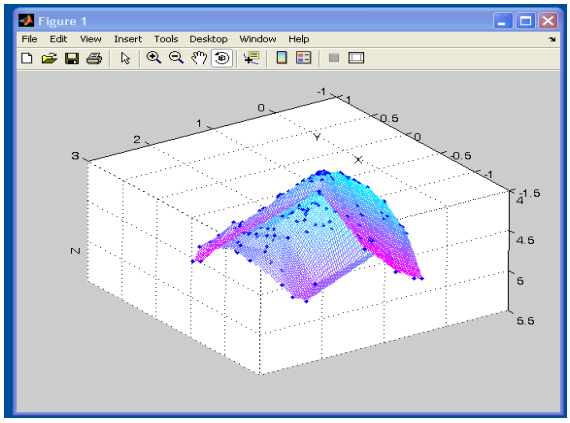


Fig 6 3-D model with surface from 4 views

### 4.7 Texture Mapping

After obtaining the 3-D model of an object, texture of the original object has been mapped onto the 3-D model so that it looks same as the object. The result of the texture mapped 3-D model is as shown in fig. 7

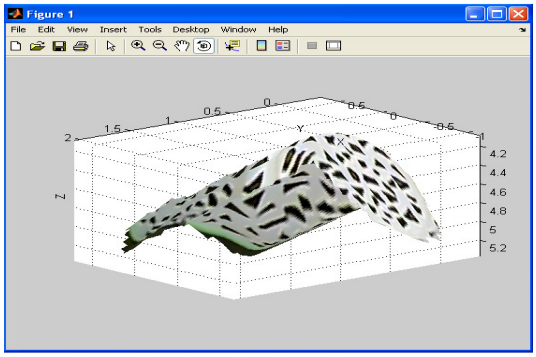


Fig 7 3-D model with texture mapped

## V. CONCLUSION

The system consists of an inexpensive underwater stereo camera, a turn table and personal computer. Developed autonomous System to build 3-D Model of underwater objects is easy to use and robust under illumination changes as this system extracts SIFT features rather than intensity values of the images.

The images are enhanced and feature points of those images are extracted and matched between pair of stereo images. Final 3D reconstruction is optimized and improved in a post processing stage. Geometrical 3Dconstruction obtained with natural images collected during the experiment out to be very efficient and promising. The estimation of dimensions of the object is also nearly accurate.

## ACKNOWLEDGMENT

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# ANALYSIS AND CONTROL OF DOUBLE-INPUT INTEGRATED BUCK-BUCK-BOOST CONVERTER FOR HYBRID ELECTRIC VEHICLES

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## *ABSTRACT*

*The energy storage unit is one of the most important aspects in structure of hybrid electrical vehicles, since it directly impacts the performance, fuel economy, cost, and weight of the vehicle. In order to fully utilize the advantages of each energy storage device, employment of multi-input power converters is inevitable. In this paper analysis and control of double input integrated buck-buck-boost converter(DIIBBBC) is presented and operating modes are analyzed . In order to have simple control strategy as well as simpler compensator design a single loop control scheme, voltage-mode and current-limit control, are proposed here for the power distribution. Closed loop converter performance of this converter is simulated in MATLAB/Simulink and results show the performance of the converter.*

***KEYWORDS:*** *Integrated buck-buck-boost converter, Hybrid electrical vehicles, Multi-input power converters.*

## I. INTRODUCTION

Ultracapacitors have been proposed to be utilized in the electrical distribution system of conventional and hybrid vehicles to serve applications like local energy cache, voltage smoothing, pseudo 42V architecture, and service life of batteries extension [1]. However, the high specific power of ultracapacitors is the major reason of them being used as intermediate energy storage unit during acceleration, hill climbing, and regenerative braking. An energy storage unit comprising both batteries and ultracapacitors have been choice for the future vehicles. The basic idea is to realize advantages of both batteries and ultra capacitors while keeping the weight of the entire energy storage unit minimized through an appropriate matching [2].

Several structures for combining batteries and ultracapacitors have been introduced in the literature [3]. However in these the power conversion efficiency is major challenge for the power supply designer. To meet these concerns multi-input converters with different topology combinations are coming up in the recent days [5]. Although there are several different types of switch-mode dc-dc converters (SMDC), belongs to buck, boost and buck-boost topologies, have been developed and reported in the literature to meet variety of application specific demands. but an integrated converter with buck and buck-boost feature is more suitable for this application. In view of this a double input integrated buck-buck-boost converter (DIIBBBC) and its control features are analyzed in this paper. In the following, Section 2 presents the operating modes of the DIIBBBC. In Section 3 the analysis of the DIIBBBC is expounded in state space model. Section 4 shows the Control Strategies for the DIIBBBC. Section 5 shows the MATLAB/simulation of DIIBBBC and the Simulation results. Finally, conclusions are provided in Section 6.

## II. OPERATION OF THE DIIBBBC

The circuit diagram of proposed DIIBBBC, shown in Figure. 1. It consists of two input voltage sources $V_{HI}$ and $V_{LO}$, and an output voltage $V_O$ .Power switches $M_{HI}$ and $M_{LO}$ are connected to the high voltage source $V_{HI}$ and the low voltage source $V_{LO}$, respectively. When the power switches are turned off, power diodes $D_{HI}$ and $D_{LO}$ will provide the by-pass path for the inductor current to flow continuously. By applying the PWM control scheme to the power switches $M_{HI}$ and $M_{LO}$, the proposed double-input DCDC converter can draw power from two voltage sources individually or simultaneously or singly.

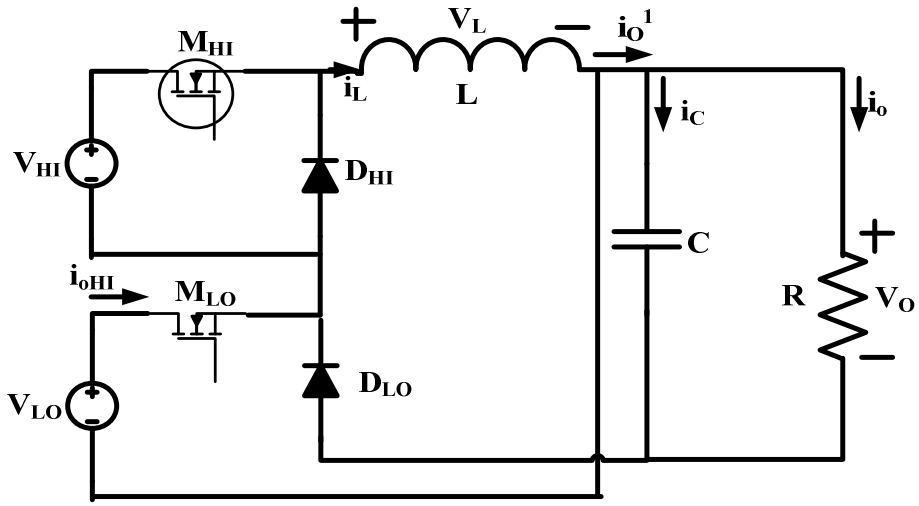



Figure 1. The proposed DIIBBBC

There are four different operation modes which can be explained as follows.

**Mode I** *($M_{HI}$* : on *& $M_{LO}$ :off)*
In Mode I, the power switch $M_{HI}$ is turn on and $M_{LO}$ is turn off. Because of the conduction of $M_{HI}$, power diode $D_{HI}$ is reverse biased and can be treated as an open circuit. On the other hand, power switch $M_{LO}$ for the low voltage source $V_{LO}$ is turned off and the power diode $D_{LO}$ will provide a by-pass path for inductor current $i_L$. The equivalent circuit of Mode I is shown in Figure 2(a). In this mode, the high voltage source will charge the energy storage components, inductor L and capacitor C, as well as provide the electric energy for the load.

**Mode II** *($M_{HI}$* : off *& $M_{LO}$ : on)*
In Mode II, the power switch $M_{HI}$ is tumed off and $M_{LO}$ is tumed on. Also, the power diode $D_{HI}$ is turned on as a short circuit and $D_{LO}$ is turned off as an open circuit. Figure.2(b) shows the equivalent circuit for Mode 11. During this operation mode, the low voltage source, $V_{LO}$ will charge the inductor L, while the demanded load is provided by the output capacitor C.

**Mode III** *($M_{HI}$* : off *& $M_{LO}$ :off)*
Both of the power switches $M_{HI}$ and $M_{LO}$ are turned off in Mode 111. Power diodes $D_{HI}$ and $D_{LO}$ will provide the current path for the inductor current. The equivalent circuit for Mode III is shown in Figure. 2(c). Both of the voltage sources $V_{Hl}$ and $V_{LO}$ are disconnected from the proposed double-input converter. The electric energy stored in L and *C* will be released into the load.

**Mode IV** *($M_{HI}$* : on *& $M_{LO}$ :on)*
In Mode *IV,* both of $M_{Hl}$ and $M_{LO}$ are turned on and $D_{HI}$ and $D_{LO}$ are turned off with reverse biased voltages. Two input voltage sources $V_{Hl}$ and $V_{LO}$ are connected in series to charge the inductor. L. The demanded power for the load is now provided by the capacitor *C.* In this operation mode, both of the

high now voltage sources will transfer electric energy into the proposed double-input DC-DC converter, simultaneously. The equivalent circuit for Mode IV is shown in Figure. 2(d).

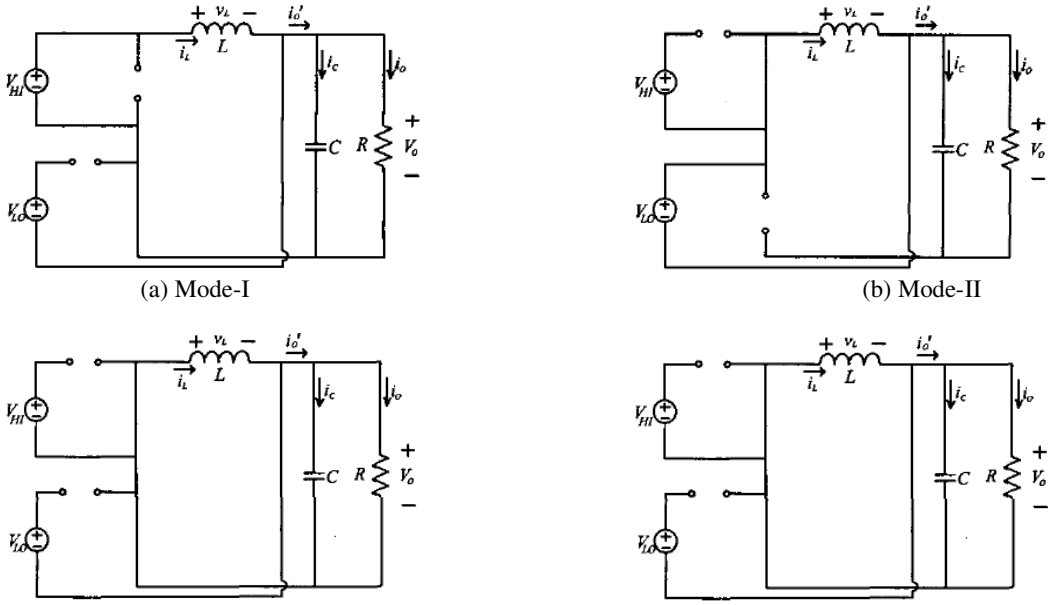



Figure.2 operating modes of proposed DIIBBBC

Theoretically, the switching frequency of $M_{HI}$ and $M_{LO}$ can be different. However, in order to reduce the electromagnetic interference (EMI) and facilitate the filter design, $M_{HI}$ and $M_{LO}$ should he operated with the same switching frequency, practically .For the same switching frequency, $M_{HI}$ and $M_{LO}$ can be synchronized by the same turn-on transition with different turn-off moment, or the same turn-off transition with different turn-on moment. Although either way can achieve the synchronization of the switching control, only the latter one with turn-off synchronization will be introduced in this paper for further explanations. Figure.3. Shows the typical voltage and current waveforms for key components of the proposed DIIBBBC under turn-off synchronization.

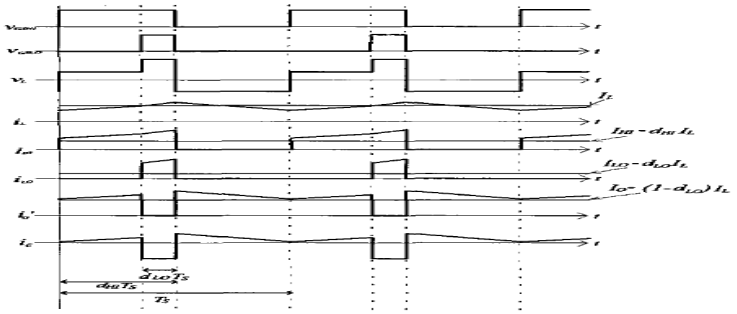


Figure 3. The typical voltage and current waveforms for key components o f the proposedDIIBBBC

## III. STATE SPACE MODELLING OF DIIBBBC

In CICM the TIBBC goes through three topological stages in each switching period and it's power stage dynamics can be described by a set of state-space equations [10] given by:

$$x = A_K x = B_K u$$
$$v_0 = C_k x \qquad (1)$$

where $x = [\ i_L \quad v_c\ ^T\ ]$ and $u = [v_g]$, k=1,2,3 and 4 for mode-1, mode-2, mode -3 and 4, respectively. Here the circuit operation depends on the type of controlling signal used for switching devices $S_1$ and $S_2$. In any case for proper functioning of the integrated converter, the gate control signals for the switching devices needs to be synchronized either in the form of trailing or leading-edge modulated pulses. Further, the operating modes depends on the duty ratio's of the switching devices, $d_1<d_2$ or d1> d2, and in any case only three modes will repeat in one switching cycle. Applying the state-space averaging analysis and upon simplification results the average model $\dot{x} = A\ x + B\ u$ where A=($A_1d_1+A_2d_2+A_3d_3$), B=($B_1d_1+B_2d_2+B_3d_3$) and these matrices are:

$$A_1=\begin{bmatrix} -\frac{r_L}{L}-\frac{R}{(R+r_c)} & -\frac{R}{(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix};B_1=\begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \tag{2}$$

$$A_2=\begin{bmatrix} \frac{r_L}{L} & 0 \\ 0 & -\frac{1}{C(R+r_c)} \end{bmatrix};B_2=\begin{bmatrix} \frac{1}{L} & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \tag{3}$$

$$A_3=\begin{bmatrix} -\frac{r_L}{L}-\frac{r_cR}{(R+r_c)} & -\frac{R}{(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix};B_3=\begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \tag{4}$$

$$A_4=\begin{bmatrix} \frac{r_L}{L} & 0 \\ 0 & -\frac{1}{C(R+r_c)} \end{bmatrix};B_4=\begin{bmatrix} 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \tag{5}$$

$$C_1=C_3=\begin{bmatrix} \frac{r_cR}{(R+r_c)} & \frac{R}{(R+r_c)} \end{bmatrix};C_2=C_4\begin{bmatrix} 0 & \frac{R}{(R+r_c)} \end{bmatrix} \tag{6}$$

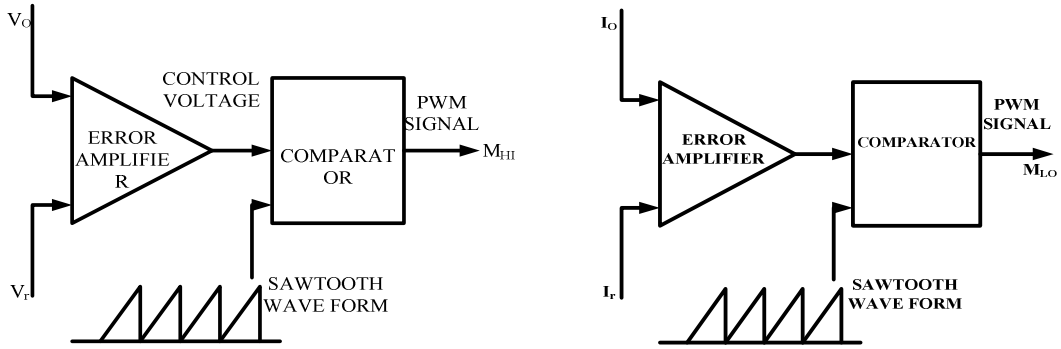
In this DIIBBBC the diodes will be the integral part of both buck and buck-boost converters, while the switching devices are unique to the individual converters. Load and it's filtering capacitor are common to both the converters. Buck converter is formed by: S1, D1, D2, L, R; while Buck-boost converter is formed by: S2, D1, D2, L, R. The steady-state load voltage can easily be established, either by employing volt-sec balance or through state-space model steady-state solution [x] =$A^{-1}$BU, as

$$V_o = \frac{d_2}{(1-d)_1} V_h + \frac{d_1}{(1-d_1)} V_l \tag{7}$$

## IV. CONTROL STRATEGIES FOR THE DIIBBBC

In this paper for the DIIBBBC two inter dependent single-loop control schemes are proposed. This structure is capable of maintaining the load voltage regulation while ensuring the load distribution on

the individual sources. The control schemes can be interchangeable from one to other depending on their power supplying capacity [10]. To illustrate the control principle, current control-loop for low voltage source (LVS), voltage control-loop for high voltage source (HVS) is shown in Figure. 4.




(a) Voltage Control (b) Current Control

Figure 4. Control of Multi-input Buck-Boost Converter.

## V. SIMULATION AND RESULTS

To verify the developed modelling and controller design, a 200 W DIIBBBC system was designed to supply a constant dc bus/ load voltage of 48V from a two different dc sources: (i) high voltage power source: 60 V, (ii) low voltage power source: 30 V. The switching frequency of 50 kHz is used for driving both the switching devices. In order to conform the controller design analysis simulation studies has been carried out on The DIIBBBC. MATLAB/Simulink is used for this purpose. Figure 5 shows the Simulink model of proposed DIIBBBC system .The output voltage ,current and power waveforms are shown in figure 6,figure 7,figure 8,The Results of dynamic behaviour of the proposed converter is shown Figure 9, Figure 10and Figure 11.The output voltage which does not affect due to the step transient as shown in Figure 9.

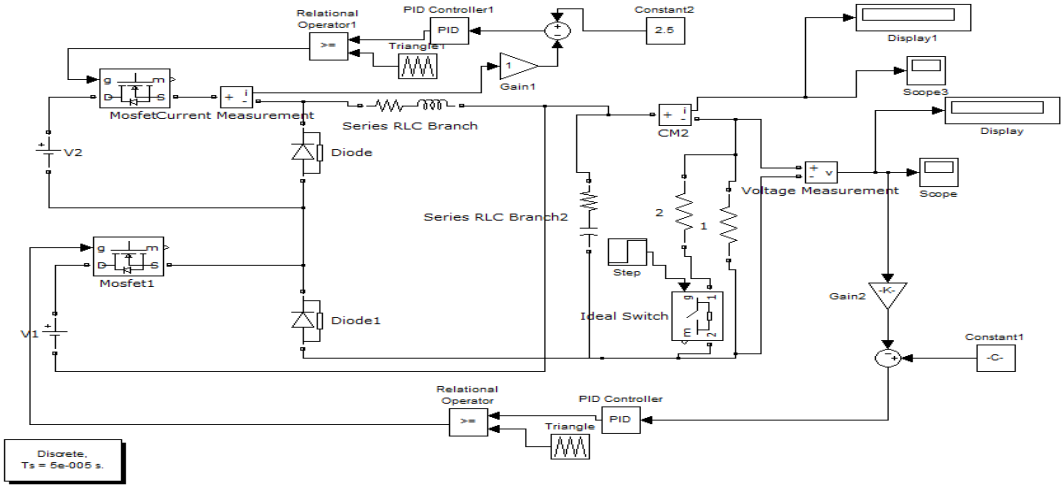



Figure 5.TheMATLAB/simulink model of proposed DIIBBBC

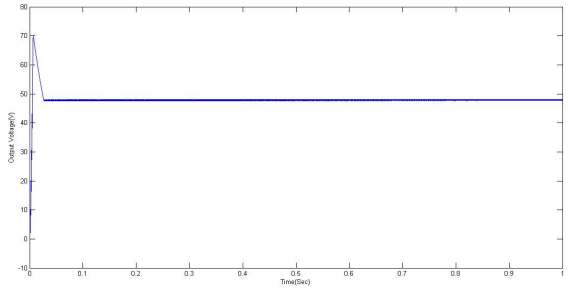


Figure 6. Output Voltage(V)

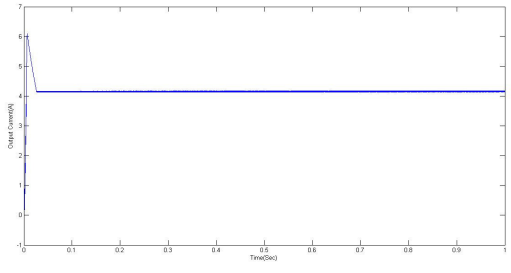


Figure 7. Output Current(A)

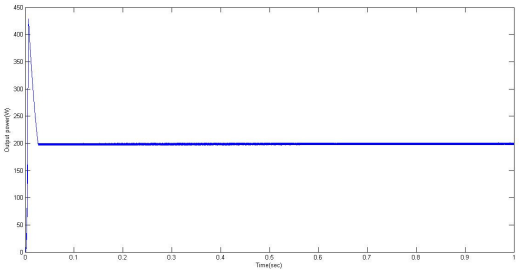


Figure 8. Output power(W)

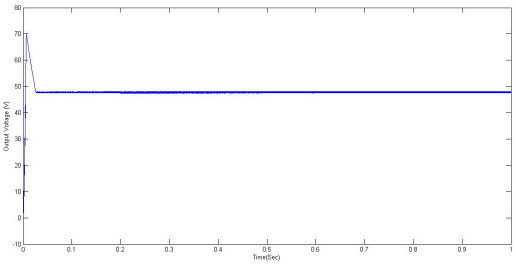


Figure 9. Output Voltage(V) with step change

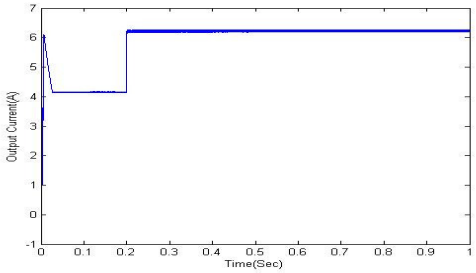



Figure 10. Output Current(A) with step change

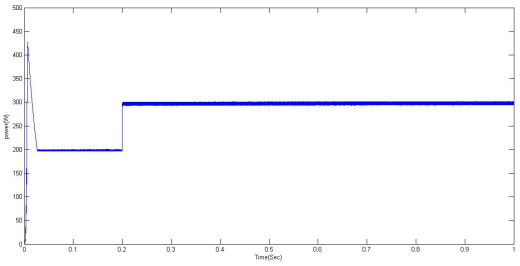


Figure 11. Output Power(W) with step change

## VI. CONCLUSION

Double input integrated buck-buck-boost converter (DIIBBBC) is presented and operating principle including operating modes, the steady state analysis and power flow control is analyzed. Validity of single-loop control strategies, voltage mode and current-mode, have been tested for load voltage regulation and power distribution. The closed-loop converter design was verified using MATLAB simulink and results proves the performance of the converter. Also, the step-load change response shows that the expected power management capability can be achieved.

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# MACHINE LEARNING APPROACH FOR ANOMALY DETECTION IN WIRELESS SENSOR DATA

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## *ABSTRACT*

*Wireless sensor nodes can experience faults during deployment either due to its hardware malfunctioning or software failure or even harsh environmental factors and battery failure. This results into presence of anomalies in their time-series collected data. So, these anomalies demand for reliable detection strategies to support in long term and/or in large scale WSN deployments. These data of physical variables are transmitted continuously to a repository for further processing of information as data stream. This paper presents a novel and distributed machine learning approach towards different anomalies detection based on incorporating the combined properties of wavelet and support vector machine (SVM). The time-series filtered data are passed through mother wavelets and several statistical features are extracted. Then features are classified using SVM to detect anomalies as short fault (SF) and noise fault (NF). The results obtained indicate that the proposed approach has excellent performance in fault detection and its classification of WS data.*

## *KEYWORDS*

*Wireless Sensor Networks, Anomaly Detection, SVM, Wavelet Filters, data fault, fault detection*

## I. INTRODUCTION

Wireless sensor networks have already emerged as potential source in monitoring and thereby collection of information in remote geographical, industrial, civil infrastructures and even power plants. In fact, a large number of sensor nodes equipped with limited computing and communication abilities are deployed to monitor the variation of physical variables. Due to their uncontrolled use or harsh environment, they are sensible to various faults which may lead to abnormal data patterns in monitoring domain. Literatures [1], [2] and [3] have reported the existence of faulty data monitored by sensors in their deployment in field environment. This is said to be caused either due to defect in hardware design, improper calibration of sensors or low battery levels of sensor nodes. Also any change or uncertainty in the environment being monitored may lead to affect the distribution of data measurements. Anomaly detection in communication network traffic and use of wavelets to identify is proposed in [4] and role of wavelet analysis is studied in [5].

Due to continuous collection of data by wireless sensor network, it becomes cumbersome to aggregate them and difficult in detection of anomalies present. The data collection from wireless sensors can be managed at centralized or distributed level in the network. The centralized approach in study of data pattern/processing posses constraint to prolong life time of network, since limited battery power of nodes gets depleted even in transmission of anomalous signals. On other hand, in case of distributed approach, each node is meant to process the data collected and send the descriptive information to either other neighbouring nodes or base station.

Truly speaking, the research needs to be oriented towards automatic detection and classification of sensor data faults at collection point itself. The investigation on faulty sensor data gains its importance

due to the fact that this would help in detection and thereby its elimination at sensor node level itself. This could enhance the battery operating life in sensor node since erroneous data need not be transmitted to the base station thus contributing towards energy efficiency of entire sensor networks. Thus, efficient anomalies detection measures need to be adopted at the node so as to raise the alert in the operating system. They need to have their performance insensitive to any parameter setting in the algorithm or any pattern change in time-series data. Additionally, it is also desired that the technique should involve low computational burden. It is crucial that a centralized network management tool embeds the required expert decision to detect all possible anomaly types, as the network is perceived holistically as an intelligent data delivery system. The design of such efficient and reliable tool demands a comprehensive understanding of all types of wireless sensor data anomalies, their likely causes, and their potential solutions.

This paper considers a study on anomalies detection and classification in wireless sensor data with use of discrete wavelet transform (DWT) and support vector machine (SVM) properties. The proposed approach does not utilize a huge amount of data in processing the information sought and efficiently detects and classifies the different types of fault with little processing time. It is aimed to detect and classify anomalies at node level according to the characteristics of data collected by each individual sensor.

The rest of the paper is organized as follows. In section 2, related work in the fault detection strategy is addressed, followed by methodology of proposed scheme with used techniques in section 3. The performance evaluation and discussion is presented in section 4. Lastly, the conclusion is drawn in section 5.

## II. RELATED WORK

In the past, fault detection in WSN has been investigated [6-11]. The authors have presented an approach based on cross-validation of statistical irregularities for on-line detection of faults in sensor measurements [6]. Ruiz et al. [7] have discussed use of external manager for fault detection in event-driven WSN. The fault diagnosis study based on PMC model is presented in [8]. The use of statistical signal processing technique, namely principal component analysis (PCA) in model development to predict the physical measurand phenomenon is presented in [9]. Any deviation in regular physical pattern with respect to model prediction suggests the occurrence of an event. Similarly, rule-based method, estimation method and learning-based method have been discussed for fault detection/classification of real-world sensor data [10-11]. The performance of these three techniques is qualitatively explored to classify the different types of fault in sensor data as short fault (SF), noise fault (NF) and constant fault (CF). The rule-based approach requires predefining the level of threshold based on histogram method to categorize the noise fault, short fault and constant fault as a separate class. The linear least square estimation approach is based on statistical correlation between sensor measurements and a suitable threshold. The value of threshold remain to be determined heuristically either by maximum error or confidence limit. A learning based approach; Hidden Markov model is also discussed to detect and classify the different fault types. The authors in [12] have used change in mean, variance, covariance for detecting distribution changes in sensor data. This detection scheme is based on the fact, probability distribution of sensor data is known a priori, which is unrealistic in field deployments. A distributed fault detection algorithm for detection and isolation of faulty sensors in communication network is presented in [13]. The proposed approach is based on local comparisons of sensed data between neighbours with a suitable threshold decision criteria test.

The problem associated in processing of huge size data is overcome with use of feature extraction by DWT and has been presented for anomaly detection in [14]. The use of DWT for anomaly detection requires predefining a threshold to make a judgment between *normal* and faulty data series.

Recently, combination of self-organizing map (SOM) with wavelet technique is suggested for anomaly detection on synthetic and as well as real world data sets [15]. The comparative study of said approach outperforms over SOM or wavelet as alone. The histogram method is used to select an appropriate value of threshold. Chenglin et al. [16] have demonstrated the use of particle swarm optimization and support vector machine in fault diagnosis of sensor.

Faulty sensors typically report extreme or unrealistic values that are easily distinguishable. Despite the above research effort, still there does not exist well-accepted technique on anomaly detection and

its classification in wireless sensor data. An edge cutting challenge is to develop the capability to carry out fault diagnosis in terms of its identification and classification without requiring any prior knowledge about the data distribution. There is no consensus on the existence of a simple, accurate and efficient approach in this line of research study. Model based event/anomaly detection scheme requires the availability of *normal* data-series in hand. The DWT technique for anomaly detection gets influenced by the value of threshold used, which in turn depends on number of samples $N$ in data series. Thus correct selection of $N$ requires knowledge to be known in advance on variation of non-faulty sensor data. A threshold set too high will result to increased missed detections, while a low value into many false positives rate. Also, a fixed threshold may not perform well under dynamic scenario of environment pattern. The use of SOM in communication applications or WSNs is widely discussed however, suffers due to its limitation in requirement for processing time, which increases with size of input data. The accuracy of SOM algorithm is influenced by size of neurons, thus a compromise must be reached between the processing time and detection/classification accuracy.
The research analysis oriented to above related problem is due to motivation drawn in application of DWT [17] and [18] for fault detection and SVMs [19] and [21] for binary and multi-class automatic classification of power system/power quality disturbances.

# III. METHODOLOGY

The reduction in data size can be obtained by extraction of important statistical features with use of wavelet approach from real time-series data sets. These features vector when passed through SVM results into classification of different types of faults. The combined approach of above two has been successfully applied in study of fault detection and classification in electrical power system. The flow chart to explain the steps adopted in series-data anomaly detection and subsequent classification to different class is illustrated in Fig.1. The anomaly detection scheme embedded in the architecture of sensor node is suggested in Fig. 2. Initially, each sensor node senses its action and information is processed. It is necessary to make a distinguish between normal and anomaly data-series. A mother wavelet extraction and feature classification through SVM is embedded in node architecture to ensure that normal data is transmitted to cluster head.

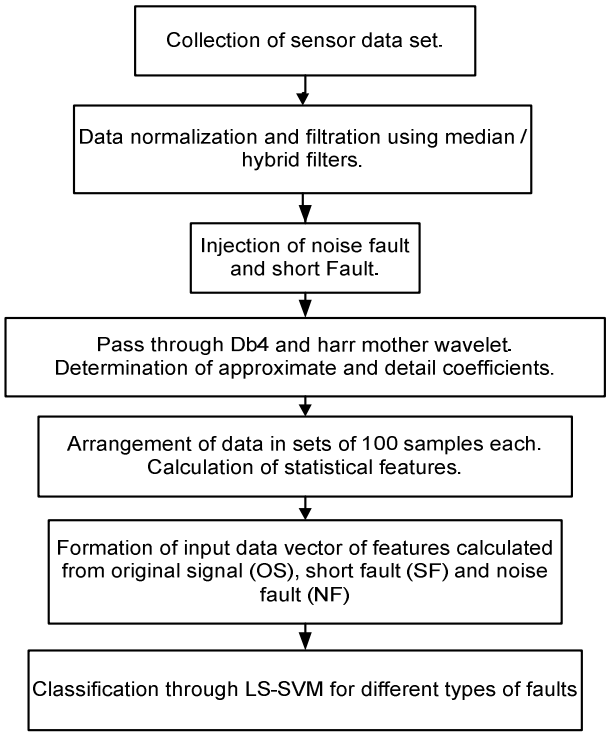



Figure 1. Flow chart of proposed scheme for series-data anomaly detection and classification

### 3.1 Discrete wavelet transform

The discrete wavelet transform decomposes transients into a series of wavelet components, each of which corresponds to a time-domain signal that covers a specific frequency band containing more detailed information. Wavelets localize the information in the time-frequency plane which is suitable for the analysis of non-stationary signals. DWT divides up data, functions into different frequency components, and then studies each component with a resolution matched to its scale. The separate decomposition of data signal into fine-scale information is referred as detail (D) coefficients, while rough-scale information known as approximate (A) coefficients. The approximation is the high scale, low-frequency component of the signal. The detail is the low-scale, high-frequency components. The decomposition process can be iterated, with successive approximations being decomposed in turn, so that one signal is divided into many lower resolution components which is called the wavelet decomposition tree and is shown in Fig. 3. As decompositions are done on higher levels, lower frequency components are filtered out progressively.

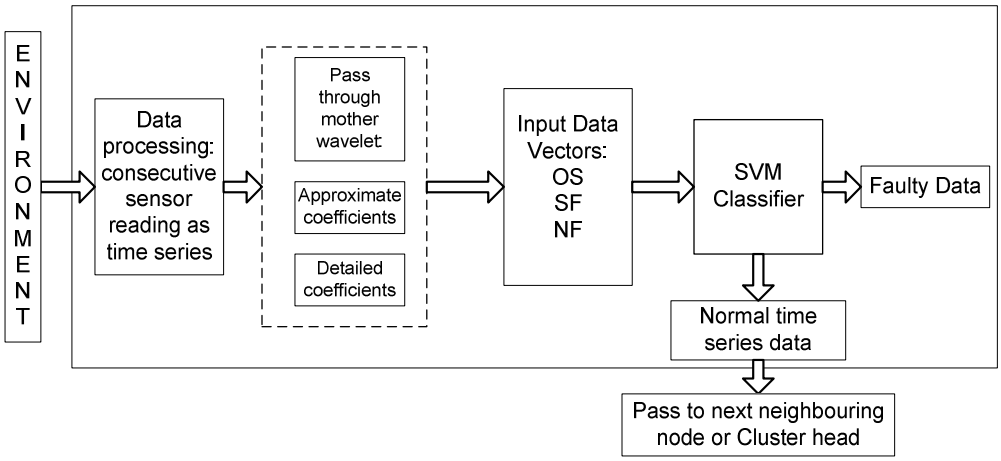



Figure 2. Internal Architecture of anomaly detection scheme

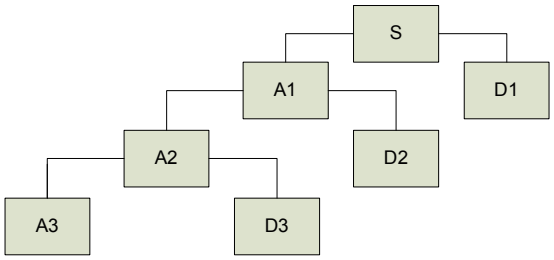



Figure 3. Wavelet decomposition tree

The wavelet transform not only decomposes a signal into frequency bands, but also, unlike the Fourier transform, provides a non uniform division of the frequency domain (i.e., the wavelet transform uses short windows at high frequencies and long windows for low frequency components). Wavelet analysis deals with expansion of functions in terms of a set of basic functions (wavelets) which are generated from a mother wavelet by operations of dilatations and translations.
DWT of sampled data signal can be obtained by implementing the discrete wavelet transform as:

$$DWT(f,x,y)=\frac{1}{\sqrt{x_0^m}}\sum_k f(k)\Psi^*\left(\frac{n-kx_0^m}{x_0^m}\right) \quad (1)$$

Where the parameters $x$ and $y$ in equation (1) are replaced by $x_0^m$ and $kx_0^m$, $k$ and $m$ being integer variables. In a standard DWT, the coefficients are sampled from the CWT on a dyadic grid. Using the scaling function, the signal can be expressed as:

$$y(t) = \sum_{k=-\infty}^{\infty} c_{jo}(k) 2^{jo/2} \phi(2^{jo} t - k) + \sum_{k=-\infty}^{\infty} \sum_{j=jo}^{\infty} d_j(k) 2^{j/2} \psi(2^j t - k) \quad (2)$$

Where $jo$ represents the coarsest scale spanned by the scaling function. The scaling and wavelet coefficients of the signal $y(t)$ can be evaluated by using a filter bank of quadrature mirror filters given as:

$$a_j^{AC}(k) = \sum_{m=-\infty}^{\infty} c_{j+1}(m) h(m - 2k) \quad (3)$$

$$d_j^{DC}(k) = \sum_{m=-\infty}^{\infty} c_{j+1}(m) h_1(m - 2k) \quad (4)$$

Equation (3) and (4) show that the coefficients at coarser level can be attained by passing the coefficients at the finer level to their respective filter followed by a decimation of two. Implementation of DWT involves successive pairs of high pass and low pass filters at each scaling stage of wavelet transform. This can be thought as successive approximations of the same function, each approximation providing the incremental information related to a particular scale (frequency range), and the first scale covering a broad frequency range at the high frequency end of the frequency spectrum, however, with progressively shorter bandwidths. Conversely, the first scale will have the highest time resolution; higher scales will cover increasingly longer time intervals. *Daubechies4* (db4) and *haar* wavelets are used in this work for fault detection in sensor data time-series.

### 3.2 Support vector machine

A class of machine-learning algorithm that uses kernel function is capable to emulate a mapping of data measurements from the input space vector to a higher dimensional feature space vector. The linear or smooth surfaces in the feature space result into non-linear surfaces in the input space and thereby classify the data as normal or anomalous. Vapnik et al. [22] introduced binary SVM classifier using theory of kernel-based methods and structural risk minimization. In respect of the limitations of other machine learning techniques like, ANNs, local minima convergence, over-learning and difficulty in selection of appropriate network structure does not pose a constraint in use of SVMs. This approach is a computationally powerful algorithm based on statistical learning theory firstly proposed by Salat and Osowski [19]. The input vector space in SVMs is usually mapped into a high dimensional feature space and a hyper-plane in the feature space is used to maximize its classification ability. SVMs can potentially handle large feature spaces as its training is carried out so that the dimension of classified vectors does not affect the performance of SVM. This suits in the application for large classification problem associated in sensor data fault types. The advantage of SVMs are due to better generalization properties as comparison to conventional neural classifiers because training is based on sequentially minimized optimization (SMO) technique [21-22]. For M-dimensional inputs $F_i (i = 1, 2, ....., M), M$ is the number of features sampled at regular interval in time-series data, which belong to class 1 or class 2 with outputs $o_i = 1$ for class OS and $o_i = -1$ for class SF/NF, respectively. The hyper-plane for linearly separable feature $F$ is represented as:

$$f(F) = w^T F + b = \sum_{j=1}^{m} w_j F_j + b = 0 \quad (5)$$

where *w* is an m-dimensional vector and *b* is a constant. The position of the separating hyperplane is decided by the values of $w$ and scalar *b*. The constraints followed by the hyperplane are
$f(F_i) \geq 1$ if $o_i = 1$ and $f(F_i) \geq -1$ if $o_i = -1$ and thus

$$o_i f(F_i) = o_i (w^T F + b) \geq +1 \; for \; i = 1, 2, ....., M \quad (6)$$

The hyperplane that creates the maximum distance between the plane and the nearest data is called the optimal separating hyperplane as shown in Fig. 4. The geometrical distance is found as $\|w\|^{-2}$ [17]. The optimal hyperplane is obtained based on the quadratic optimization problem:
Minimize

$$\frac{1}{2}\|w\|^{-2} + C\sum_{i=1}^{M}\xi_i \text{ subject to } \quad o_i(w^T s+b) \geq 1-\xi_i \quad for\ i=1,2,.....,M \tag{7}$$

$$\xi_i \geq 0 \quad for \ \ all \ \ i$$

where $\xi_i$ is the distance between the margin, parameter C is error penalty factor that takes into account misclassified point in training/testing set and the examples $F_i$ lying on the wrong side of the margin. Based on Kuhn–Tucker conditions, a maximize problem [17] can be formulated and the solution of these optimal problem leads to determination of support vector (SV) which lie on the separating hyper planes. The number of SVMs are less than the number of training samples to make SVMs computationally efficient [19]. The value of the optimal bias $b^*$ can be found from the expression: $b^* = -\frac{1}{2}\sum_{SVs} o_i\alpha_i^*(v_1^T F_i + v_2^T F_i)$ (8)

where $v_1$ and $v_2$ are the arbitrary SVMs for class 1 and class 2, respectively.
Then the final decision function is given by

$$f(F) = \sum_{SVs}\alpha_i o_i F_i^T F + b^* \tag{9}$$

Any unknown feature sample $F$ is thus classified as,

$$F \in \begin{Bmatrix} Class-1, \ f(F) \geq 0 \\ Class-2, otherwise \end{Bmatrix} \tag{10}$$

The nonlinear classification of sensor data faults can accomplished using SVMs applying a kernel function by mapping the classified data to a high-dimensional feature space where the linear classification is possible [19]. There are different kernel functions used according to the type of classification scenario.

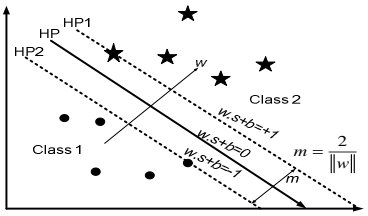



Figure 4. Optimal hyper-plane formed in SVM classification

In this paper, Gaussian radial basis kernel function which gives the best results is selected and the classification accuracy results are compared with other kernel functions, i.e. polynomial kernel. The radial basis kernel function is defined as:

$$K(F,z) = \exp\left(-\frac{|F-z|^2}{2\sigma^2}\right) \tag{11}$$

where $\sigma$ is the width of the Gaussian function known as Gaussian kernel parameter. The detailed explanation about the SVMs is given in [19]-[21].

### 3.3 Real-time series data signal processing

The combination of above two techniques is implemented to support the proposed strategy of anomaly detection in a collection of real-time series data obtained from Smart-Its [23]. A Smart-It unit embodies a sensor module consisting of light sensor, microphone thermometer, X-axis and Y-axis accelerometers and pressure sensor along with a communication module. The series time variation of sound, light and pressure signals are shown in Fig. 5. These data sets were obtained over several states of environment. The constant value of pressure sensor over the entire data series is depicted which suggests a "constant" fault type. The real-time wireless sensor data of sound, light and

pressure signals is processed after being passed through median filter and median-hybrid filter. Median filter is the nonlinear filter used to preserve abrupt shifts (edges) and remove the impulsive noise from the data-series. The main issue that exists with median filter is due to its high computational cost. While on the other hand, linear median-hybrid filters have been suggested to combine the good properties of linear and median filters by linear and nonlinear operations. They are computationally much less expensive than standard median filters. The series-data in study for anomaly detection is normalized to eliminate the potential outliers as:

$$Normalized\ data = \frac{Raw\ data - Mean(Raw\ data)}{Variance(Raw\ data)} \quad (12)$$

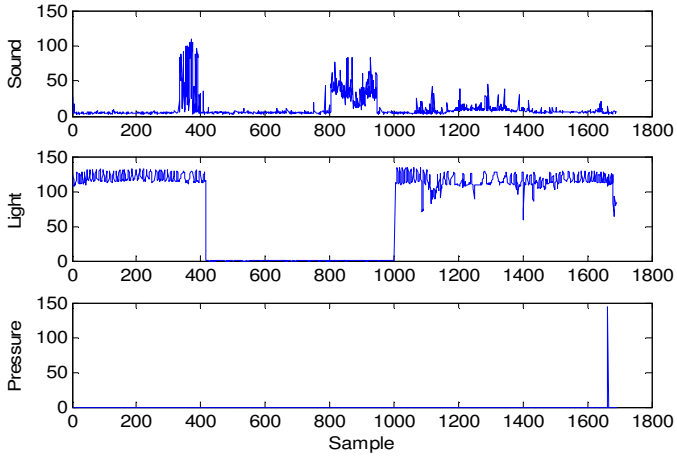



Figure 5. Real-time series variation of raw signals

### 3.4 Sensor data faults:

The three common types of sensor data faults as according to the definition in [8] are short fault, noise fault and constant fault. The short fault refers to sharp change in monitored quantity at an instant with respect to its previous sample. The noise fault is characterized by an increased variance over a definite period, i.e. successive samples unlike short fault at single sample only. On the other hand, constant fault describes a constant value, may be either higher or lower compared to normal measurements for successive samples. Such fault type results to zero value of standard deviation for monitored samples. In the study reported here, only two types of faults; short fault and noise fault are considered. These faults have been experimentally observed in several environmental monitoring platforms.

A sample of short fault (SF) data is obtained by injecting short fault intensity $f = \{3.5\}$ to a data value as: $d_i^{sf} = d_i \times f$ (13)

at a randomly picked data sample $d_i$.

Fig. 6 shows the instants at which short fault were injected into the signal obtained through filters for their detection classification. The total percentage of short fault injected into series data is about 1.0%.Similarly, a series of noise fault (NF) is introduced into normalized raw data through random selection of successive samples $d_s$ and superimpose of a random signal with 20dB noise content having signal property of zero mean and unity variance. The variation of sound series data with noise introduced at randomly chosen 200 successive samples over three different intervals is shown in Fig. 7. Thus, total number of noise fault samples in the series data is 35.5%.

### 3.5 Combination of DWT and SVM:

The approximate and detail coefficients are obtained through *db4* and *haar* wavelet from the normalized data after being passed into median and hybrid filter. These coefficients belong to original signal (OS) without any fault, short fault and noise fault injected in time series data. To reduce the size of input data fed to SVM, four features; namely mean, standard deviation, moment and variance are extracted from each 100 samples in time series data. Thus time-series data is transformed into sets of features $\{f_{mean}, f_{STD}, f_m, f_{\text{var}}\}$ and now to be represented as:

$$F_{OS}, F_{SF}, F_{NF} = \begin{bmatrix} f_{mean} & f_{STD} & f_m & f_{\text{var}} & for\ 1-100\ samples \\ : & : & : & : & : \\ f_{mean} & f_{STD} & f_m & f_{\text{var}} & for\ 1501-1600\ samples \end{bmatrix} \quad (14)$$

Thus, feature vector of time-series data consists of 16 rows with 4 columns.

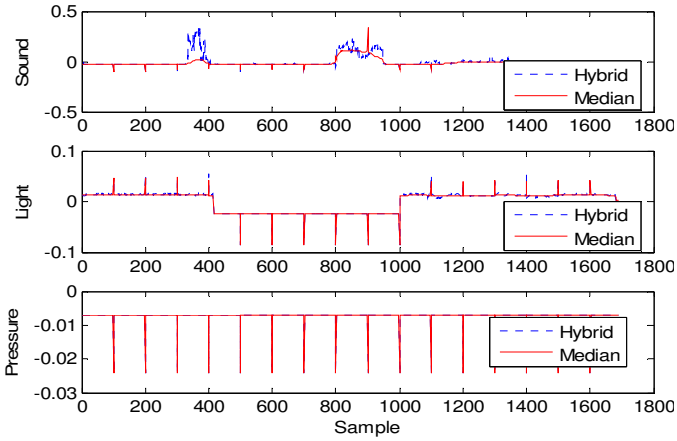



Figure 6. Short fault injected into the raw signal (normalized)

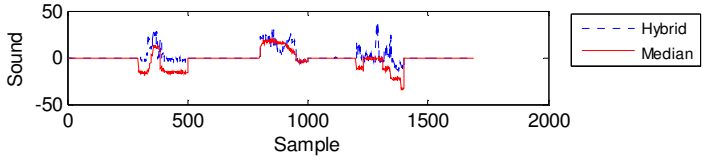



Figure 7.Noise fault introduced into the raw signal (normalized)

The data collection by sensor may have any pattern of anomaly present in the entire length of time-series. A subset of data measurements over some continuous time frame may differ in their pattern from the general trend to warrant being considered as anomalous data series. Hence to take into account such phenomenon occurrence, the input data vector fed to SVM is represented in two different forms; sequential-series (SE) and staggered-series (ST). A sequential-series of features refers to time-series wherein, entire length of data consists of samples corresponding to original signal followed by anomaly signal. On other hand, staggered-series relates to time-series that consists of alternate sampled series of original signal and anomaly signal. An enhanced performance in classification may be achieved with use of more number of data sets in training of SVM. So, use of duplicate data sets corresponding to each pattern is considered in study. Thus, input vector fed to SVM for classification is given as:

$$(Input\ vector)_{SE} = \begin{bmatrix} F_{OS} \\ F_{OS} \\ F_{SF,NF} \\ F_{SF,NF} \end{bmatrix}; \qquad (Input\ vector)_{ST} = \begin{bmatrix} F_{OS} \\ F_{SF,NF} \\ F_{OS} \\ F_{SF,NF} \end{bmatrix} \quad (15)$$

and forms 32 rows with 4 columns.

With the above input vector, the objective remains to partition set of features belonging to each category of type of signal, i.e. $F_{OS} \cap F_{SF} = \Phi$ and $F_{OS} \cap F_{NF} = \Phi$. The output of SVM algorithm for sets of features that belong to OS class is defined as 1, while for fault types, as -1 to differentiate between the two categories. The input vector (15) obtained using time-series data passed through median filter is considered for training, while those from hybrid filter as testing of SVM classifier.

# IV. PERFORMANCE EVALUATION AND DISCUSSION

This section presents the performance evaluation of proposed scheme; integration of DWT and SVM in detection and classification of anomaly in time-series data collected by wireless sensor. The results presented here are produced using real-time series data sets obtained from sensor modules deployed in real environment. The performance indices (16-18) are used to assess the performance of proposed scheme of anomaly detection in real time-series data sets [21]. Consider $\{P,N\}$ be the positive and negative instance classes as assigned and $\{P_c,N_c\}$ be the classifications obtained by the SVM classifier. Also consider, $P(P|I)$ be the posterior probability for an instance $I$ that is positive. Then,

True positive rate (TPR) of the classifier is:

$$TPR = P(P_c|P) \approx \frac{positives\ correctly\ classifed}{total\ \ positives\ assigned} \quad (16)$$

False positive rate (FPR) of the classifier is:

$$FPR = P(P_c|N) \approx \frac{negatives\ incorrectly\ classifed}{total\ negatives\ assigned} \quad (17)$$

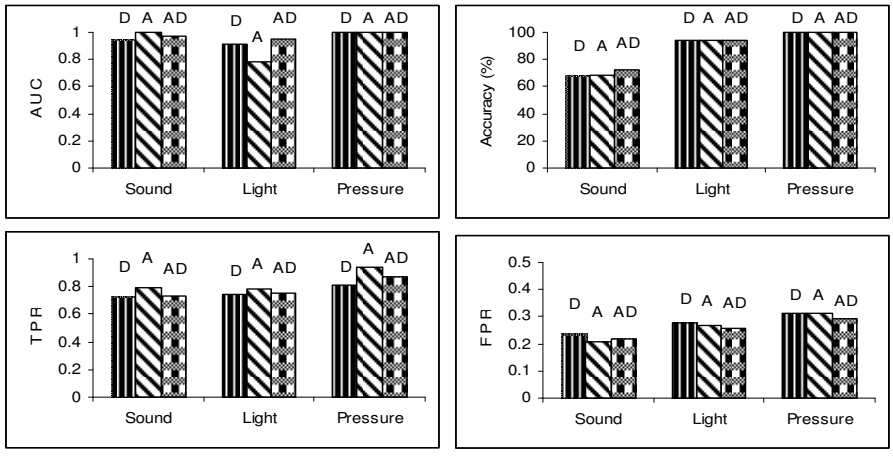
Detection accuracy (DA) of the classifier is:

$$Detection\ accuracy = \frac{TPR}{TPR + FPR} \times 100\,\% \quad (18)$$

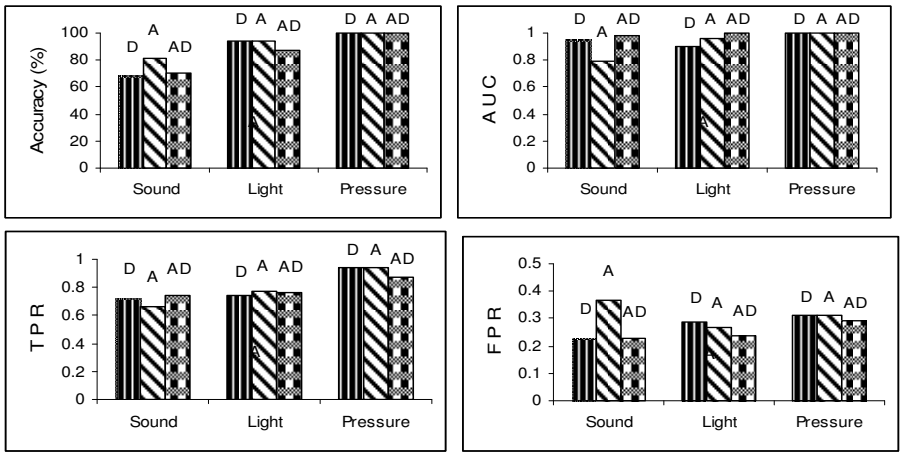
Area under the receiver operating characteristic (ROC) curve (AUC): The area under the ROC curve, or simply AUC, provides a good "summary" for the performance of the ROC curves [22].

## 4.1 SVM as binary classifier:

The performance indices of classifier scheme are evaluated using features extracted from detail (D), approximate (A) and both approximate and detail (AD) coefficients of wavelet. The analysis of these indices determined for time-series data belonging to original signal and short fault is shown in Fig. 8. The AUC value of classifier is observed to be in the range from 0.90-1.0. A unity value of AUC is indicated for pressure data series. In fact, the original pressure signal exhibits a constant value and a short fault injected within 100 samples, are distinctly represented in form of statistical feature. Thus, such change in data pattern is distinctly classified as a separate class. Fig. 9 shows the classification performance of original signal against noise fault. As observed, AUC gets increased with use of features extracted from both approximate and detail (AD) coefficients of wavelet. The classification pattern generated from SVM classifier for light signal and sound signal is depicted in Fig. 10 and 11 respectively. As observed, the features are distinctly represented through the classifier boundary.

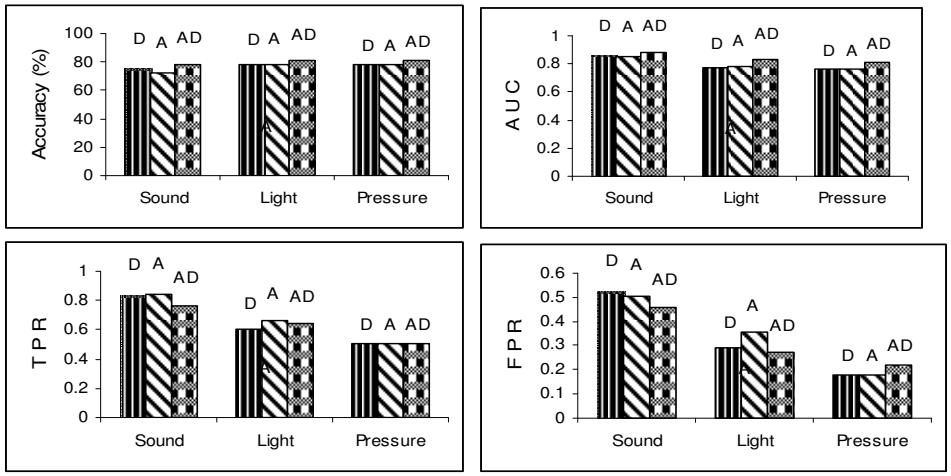



(a) Sequential series

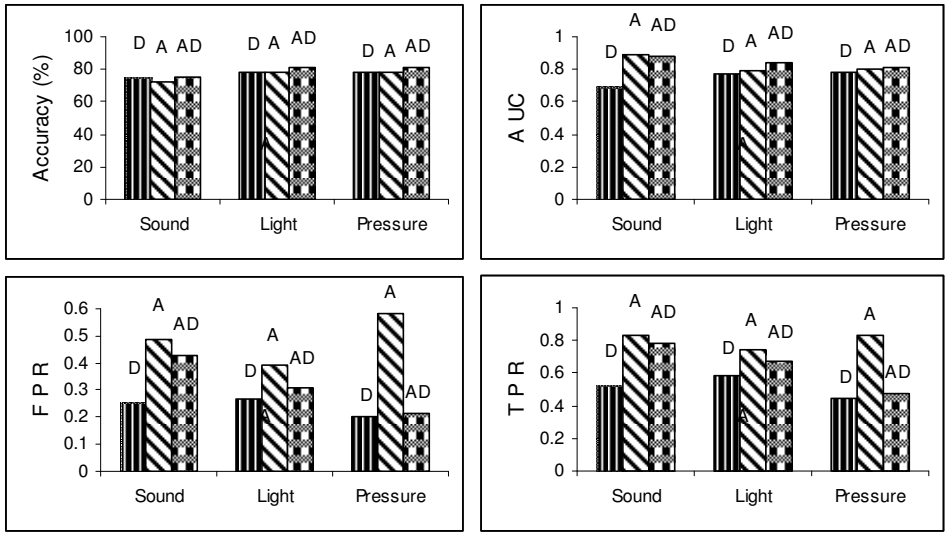



(b) Staggered series

Figure 8. Performance indices of SVM classifier as binary class for OS vs SF

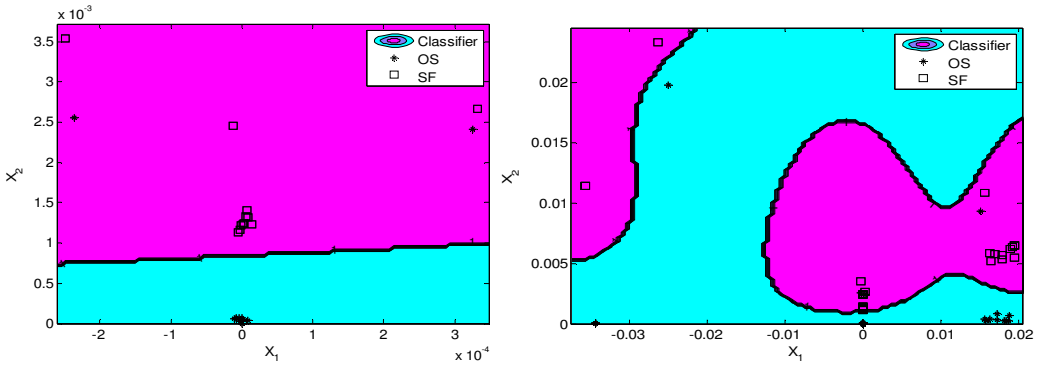



(a) Sequential series



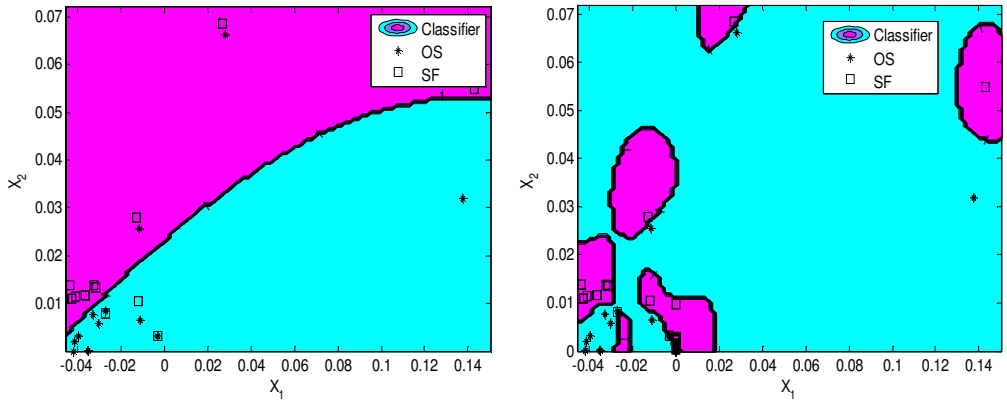

(b) Staggered series

Figure 9.Performance indices of SVM classifier binary class for OS vs NF




(a) Detail coefficient (b) Both approximate and detail coefficient

Fig. 10.Classification pattern of SVM classifier for light signal as sequential series



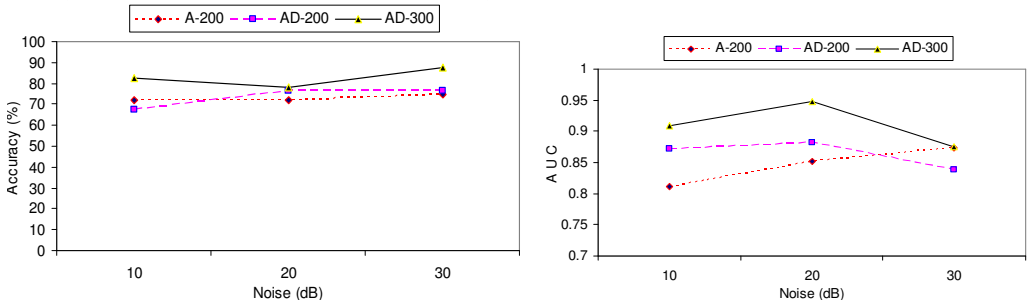

(a) Approximate coefficient (b) Both approximate and detail coefficient

Figure 11. Classification pattern of SVM classifier for sound signal as staggered series

Further, the result is presented for time series data having different magnitude of noise introduced at randomly chosen 200 and 300 successive samples with features fed as sequential series to SVM classifier. The classification performance between original and noise of sound signal by use of approximate and approximate-detail coefficients is presented in Fig. 12. As observed, the classification property has not deteriorated.

Next, classifier performance is tested for time series data having different magnitude of short fault introduced. The results are presented in Fig. 13 for classification between original and short fault light signal with features fed as sequential and staggered series.

The SVM classifier by use of coefficients extracted through haar mother wavelet is also carried out and presented in following paragraph. The results are obtained for short fault, $f = \{3.5\}$ and 20 dB noise introduced in time series data. The comparative performance with AD coefficients extracted through dB4 mother wavelet is shown in Fig. 14.



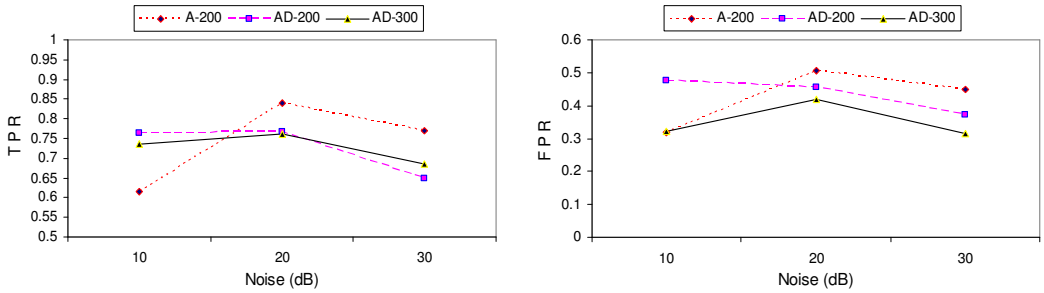



Figure 12.Classification performance for different magnitude of noise introduced at randomly chosen 200 and 300 successive samples

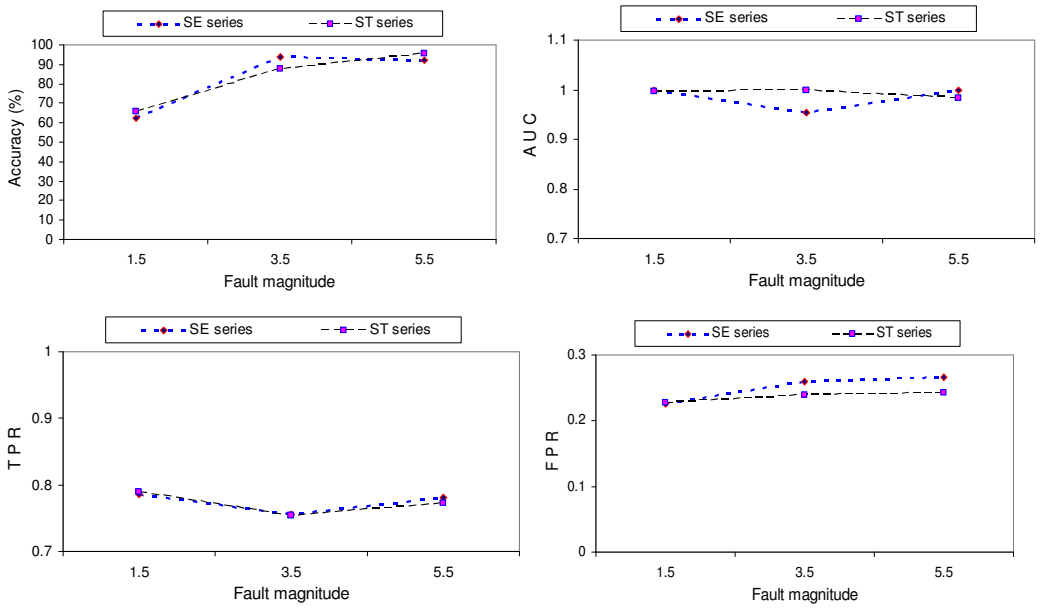



Figure 13. Classification performance for different magnitude of short fault introduced

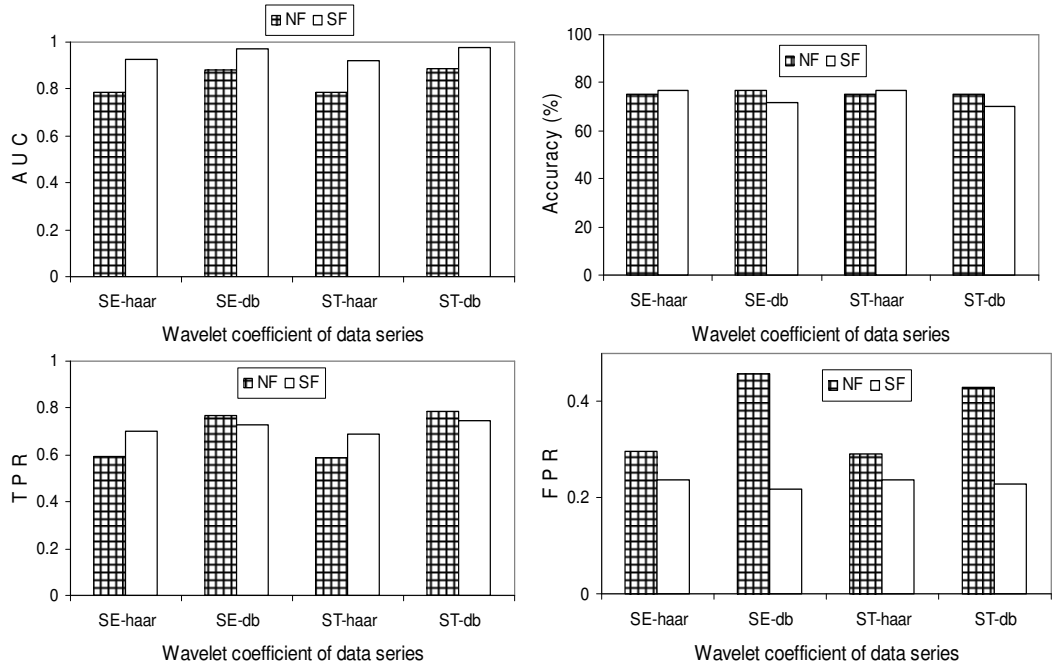
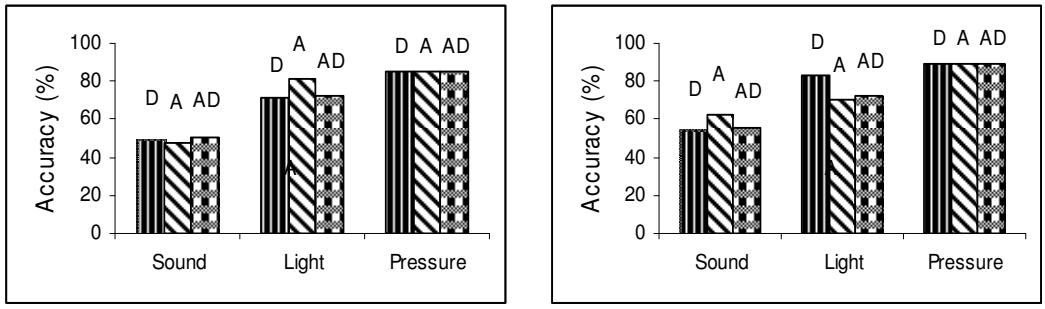



Figure 14. Comparative performance between mother wavelets for OS-SF and OS-NF by use of features as sequential and staggered series

### 4.2 SVM as multi-class classifier:

The classification of original signal against short fault and noise fault as a multi-class problem is discussed in this sub-section. Since performance in terms of detection accuracy can be considered for multi-class, thus other indices are not evaluated. Fig. 15 presents the detection accuracy with use of features extracted from different coefficients of wavelet




(a) Sequential series (b) Staggered series

Figure 15. Performance indices of SVM classifier as multi-class for OS vs SF vs NF

## V. CONCLUSION

The integration of DWT and SVM for anomaly detection and classification problem was presented in this paper using real-time series data of wireless sensor deployed in field environment. The signal processing property of DWT was utilized in fine-scale and approximate-scale extraction of information from data. The use of statistical features instead of series data in form of wavelet coefficients resulted in reduce size of input vector fed to SVM. The value of AUC as binary class was determined in the range of 0.9-1.0 for OS against SF, while for OS against NF, it lies between 0.75-0.86. The robustness of SVM classifier was demonstrated for fault magnitude change and different noise level introduced in time series data. The detection accuracy as multi-class was also found to be high. The suggested approach in anomaly detection and classification is independent from heuristic adjustment of any parameter and does not require any domain knowledge of non-faulty data series in obtaining high accuracy.

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# FEED FORWARD BACK PROPAGATION NEURAL NETWORK METHOD FOR ARABIC VOWEL RECOGNITION BASED ON WAVELET LINEAR PREDICTION CODING

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## *ABSTRACT*

*A novel vowel feature extraction method via hybrid wavelet and linear prediction coding (LPC) is presented here. The proposed Arabic vowels recognition system is composed of very promising techniques; wavelet transform (WT) with linear prediction coding (LPC) for feature extraction and feed forward backpropagation neural network (FFBPNN) for classification. Trying to enhance the recognition process and for comparison purposes, three techniques of WT were applied for the feature extraction stage: Wavelet packet transform (WPT) with LPC, discrete wavelet transform (DWT) with LPC, and WP with entropy (WPE). Moreover, different levels of WT were used in order to enhance the efficiency of the proposed method. Level 2 until level 7 were studied. A MATLAB program was utilised to build the model of the proposed work. The performance of 82.47% recognition rate was established. The mentioned above methods were investigated for comparison. The best recognition rate selection obtained was for DWT.*

***KEYWORDS***: *Wavelet; Entropy; Neural Network; Arabic Vowels.*

## I. INTRODUCTION

Unlike the English language, Arabic language recognition has the lowest share of attraction; this is due to its nature, in terms of, various dialects and several alphabets forms. But because of an increase of loudening activity in mobile communication domain draw new opportunities and shed some lights for applications of speech recognition including words and sentences in English as well as in Arabic. So, the Arabic text to speech and vice versa as well as incredibly critical issues in many applications that are attracted the users.

Numerous researchers have contributed in speech recognition, particularly in Arabic language recognition. The major work of studying speech recognition for Arabic language dealing with the morphological structure is presented in [1]. To recognize the distinct Arabic phonemes (pharyngeal, geminate and emphatic consonants) [2,3], the phonetic features is discussed. This allocates and motivates interesting researchers of Arabic language with different dialect at various countries. The applications in term of implementation of recognition system devoted to spoken separated words or continuous speech are not extensively conducted. [4] has studied the derivative scheme, named the concurrent general recursive neural network (GRNN), implemented for accurate Arabic phonemes recognition in order to automate the intensity and formants-based feature extraction. The validation tests expressed in terms of recognition rate obtained with free of noise speech signals were up to 93.37%. [5] has investigated an isolated word speech recognition by means of the recurrent neural network (RNN). The achieved accuracy was 94.5% in term of recognition rate in speaker-independent mode and 99.5% in speaker-dependent mode. [6] discussed a set of Arabic speech recognition systems also.

The Fuzzy C-Means method has been added to the traditional ANN/HMM speech recognizer using RASTA-PLP features vectors. The Word Error Rate (WER) is over 14.4%. With the same way, an

approach using data fusion gave a WER of 0.8%. However, this method was tested only on one personal corpus and the authors showed that the obtained improvement needed the use of three neural networks running in parallel. Another alternative hybrid method was suggested [7], where the Support Vector Machine (SVM) and the K nearest neighbour (KNN) were substituted to the ANN in the traditional hybrid system, but the recognition rate, did not exceed 92.72% for KNN/HMM and 90.62% for SVM/HMM.

Saeed and Nammous [8] presented a novel Algorithm to recognize separate voices of some Arabic words, the digits from zero to ten. For feature extraction, transformation and hence recognition, the algorithm of minimal eigenvalues of Toeplitz matrices together with other methods of speech processing and recognition were used. The success rate obtained in the presented experiments was almost ideal and exceeded 98% for many cases. A hybrid method has been applied to Arabic digits recognition [9].

In literature papers, other researchers used neural networks to recognize features of Arabic language such as emphasis, gemination and related vowel lengthening. This was studied using ANN and other techniques [10], where many systems and configurations were considered including time delay neural networks (TDNNs). Again ANNs were used to identify the 10 Malay digits [11, 12] has anticipated a heuristic method of Arabic digit recognition, by means of the Probabilistic Neural Network (PNN). The use of a neural network recognizer, with a nonparametric activation function, presents a promising solution to increase the performances of speech recognition systems, particularly in the case of Arabic language. [13] demonstrated the advantages of the GRNN speech recognizer over the MLP and the HMM in calm environment.

Unfortunately, formants of Arabic vowels are not sufficiently tackled in the literature. Other studies that addressed formant frequencies in Arabic were not directed toward obtaining norms or comparing these frequencies to frequencies of vowels spoken by other populations. As an alternative, studies were directed toward speech perception, recognition, or speech analysis in Arabic [19,20,21,22]. These studies scheduled a range of formant frequency values. The presented research paper introduces a novel combination of wavelet transform, LPC and FFBPNN. The benefit of such sophistication conjunction is to create a dialect-independent Arabic vowels classifier. The remainder of the paper is organized as follows: a brief introduction to Arabic language is presented in section 2. The proposed method is described in section 3. The experimental results and discussion is introduced in section 4 followed in section 5 by conclusions.

## II. ARABIC LANGUAGE

Recently, Arabic language became one of the most significant and broadly spoken languages in the world, with an expected number of 350 millions speakers distributed all over the world and mostly covering 22 Arabic countries. Arabic is Semitic language that characterizes by the existence of particular consonants like pharyngeal, glottal and emphatic consonants. Furthermore, it presents some phonetics and morpho-syntactic particularities. The morpho-syntactic structure built, around pattern roots (CVCVCV, CVCCVC, etc.) [22]. The Arabic alphabet consists of 28 letters that can be expanded to a set of 90 by additional shapes, marks, and vowels. The 28 letters represent the consonants and long vowels such as ى and آ (both pronounced as/a:/), ي (pronounced as/i:/), and و ( pronounced as/u:/). The short vowels and certain other phonetic information such as consonant doubling (shadda) are not represented by letters directly, but by diacritics. A diacritic is a short stroke located above or below the consonant. Table 1 shows the complete set of Arabic diacritics. We split the Arabic diacritics into three sets: short vowels, doubled case endings, and syllabification marks. Short vowels are written as symbols either above or below the letter in text with diacritics, and dropped all together in text without diacritics. We get three short vowels: fatha: it represents the /a/ sound and is an oblique dash over a letter, damma: it represents the /u/ sound and has shape of a comma over a letter and kasra: it represents the /i/ sound and is an oblique dash under a letter as reported in Table 1.

**Table 1**. Diacritics above or below consonant letter

| Short Vowel Name (Diacritics) | Diacritics above or below letter 'ب' (sounds B) | Pronunciation |
|---|---|---|
| Fatha | بَ | /ba/ |
| Damma | بُ | /bu/ |
| Kasra | بِ | /bi/ |
| Tanween Alfath | بًا | /ban/ |
| Tanween Aldam | بٌ | /bun/ |
| Tanween Alkasr | بٍ | /bin/ |
| Sokun | بْ | /b/ |

# III. FEATURES EXTRACTION BY WAVELET TRANSFORM

Before the stage of features extraction, the speech data are processed by a silence removing algorithm followed by the application of a pre-processed by applying the normalization on speech signals to make the signals comparable regardless of differences in magnitude. In this study three feature extraction methods based on wavelet transform are discussed in the following part of the paper.

## 3.1 Wavelet Packet Method with LPC

For an orthogonal wavelet function, a library of wavelet packet bases is generated. Each of these bases offers a particular way of coding signals, preserving global energy and reconstructing exact features. The wavelet packet is used to extract additional features to guarantee higher recognition rate. In this study, WPT is applied at the stage of feature extraction, but these data are not proper for classifier due to a great amount of data length. Thus, we have to seek for a better representation for the vowel features. Previous studies proposed that the use of LPC of WP as features in recognition tasks is competent. [18] Suggested a method to calculate the LPC orders of wavelet transform for speaker recognition. This method may be utilized for Arabic vowel classification. This is possible because each Arabic vowel has distinct energy (Fig.2). Fig.4 shows LPC orders calculated for WP at depth 2 for three different utterances of Arabic a-vowel for the same person. We can notice that the feature vector extracted by WP and LPC is appropriate for vowel recognition.

## 3.2 Discrete Wavelet Transform Method with LPC

The additional proposed method is DWT combined with LPC. In this method the LPC is obtained from DWT Sub signals. The DWT at level three is generated and then 30 LPC orders are obtained for each sub signals to be combined in one feature vector. The main advantage of such sophisticated feature method is to extract different LPC impact based on multi resolution of DWT capability [14]. LPC orders sequence will contain distinguishable information as well as wavelet transform. Fig.4 shows LPC coefficients calculated for DWT at depth 3 for three different utterances of Arabic a-vowel for the same person. We may notice that the feature vector extracted by DWT and LPC is appropriate for vowel recognition.

## 3.3 Wavelet Packet Entropy Method

[15] Suggested a method to calculate the entropy value of the wavelet norm in digital modulation recognition. [16] Proposed features extraction method for speaker recognition based on a combination of three entropy types (sure, logarithmic energy and norm). Lastly, [17] investigated a speaker identification system using adaptive wavelet sure entropy.

As seen in above studies, the entropy of the specific sub-band signal may be employed as features for recognition tasks. This is possible because each Arabic vowel has distinct energy (see Fig.2). In this paper, the entropy obtained from the WPT will be employed for Arabic vowels recognition. The features extraction method can be explained as follows:

- Decomposing the speech signal by wavelet packet transform at level 7, with Daubechies type (db2).
- Calculating three entropy types for all 256 nodes at depth 7 for wavelet packet using the following equations:

Shannon entropy:

$$E1(s) = -\sum_i s_i^2 \log(s_i^2) \quad (1)$$

Log energy entropy:

$$E1(s) = \sum_i \log(s_i^2) \quad (2)$$

Sure entropy:

$$|s_i| \le p \Rightarrow E(s) = \sum_i \min(s_i^2, p^2) \quad (3)$$

where $s$ is the signal, $s_i$ are the WPT coefficients and $p$ is a positive threshold. Entropy is a common concept in many fields, mainly in signal processing. Classical entropy-based criterion describes information-related properties for a precise representation of a given signal. Entropy is commonly used in image processing; it posses information about the concentration of the image. On the other hand, a method for measuring the entropy appears as a supreme tool for quantifying the ordering of non-stationary signals. Fig.3 shows Shannon entropy calculated for WP at depth 7 for Arabic a-vowel and Arabic e-vowels for two persons. For each person two different utterances were used, we can notice that the feature vector extracted by Shannon entropy is appropriate for vowel recognition. This conclusion has been obtained by interpretation the following criterion: the feature vector extracted should possess the following properties:

1) Vary widely from class to class.
2) Stable over a long period of time.
3) Should not have correlation with other features (see Fig.3 and 4).

### 3.4 Classification

Speech recognition with NN has recently undergone a significant development. Early experiments have exposed the potential of these methods for tasks with limited complexity. Many experiments have then been performed to test the ability of several NN models or approaches to the problem. Although most of these preliminary studies deal with a small number of signals, they have shown that NN models were serious candidates for speaker identification or speech recognition tasks. NN classifiers like FFBPNN may lead to very good performances because they allow to take into account speech features information and to build complex decision regions. However, the complexity of classification training procedures forbids the use of this simple approach when dealing with a large number of patterns. Two solutions do emerge for managing large databases: modular classification systems which a how to break the complexity of single NN architectures, or NN predictive models which tender a large variety of possible implementations.

Classification operation performs the intelligent discrimination by means of features obtained from feature extraction phase. In this study FFBPNN is used. The training condition and the structure of the NN used in this paper are as tabulated in Tab.2. These were selected empirically for the best performance selected for $10^{-5}$ of mse. That is accomplished after several experiments, such as the number of hidden layers, the size of the hidden layers, value of the moment constant, and type of the activation functions or transfer functions. 180x24 feature matrix which is obtained in features extraction stage for 24 vowel patterns (see flow chart at Fig.1) is given to the input of the Feed-forward networks consist of several layers using the DOTPROD weight function, NETSUM net input function, and the particular transfer functions. The weights of the first layer come from the input. Each network layer has a weight coming from the previous layer. All layers have biases. The last layer is the network output, which we call target (T). In this paper target is designed as a six binary digits for each features vector:

$$T = \begin{bmatrix} 0\ 0\ 0...1 \\ 0\ 0\ 0...0 \\ 0\ 0\ 0...0 \\ 0\ 1\ \ 1...1 \\ 1\ 0\ \ 1...0 \end{bmatrix} \quad (4)$$

**Table 2** Parameters used for the Network

| Functions | Description |
|---|---|
| Network Type | Feed Forward Back Propagation |
| No. of Layers | Four Layers: Input, Two Hidden & Output |
| No. of neurons in Layers | 128- Input, 30-Hidden & -4 Output |
| Weight Function | DOTPROD |
| Training Function | Levenberg-Marquardt Backpropagation |
| Activation functions | Log- sigmoid |
| Performance Function (mse) | $10^{-5}$ |
| No. of Epochs | 200 |

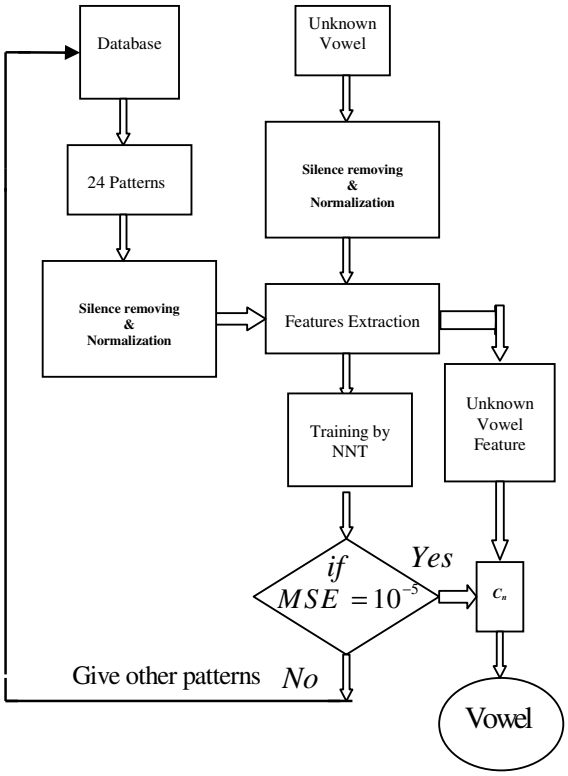


Fig. 1. Proposed expert system flow diagram of the proposed system

The mean square error of the NN is achieved at the final of the training of the ANN classifier by means of Levenberg-Marquardt Backpropagation. Backpropagation is used to compute the Jacobian jX of performance with respect to the weight and bias variables X. Each variable is adapted according to Levenberg-Marquardt,

$$jj = jX * jX$$
$$je = jX * E \quad (5)$$
$$dX = -(jj + I * Mu) \setminus je$$

Where $E$ is all errors and $I$ is the identity matrix. The adaptive value $Mu$ is increased by 10 $Mu$ increase factor until the change above outcomes in a reduced performance value. The change is then made to the network and $Mu$ is decreased by 0.1 $Mu$ decrease factor. After training the 24 (12 male and 12 female) speakers a feature, imposter simulation is performed. The unknown vowel simulation result (SR) is compared with each of the 24 patterns target ( $P_n$, n =1,2,…,24) in order to determine the decision by

$$C_n = 100 - [100 * \sqrt{(\sum (P_n - SR)^2 / \sum P_n^2)}] \quad (6)$$

where $C_n$ is the similarity percent between unknown vowel simulation results and pattern target $P_n$. The vowel is identified as patterns of maximum similarity percent. For instant, when most higher magnitudes of $C_n$ belong to given type patterns then decision is this type.

## IV. RESULTS AND DISCUSSION

In this research paper, speech signals were recorded via PC-sound card, with a sampling frequency of 16000 Hz. The Arabic vowels were recorded by 27 speakers of different Arabic dialects (Jordanian, Palestinian and Egyptian: 5 females, along with 22 males. The recording process was provided in normal university office conditions. Our investigation of speaker-independent Arabic vowels classifier system performance is performed via several experiments depending on vowel type. In the following three experiments the used feature extraction method is WP and LPC.

**Experiment-1**

We experimented 95 long Arabic vowels آ (pronounced as/a:/) signals, 354 long Arabic vowels ي (pronounced as/e:/) signals and 88 long Arabic vowels و (pronounced as/u:/) signals. The results indicated that 84.44% were classified correctly for Arabic vowels آ, 71.47% of the signals were classified correctly for Arabic vowel ي, and 72.72% of the signals were classified correctly for Arabic vowel و. Tab.3 shows the results of Recognition Rates.

**Experiment-2**

We experimented 90 short Arabic vowels أ (fatha) (pronounced as/a:/) signals, 45 short Arabic vowels ي (kasra) (pronounced as/e:/) signals and 45 long Arabic vowels و (damma) (pronounced as/u:/) signals. The results indicated that 100% were classified correctly for short Arabic vowels أ, 84.44% of the signals were classified correctly for short Arabic vowel ي, and 91.11% of the signals were classified correctly for short Arabic vowel و. Tab.4 shows the results of Recognition Rates.

**Experiment-3**

In this experiment we study the recognition rates for long vowels connected with other letter such ل (pronounced as/l/) and ر (pronounced as/r/). Tab. 5, reported the recognition rates. The results indicated 82.89% average recognition rate.

**Experiment-4**

In experiment-4, short Arabic vowels: fatha: represents the short أ (pronounced as short /a/), kasra: represents the short ي (pronounced as short /e:/) and damma represents short و (pronoused as short /u/) for each vowel a number of signals of 20 speakers results are reported in tab. 6 . The recognition rates of above mentioned three short vowels connected with other letter such ل (pronounced as/l/) and ر (pronounced as/r/) are studied and their results are tabulated in table 6. The average recognition rate was 88.96%.

**Table 3:** The recognition rate results for long vowels

| Long Vowels | Number of Signals | Recognized Signals | Not Recognized Signals | Recognition Rate [%] |
|---|---|---|---|---|
| **Long A** أ | 90 | 76 | 14 | 84.44 |
| **Long E** ي | 354 | 253 | 101 | 71.47 |
| **Long O** و | 88 | 64 | 24 | 72.72 |
| | | | **Avr. Recognition Rate** | **76.21** |

**Table 4:** The recognition rate results for short vowels

| Short Vowels | Number of Signals | Recognized Signals | Not Recognized Signals | Recognition Rate [%] |
|---|---|---|---|---|
| **Short A** أ | 95 | 95 | 0 | 100 |
| **Short E** ي | 45 | 38 | 7 | 84.44 |
| **Short O** و | 45 | 41 | 4 | 91.11 |
| | | | **Avr. Recognition Rate** | **91.85** |

**Table 5:** The recognition rate results for long vowels connected with other letters

| Long Vowels | Number of Signals | Recognized Signals | Not Recognized Signals | Recognition Rate [%] |
|---|---|---|---|---|
| **La** لا | 54 | 46 | 8 | 85.19 |
| **Le** لي | 54 | 52 | 2 | 96.30 |
| **Lo** لو | 54 | 32 | 22 | 59.26 |
| **Ra** را | 48 | 44 | 4 | 91.67 |
| **Re** ري | 46 | 40 | 6 | 89.96 |
| **Ro** رو | 48 | 36 | 12 | 75.00 |
| | | | **Avr. Recognition Rate** | **82.89** |

**Table 6:** The recognition rate results for short vowels connected with other letters

| Short Vowels | Number of Signals | Recognized Signals | Not Recognized Signals | Recognition Rate [%] |
|---|---|---|---|---|
| **La** لا | 54 | 50 | 4 | 92.59 |
| **Le** لي | 54 | 50 | 4 | 92.59 |
| **Lo** لو | 54 | 48 | 6 | 88.89 |
| **Ra** را | 46 | 38 | 8 | 82.61 |
| **Re** ري | 48 | 44 | 4 | 91.67 |
| **Ro** رو | 48 | 41 | 9 | 85.42 |
| | | | **Avr. Recognition Rate** | **88.96** |

In the next experiment, the performances of the three WT Arabic vowels recognition systems (proposed in section 3) are compared with each other under the recorded database. The results of these experiments are summarized in Tab. 7. The best results were achieved by DWT and LPC.

**Table 7:** The recognition rate results for the three proposed systems

| Recognition method | Number of Signals | Recognition Rate [%] |
|---|---|---|
| **WP** | 1356 | 80.23 |
| **DWT** | 1356 | 82.47 |
| **WPE** | 1356 | 72.9 |

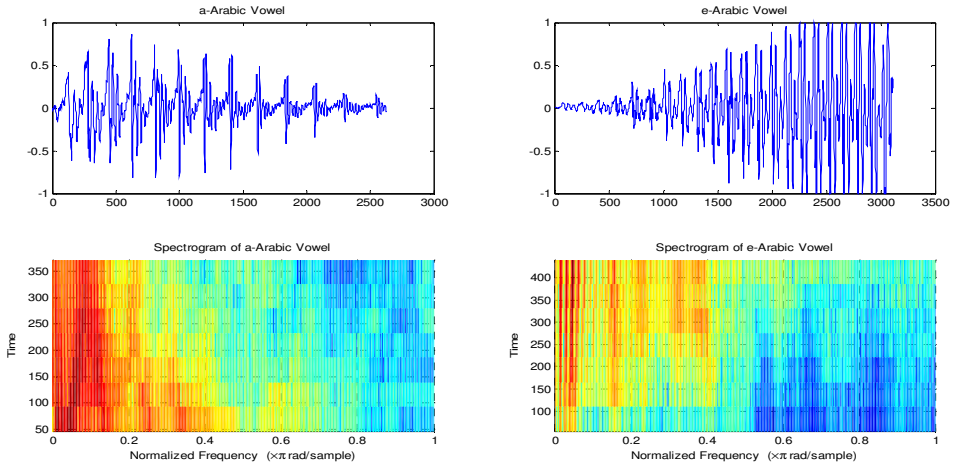


**Figure 2**.a. First Arabic Vowels of a speaker 1 with spectrogram

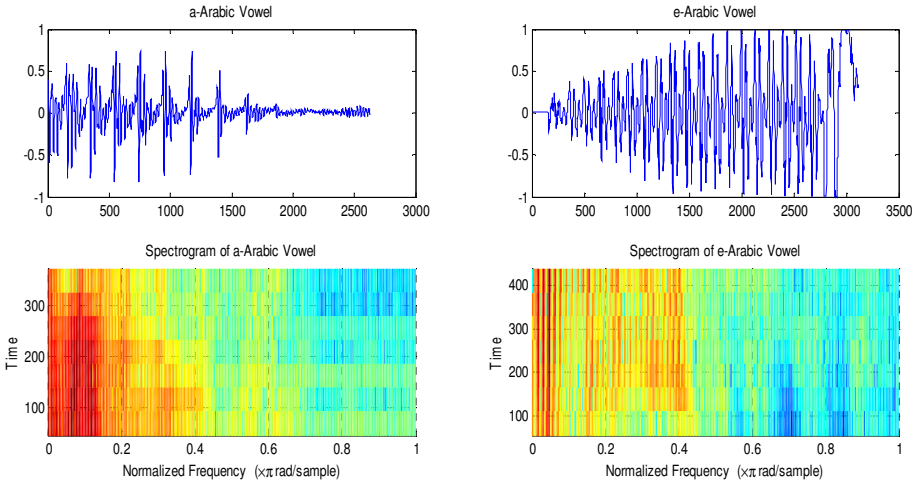


**Figure 2**. First Arabic Vowels of a speaker 2 with spectrogram

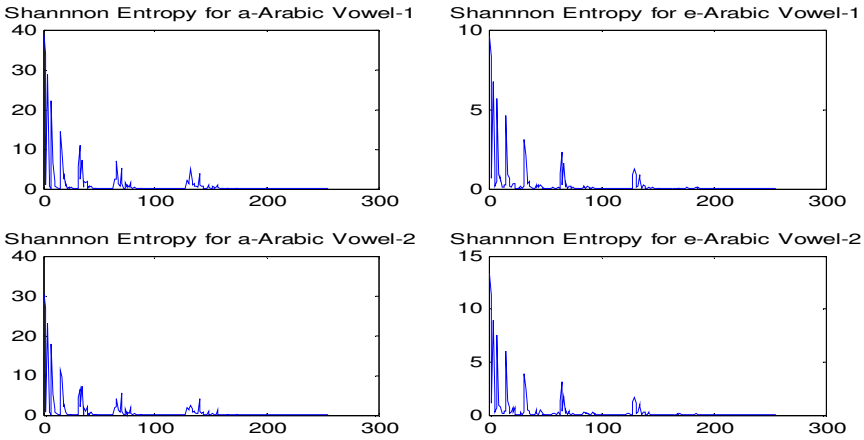


**Figure 3**. Shannon entropy for Arabic vowels presented in Figure 2

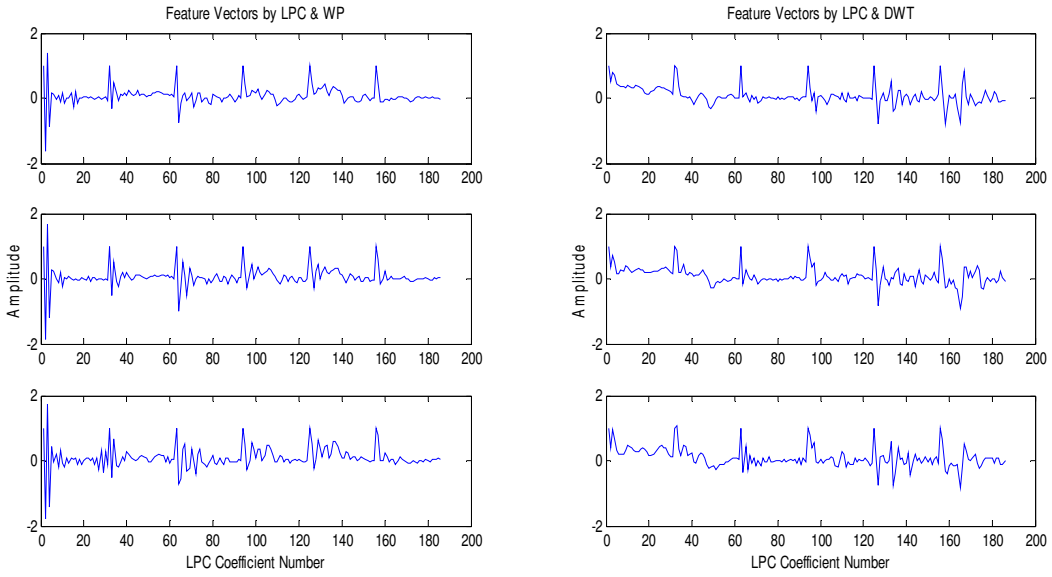


**Figure 4**. WP and DWT with LPC for three utterances of Arabic a-vowel for the same speaker.

## V. CONCLUSION

Feed forward backpropagation neural network based speech recognition system is proposed in this paper. This system was developed using a wavelet feature extraction method. In this work, effective feature extraction method for Arabic vowels system is developed, taking in consideration that the computational complexity is very crucial issue. Trying to enhance the recognition process, three techniques of WT were applied for the feature extraction stage: WP with LPC, DWT with LPC, and WPE. The experimental results on a subset of recorded database showed that feature extraction method proposed in this paper is appropriate for Arabic recognition system. Our investigation of dialect-independent Arabic vowels classifier system performance is performed via several experiments depending on vowel type. The declared results showed that the proposed method can make an effectual analysis with identification rates may reach 100% in some cases.

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# SIMULATION AND ANALYSIS STUDIES FOR A MODIFIED ALGORITHM TO IMPROVE TCP IN LONG DELAY BANDWIDTH PRODUCT NETWORKS

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***ABSTRACT***

*It is well known that TCP has formed the backbone of the Internet stability and has been well tuned over years. Today the situation has changed, that is because the internetworking environment become more complex than ever, resulting in changes in TCP congestion control are produced and still in progress. In this paper we use an analytic fluid approach in order to analyze the different features of slow start, traditional swift start, and modified swift start algorithms. We then use simulations to confirm our analytic results which are promising enough.*

***KEYWORDS:*** *TCP, congestion control, Slow Start and Swift Start algorithms, high-speed networks, long-delay bandwidth product networks.*

## I. INTRODUCTION

Since more than three decades Cerf and Kahn have been initiated in their paper [1] the first work of Transmission Control Protocol (TCP), which originally defined in RFC 793 [2]. However, when a TCP connection is opened and data transmission starts, TCP uses an algorithm known as slow start to probe the network to determine the available capacity over the connection's path. It is well known that the TCP is responsible for detecting and reacting to overloads in the Internet and has been the key to the Internet's operational success in the last few decades. However, as link capacity grows and new Internet applications with high-bandwidth demand emerge, TCP's performance is unsatisfactory, especially in high-speed and long-distance networks. In these networks TCP underutilizes link capacity because of its conservative and slow growth of congestion window. The congestion window governs the transmission rates of TCP [3]. TCP is often blamed that is cannot use efficiently network paths with high Bandwidth Delay Product (BDP). The BDP is of fundamental importance because it determines the required socket buffer size for maximum throughput [4].

The basic implementations of TCP are based on Jacobson's classical slow start algorithm for congestion avoidance and control [5,6]. A number of solutions have been proposed to alleviate the a aforementioned problem of TCP by changing its congestion control algorithm such as BIC-TCP [7], congestion control [8], CUBIC [9], FAST [10], HSTCP [11], H-TCP [12], LTCP [13], STCP [14], TCP-Westwood [15], TCP-Africa [16], fast retransmit, fast recovery [17-20], the new Reno Modification to TCP fast recovery algorithm [21], and Increasing TCP's Initial Window [22] which was evaluated in [23]. All these enhancements were added to TCP congestion control and others are still in progress to avoid unnecessary retransmissions and to enhance the connection efficiency without altering the fundamental underlying dynamics of TCP congestion control [24]. Other congestion control algorithms were suggested for TCP such as the delay-based approach for congestion avoidance [25] and explicit congestion notification (ECN) [26,27].

Technology trends indicate that the future Internet will have a large number of very high bandwidth links such as fiber links, and very large delay satellite links. These trends are problematic because TCP reacts adversely to increases in bandwidth or delay. Mathematical analysis of current slow start TCP congestion control algorithms reveals that, as the delay-bandwidth product increases, TCP bandwidth utilization decreases especially for large delay links. So many other congestion control algorithms were suggested to enhance the performance of TCP of high delay-bandwidth product network such as Fast TCP [18-21], TCP Fast Start [22], Explicit Control Protocol (XCP) [23], High Speed TCP [24], Quick-Start for TCP and IP [25] and others.

## II. BACKGROUND

F. J. Lawas-Grodek and Diepchi T. Tran have tested the results of the Swift Start algorithm in single-flow and multiple-flow test beds under the effects of high propagation delays, various bottlenecks, and small queues sizes. Also, they've estimated the capacity and implements packet pacing; the results were that in a heavily congested link, the Swift Start algorithm would not be applicable. The reason is that the bottleneck estimation is falsely influenced by timeouts included by retransmissions and the expiration of delayed acknowledgment (ACK) timers, the causing their modified Swift Start code to fall back to regular TCP [28]. In the previous work [29-32], we've modified the traditional (original) Swift Start algorithm [33,34] to overcome its drawbacks. However, the modified Swift Start algorithm results have confirmed its succeed in improving the start up connection by quickly estimating to the available bottleneck rate in the connection path, and its performance does not affected when using Delayed Acknowledgment or acknowledges compression.

## III. SLOW START OVER LONG DELAY-BANDWIDTH PRODUCT NETWORKS

Recently there are some researches investigate the congestion control and long delay bandwidth product such as [35-44]. To determine the data flow, the Slow Start TCP uses two main variables, the first is the Congestion Window (CWND) in which the sender-side is limit on the amount of data, and can transmit into the network before receiving an ACKnowledgment (ACK), the second is the Receiver's advertised window (RWND) in which the receiver-side is limit on the amount of outstanding data. The minimum of CWND and RWND governs data transmission. Another state variable is the Slow Start threshold (SSTHRESH), which is used to determine whether the Slow Start or congestion avoidance algorithm is used to control data transmission. When a new connection is established with a host, the congestion window is initialized to a value that is called Initial Window (IW), it equals to one segment. Each time an ACK is received; the CWND is incremented by one segment. So TCP increases the CWND by percentage of 1.5 to 2 each Round Trip Time (RTT). The sender can transmit up to the minimum of the CWND and the RWND. When the congestion window reaches the SSTHRESH the congestion avoidance should starts to avoid occurrence of congestion. The congestion avoidance increases the CWND when receiving an ACK according to equation 1.

$$CWND += SMSS \times SMSS/CWND \quad \ldots\ldots\ldots\ldots (1)$$

*Where:* ***SMSS*** is the sender maximum segment size.
CP uses Slow Start and congestion avoidance until the CWND reaches the capacity of the connection path, and an intermediate router will start discarding packets. Timeouts of these discarded packets informs the sender that its congestion window has gotten too large and congestion has been occurred. At this point TCP reset CWND to the IW, and the SSTHRESH is divided by two and the Slow Start algorithm starts again. However, there are many researches have been done such as fast retransmit; fast recovery [17-20], the New Reno Modification to TCP fast recovery algorithm [21], and increasing TCP's Initial Window [22] were added to TCP congestion control. The current implementations of Slow Start algorithm are suitable for common link which has low-delay and modest-bandwidth. That takes a small time to correctly estimate and begin transmitting data at the available capacity. Meanwhile, over long delay-bandwidth product networks, it may take several seconds to complete the first Slow Start and estimate available path capacity.

# IV. SWIFT START ALGORITHM

The Swift Start algorithm was proposed to improve the TCP connection startup by quickly estimating the path bottleneck capacity and so the congestion window by using packet pair algorithm [45] and using packet pacing [46] to spread out the congestion window over RTT to avoid router buffers over flow. In this algorithm, the TCP connection starts with four-segment (IW = 4) which are sent in burst. However, when the acknowledgements of the segments are received, the sending TCP uses the packet pair algorithm to calculate the bottleneck capacity as follow**:**

$$\mathbf{BW = \Delta t \times SegSize} \quad \ldots\ldots\ldots\ldots \textit{(2)}$$

$$\textit{Capacity = BW x RTT} \quad \ldots\ldots\ldots\ldots \textbf{(3)}$$

*Where:* Δt is the time delay between the arrival time of the acknowledgment of the first and second segment. Also the sending *TCP* uses pacing to spread the packets over the *RTT*.
However, the Swift Start can not work properly when combing it with some other techniques such as Delayed Acknowledgment DACK [47, 48] which is used in mostly all TCP implementations to reduce the number of pure data less acknowledgment packets sent by the receiver. DACK states that the TCP receiver will only send data less acknowledgment for every other received segment. If no segment is received within a specific time, the data less acknowledgment will be sent. The DACK algorithm will directly influence packet pair estimation, because the ACK is not sent promptly, but it may be delayed some time within the receiver, not due to congestion, so the sender can not correctly estimate the available bandwidth. Another problem facing Swift Start is the acknowledgment compression [49, 50], which causes the ACKs to be bunched up in the network path from the data receiver to the data sender. This compression will decrease the time gap between the ACKs which will lead to bandwidth over estimation. The third problem with Swift Start is that the employing packet pair algorithm does not take in account the delay that faces acknowledges in the reverse path. However, to overcome the three drawbacks mentioned above, a simple modification is considered to the original Swift Start algorithm [29-32] which is compared with other congestion control algorithms.

## 4.A. The Modified Swift Start Algorithm

The Modified Swift Start (MSS) algorithm aims to avoid drawbacks with the original Swift Start algorithm by modifying the packet pair algorithm, the idea behind the modification is that instead of time depending on the interval between the acknowledgments that may cause errors, it will use the time between the original messages which will be calculated by the receiver when the original messages arrive it, and then the receiver sends these information to the source when acknowledging it. The sender starts the connection by *CWND* = 4 segment, these packets are send in form of pairs, and identifies the first and the second segment of each pair by First/Second (F/S) flag. When the receiver receives the first message, it will record its sequence number and its arrival time, and it will send an acknowledgment on this message normally according to its setting. When it receives a second one, it will check whether this is the second for the recorded one or not, if it is the second for the recorded one, the receiver will calculate the interval Δt between the arrival time of the second one and the first one using the following equation :-

$$\Delta t = t_seg1 - t_seg2 \quad \mu sec \quad \ldots\ldots\ldots\ldots \textit{(4)}$$

*where: t_seg1* and *t_seg2* are the arrival time of the first and second segments respectively. However, when the receiver sends the second segment's acknowledgment, it will insert the value of Δt into the transport header option field. The sender's *TCP* will extract Δt from the header and calculate the available bit rate *BW* by using the above equation (2).

## 4.B. How does the Modified Swift Start Overcome the Drawbacks?

If the receiver uses the *DACK* technique, it will record the first segment arrival time and wait for another segment, when it receives the second one it will calculate Δt, and whenever it sends an acknowledgment, it will send Δt along with it. However, the *DACK* dos not affect the calculation of

$\Delta t$. Also acknowledgment compression will not affect the calculation of $\Delta t$, because $\Delta t$ is the time gab between the data segment itself. If *ACKs* face a delay in the reverse path, this delay will not affect $\Delta t$. because $\Delta t$ is carried explicitly with in the header and not in the time delay between *ACKs*. However, error sources are avoided and the estimated capacity is the actual capacity without neither over estimation nor under estimation.

### 4.C. Mathematical Analysis

The purpose of the mathematical analysis is to drive a mathematical model to estimate the throughput of the transmission for both MSS (Modified Swift Start) and Slow Start. Since MSS is used to enhance the connection startup, so we would be interest in the slow start phase of the connection, and the difference between the slow start and the MSS in this phase.

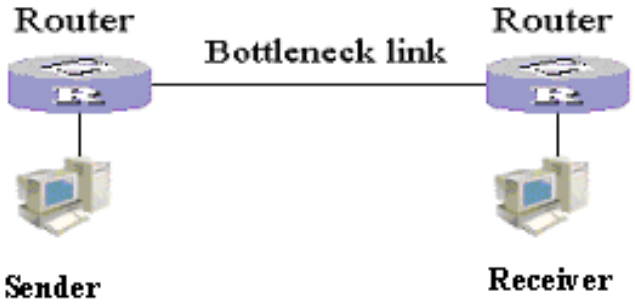


Figure 1: Topology of the network model

Figure 1 shows the topology of the network model that we've used to implement the mathematical analysis. The analysis based on the model driven in [51]. In this analysis we will ignore the 3-way handshaking, and we assume that *RTT* is constant for simplicity. This assumption is used in many researches specially when working in long delay paths, in which queuing delay is very small with respect to propagation delay see [52-54]. The following parameters are used in the analysis.

$CWND_i$ **the** congestion window at the *ith RTT*.
$CWND_1$ the initial congestion window
*b* is a parameter depends on the use of *DACK* where b=1 if *DACK* is disabled and b=2 if *DACK* is enabled
$\gamma$ = 1+1/b
$d_n$ the number of data segments sent in the interval form 0 to n **RTT*
*B* The throughput which is the amount of data sent in a certain time interval from 0 to *n* RTT*.
*C* the bottleneck capacity in Bit/sec.
S The segment size. We assume that all segments have the same length, this happens when the sender always has a data to send.

### 4.D. Slow Start Analysis

In slow start phase
$CWND_{i+1} = CWND_i + CWND_i / b$
$CWND_{i+1} = (1+1/b) * CWND_i$
$CWND_{i+1} = \gamma\ CWND_i$

$$CWND_i = \gamma^{i-1} * CWND_1$$

Let N be the *RTT* in which the congestion window is *CWND*

$$N = Log_{\gamma}\left(\frac{CWND}{CWND_1}\right) + 1 \qquad \ldots\ldots\ldots\ldots (1)$$

$d_n = CWND_1 + CWND_2 + \ldots\ldots + CWND_n$

$d_n = CWND_1 + \gamma CWND_1 + \gamma^2 CWND_1 + .. + \gamma^{n-1} CWND_1$

$$d_n = \sum_{i=1}^{n} CWND_i$$

$$d_n = CWND_1 * \frac{\gamma^n - 1}{\gamma - 1} \qquad \ldots\ldots\ldots\ldots (2)$$

Let N (d) be the number of *RTT* needed to send d segments

$$N(d) = \log_\gamma \left( \frac{d * (\gamma - 1)}{CWND_1} + 1 \right) \qquad \ldots\ldots\ldots\ldots (3)$$

From equation……..(2)

$$d_n = \frac{CWND_1 * \gamma^n - CWND_1}{\gamma - 1}$$

$$d_n = \frac{\gamma * CWND_n - CWND_1}{\gamma - 1} \qquad \ldots\ldots\ldots\ldots (4)$$

$$CWND_i = \frac{d_i (\gamma - 1) + CWND_1}{\gamma} \qquad \ldots\ldots\ldots\ldots (5)$$

Equation (5) was driven in [40].

$B(n) = d_n / (n * RTT)$

$$B(d) = \frac{d_n}{RTT * \log_\gamma \left( \frac{d_n * (\gamma - 1)}{CWND_1} + 1 \right)} \qquad \ldots\ldots (6)$$

And

$$B(CWND) = \frac{CWND_1 \ \frac{\gamma^n - 1}{\gamma - 1}}{RTT * Log_\gamma \left( \frac{CWND_n}{CWND_1} \right)}$$

$$B(CWND) = \frac{\gamma * CWND - CWND_1}{RTT (\gamma - 1) \left( \log_\gamma \left( \frac{CWND}{CWND_1} \right) + 1 \right)} \qquad \ldots\ldots\ldots (7)$$

$$B(n) = \frac{CWND_1}{n * RTT} * \frac{\gamma^n - 1}{\gamma - 1} \qquad \ldots\ldots\ldots\ldots (8)$$

Let Ns be the number of *RTT* in which the *CWIND* reaches the *SSTHRESH*.

$$Ns = \log_\gamma \left( \frac{ssthresh}{CWND_1} \right) + 1$$

In the slow start phase n is the number of *RTT* for *CWND* to reach the *SSTHRESH.*
The amount of data sent before reaching the *SSTHRESH* will be

$$B(SSTHRESH) = \frac{d_{ssthresh}}{RTT * Ns}$$

where: $d_{ssthresh}$ is the number of segments sent until the congestion window reaches *SSTHRESH*
From ……equation (4)

$$d_{ssthresh} = \frac{\gamma * ssthresh - CWND_1}{\gamma - 1}$$

$$B(SSTHRESH) = \frac{\gamma * ssthresh - CWND_1}{RTT\,(\gamma - 1)\left(\log_\gamma\left(\frac{ssthresh}{CWND_1}\right) + 1\right)} \quad \text{……..(9)}$$

When tn > Ts

$$CWND_{i+1} = CWND_i + 1/CWND_i$$

## 4.E. Modified Swift Start

In case of modified swift start let $CWND_1$ is the initial congestion window and the inter arrival delay between the two packets arriving the receiver is τ, the segment size is S. So, after the first *RTT CWND* will be

$$CWND_2 = RTT / \tau$$

Then the TCP will use the slow start to increase the congestion window so: In the model of Figure 1, τ = frame length / C For PPP connections the frame length equals to S + IP_header_length + frame_header_length

$$\tau = 8 * (S+27) / C$$

$$CWND_i = \begin{cases} CWND_1 & i = 1 \\ \gamma^{i-2} * RTT / \tau & i \geq 2 \end{cases}$$

$$d_n = CWND_1 + \frac{RTT}{\tau} * \frac{\gamma^{n-1} - 1}{\gamma - 1} \quad \text{…….…….(10)}$$

For $RTT/\tau \leq SSTHRESH$.

This condition is to grant that the connection is in slow start. Because if $RTT/\tau > SSTHRESH$ the congestion avoidance will start, and the slow start time in this case is only one *RTT.*

$$d_n = CWND_1 + \frac{\gamma * CWND_n - RTT / \tau}{\gamma - 1} \quad \text{……..…(11)} \quad \text{for } n>2$$

From equation (10), the number of *RTTs* needed to send d segments is

$$N(d) = \log_\gamma\left((d - CWND_1)\frac{\tau * (\gamma - 1)}{RTT} + 1\right) + 1$$

$$N(CWND) = \log_\gamma\left(\frac{CWND * \tau}{RTT}\right) + 2$$

$$B(n) = \frac{CWND_1 + \frac{RTT}{\tau} * \frac{\gamma^{n-1} - 1}{\gamma - 1}}{RTT * n}$$

$$B(cwnd) = \frac{CWND_1 + \frac{\gamma * CWND_n - RTT/\tau}{\gamma - 1}}{RTT * \log_\gamma\left(\frac{CWND * \tau}{RTT}\right) + 2 * RTT}$$

$$B(ssthresh) = \frac{CWND_1 + \frac{\gamma * ssthresh - RTT/\tau}{\gamma - 1}}{RTT * \log_\gamma\left(\frac{ssthresh * \tau}{RTT}\right) + 2 * RTT} \quad \text{For } CWND_i \neq CWND_1$$

$$B(d) = \frac{d}{RTT * \left(\log_\gamma\left((d - CWND_1)\frac{\tau * (\gamma - 1)}{RTT} + 1\right) + 1\right)}$$

# V. SIMULATION AND RESULTS.

The Modified Swift Start model has been implemented using Opnet modeler [55], to compare the performance results with that of the original swift start and the slow start in deferent network conditions of bandwidth and path delay. The comparison between them implemented using a single.

## 5.A Single Flow

### 5.A.a) Low Delay-Bandwidth Product Networks

The network model shown in Figure 1 implemented to study the performance of swift start TCP and compare it with the traditional (original) swift start and the slow start using single flow between the sender and the receiver. The sender uses FTP to send a 10 MB file to the receiver. The TCP parameters of both the sender and the receiver are shown in Table-1. In the simulation both the sender and the receiver uses DACK. This configuration has been used to study the difference between the original and modified swift start. The sender and the receiver are connected to the routers through a 100 Mbps Ethernet connections.

Table-1 TCP Parameters of the sender and receiver

| | |
|---|---|
| Maximum Segment Size | 1460 Bytes |
| Receive Buffer | 100000 Bytes |
| Delayed ACK Mechanism | Segment/Clock Based |
| Maximum ACK Delay | 0.200 Sec |
| Slow-Start Initial Count | 4 |
| Fast Retransmit | Disabled |
| Fast Recovery | Disabled |
| Window Scaling | Disabled |
| Selective ACK (SACK) | Disabled |
| Nagle's SWS Avoidance | Disabled |
| Karn's Algorithm | Enabled |
| Initial RTO | 1.0 Sec |
| Minimum RTO | 0.5 Sec |
| Maximum RTO | 64 Sec |
| RTT Gain | 0.125 |
| Deviation Gain | 0.25 |
| RTT Deviation Coefficient | 4.0 |
| Persistence Timeout | 1.0 Sec |

Both of the routers are CISCO 3640 with forwarding rate 5000 packets/second and memory size 265 MB. The two routers are interconnected with point to point link that link is used as a bottleneck by changing its data rate; also the path delay is controlled using this link.
Figure 2 shows the simulation and the analytical results of the congestion window for slow start TCP, traditional and Modified swift start TCP when the bottleneck data rate is 1.544 Mbps (T1) and the path RTT is 0.11674 second, which is low rate, low delay network. First we note some differences between the analytical results and the simulation results, these differences because we use a fixed RTT (RTT=0.11674 sec which is the initial RTT) in the analysis, meanwhile the RTT actually changes according to CWND due to queuing delay. We also note that the difference increases as time increases, this is logical because in the first few RTTs CWND is very small so the RTT is around the initial RTT, however the results are very close in the first few RTTs. Anyway this difference is not important for us because we are concerned on the first few RTTs.

It is clear that the modified swift start is faster and better than slow start TCP in estimating the path congestion window which is = 21929 bytes after only one RTT , then the packet pair is disabled and the slow start runs normally. The estimated congestion window is proportional to the link bandwidth and round trip time it can be calculated as follow: Assuming that packet pair delay deference is D.

CWND = the amount of data that can be sent in RTT

= RTT * MSS / D

Theoretically the packet pair delay deference is the frame length on the bottleneck link, so

D = frame length /link rate + $D_Q$

= (1460+20+7) * 8 / 1544000 = 0.007705 sec

And RTT is measured for the first pair (RTT = 0.11674 sec)

So CWND=0.11674*1460/0.007705=22120.75 bytes

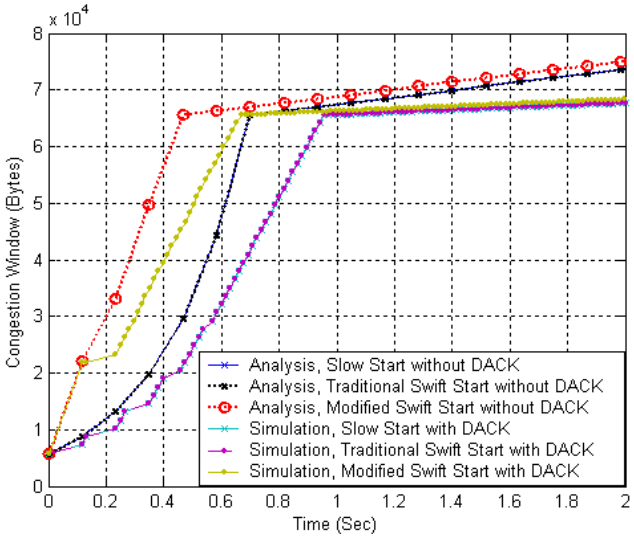


Figure 2 Congestion window for BW = 1.5 Mbps and path RTT= 0.11674 Sec

Obviously, the result in the simulation shows that the delay difference is 0.007772 sec and the CWND is 21929 bytes, these results are very close to the mathematical results. This difference between the results because in the calculation we've neglected the processing delay which may affect the value of D and so decrease CWND. The simulation also shows that after estimating the congestion window in the first RTT, the swift start stopped and the slow start runs normally, Figures 3-a and 3-b show the sent segment sequence number for this connection. It is shown that the three algorithms start the connection by sending 4 segments, after 1 RTT (0. 11674 sec) each of the slow start and traditional (original) swift start send 6 segments with in the second RTT, while the modified swift start send a

large number of segments because of its large congestion window which is 21929 bytes which is about 14 segments, these segments were paced along the second RTT, until the sender receives an other ACK that indicates that the end of the second RTT and the beginning of the third RTT, at this time the pacing was stopped and the slow start was used to complete the connection.
In Figure 3-a shows that after a certain time both algorithms reaches a constant transmission rate, we roughly calculate this rate, Transmission rate = 187848 bytes / sec

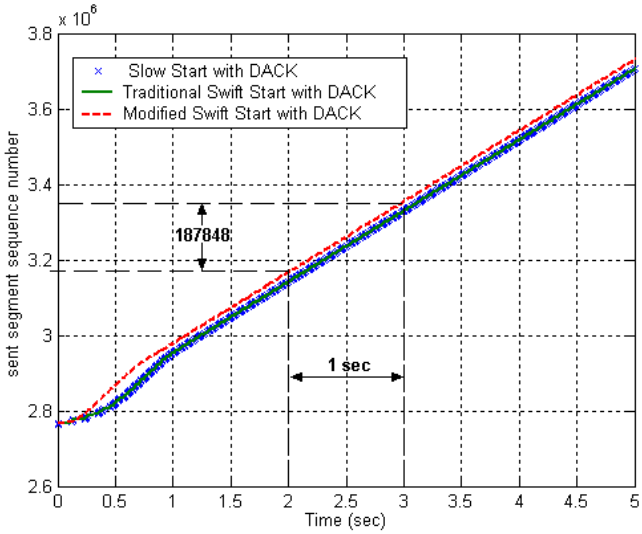


Figure 3-a the sent segment sequence number for BW = 1.5 Mbps and path RTT= 0.11674 Sec

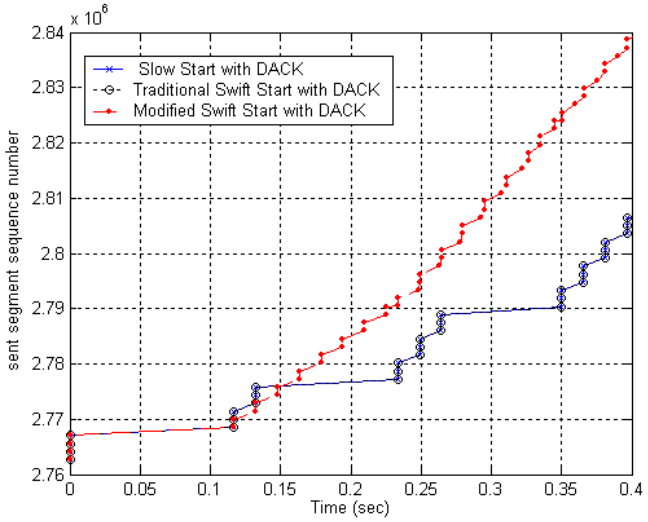


Figure 3-b the sent segment sequence number for BW = 1.5 Mbps and path RTT= 0.11674 Sec

### 5.A.b) Low Bandwidth, Long Delay networks

We've also tested the traditional and modified swift start models on this connection with the same bandwidth but with longer delays to check the performance for long delay paths. For link delay 0.1 sec the RTT was 0.31343 sec, and the estimated CWND was 58878 bytes a. Figure 4 shows the congestion window for this connection, it's clear that the modified swift start is faster than slow start.

### 5.A.c) High Bandwidth Networks

To compare between the three algorithms on high bandwidth networks we've used the same model in Figure 1 with PPP link of rate OC1 (518400000 bps) and with different RTT. First we check for short RTT to test low delay–high bandwidth networks. We've checked for RTT= 0. 07307 sec.

Figure 4 shows the congestion window for this connection; we've noted that the large congestion window which equals 460867 bytes which was estimated by the modified swift start TCP. This congestion window can be calculated as follow

CWND = RTT * *MSS / D*

*D = (1460+20+ 7) * 8 / 51840000 = 0.0002295 sec*

*CWND = 0.07307 * 1460 / 0.0002295 = 464846 bytes*

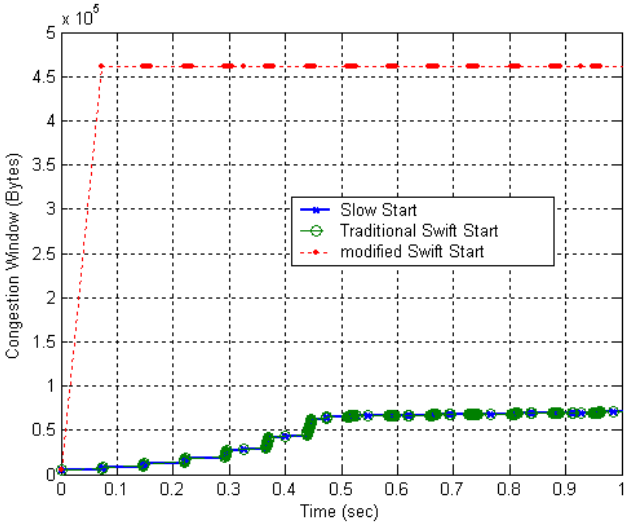


Figure 4 Congestion window for BW = OC1 Mbps and path RTT= 0.07327 Sec

Figure 5 shows the sent sequence number for this connection, also, shows the effect of large congestion window on the traffic sent in the second RTT slow start transmits six segments only while modified swift start send a bout 44 segments, that's equal to the maximum RWIND.

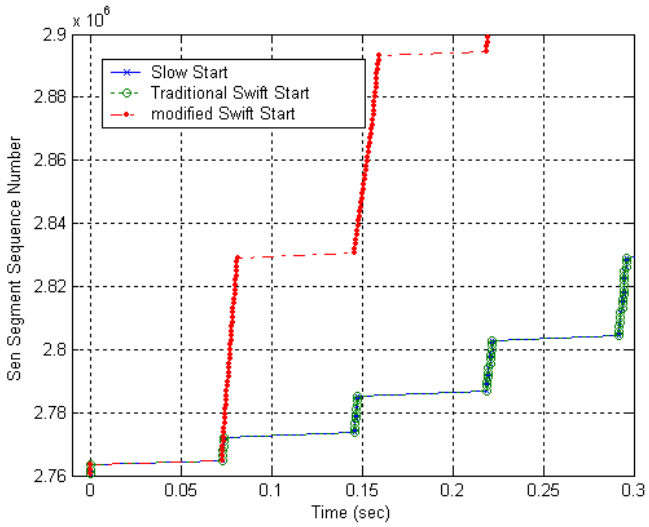


Figure 5 the sent segment sequence number for BW = OC1 Mbps and path RTT = 0.07327 Sec.

## VI. CONCLUSION

The paper presents methods of simulation and analysis for the slow start, traditional and modified swift start algorithms. The results are compared and confirm that the modified algorithm promised

enough. We've to mention here that the modified swift start algorithm maintains the core of current TCP.

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http://ehab.a.khalil.50megs.com or http://www.menofia.edu.eg/network_administrtor.asp

# MULTI-PROTOCOL GATEWAY FOR EMBEDDED SYSTEMS

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***ABSTRACT***

*The embedded systems are highly optimized to perform limited duties of particular needs. They can be control, Process, medical, signal, and image processing applications. The challenges faced by embedded systems are security, real-time, scalability, high availability and also performance based interoperability as more and more different devices are added to the systems. These complex ubiquitous systems are glued together with layers of protocols. Networking of these is a task to look for with minimum flaws in manageability, synchronization and consistency. We have attempted to design a gateway to interconnect UART with SPI, I2C and CAN Protocols. The design can be adopted for various embedded real-time applications and gives the flexibility of protocol selection.*

***KEYWORDS:*** *Real-Time Systems; Communication Protocols; Gateway and Embedded Systems.*

## I. INTRODUCTION

Embedded systems perform limited duties as they are highly optimized for a particular need. More complex applications can be solved by embedded systems with the integration of different kinds of peripherals. The range of hardware used in embedded systems reaches from FPGAs to full blown desktop CPUs which are accompanied by special purpose ICs such as DSP Processors. On the software side, depending on the needs, everything from logic implementation to systems with own operating system and different applications running on it can be found. The grand challenge is design of integrated system architecture for ultra-reliable systems demanded by the society. Rechtin [1] defines ultra-reliability as a level of excellence so high that measuring it with confidence is close to impossible. Yet measurable or not, it must be achieved otherwise the system will be judged a failure.

The fast growth of electronic functions has led to many insular solutions that prevented comprehensive concepts from taking hold in the area of electrical/electronic architectures. Now a phase began with a marked development of electrical/electronic structures and associated networking topology from a comprehensive perspective. This meant that electrical/electronic content and its networking could claim an undisputed position in the complex systems. The recognition that many functions could only be implemented sensibly with the help of electronics also prevailed. So the image of electronics transformed from being a necessary evil to being a key to new, interesting and innovative functions. These functions must communicate with one another over a complex heterogeneous network. These networks typically contain multiple communication protocols including the industry standard Universal Asynchronous Receive/Transmit (UART), Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I2C), Controller Area Network (CAN), Local Interconnect Network (LIN), TTP/C and the recently developed FlexRay.

Previously chip-to-chip communications used many wires in a parallel interface, often ICs to have 24, 28, or more pins. Many of these pins were used for inter-chip addressing, selection, control, and data transfers. In a parallel interface, 8 data bits are typically transferred from a sender IC to receiver ICs in a single operation. The introduction of serial communication has led to reduction in real estate required on the board i.e., saving both cost and space.

The UART is a circuit that sends parallel data through a serial line. UARTs are frequently used in conjunction with the EIA (Electronic Industries Alliance) RS-232 standard, which specifies the

electrical, mechanical, functional, and procedural characteristics of two data communication equipments. Some interconnects require their own voltage levels and format of digital data like communication to some flash memories, EEPROM, sensors and actuators. The efficient protocol for the particular IC has to be used with interface.

The basic principle and format of protocols used in the gateway are presented in the next section. In the section 3 we describe the board over which the gateway is designed and the results obtained and finally in section 4 the paper is concluded.

# II. ON-BOARD PROTOCOLS

The protocols used for making a gateway are discussed in brief about their principle and formats.

## 2.1. Universal Asynchronous Receive/Transmit (UART)

UART is used along with industry standard RS-232. Because of the voltage levels defined in RS-232 are different from that of IC I/O on the board, a voltage converter chip (MAX232) is needed between a serial port and an IC I/O pins as illustrated in figure 1.

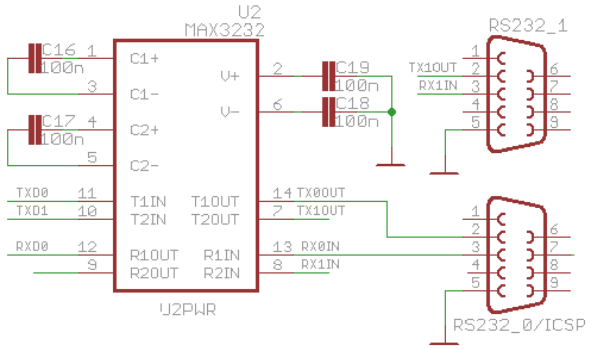


Figure. 1 Converter IC between RS232 and other ICs.

A UART includes a transmitter and a receiver. The basic functions of a UART are a microprocessor interface, double buffering of transmitter data, frame generation, parity generation, parallel to serial conversion, double buffering of receiver data, parity checking, and serial to parallel conversion. The frame format used by UARTs is a low start bit, 5-8 data bits, optional parity bit, and 1 or 2 stop bits. The frame format for data transmitted/received by a UART is given in Figure 2. No clock information is conveyed through the serial line. Before the transmission to start, the transmitter and receiver must agree on the set of parameters in advance, which include the baud rate, the number of data bits, stop bits, and the use of parity bit. The commonly used baud rates are 2400, 4800, 9600 and 19200 bauds. We should always have the same baud rates as in the PC and in the UART.

The baud rates are calculated as follows:

$$\text{Baud rate} = f_{PCLK1} / (16*BRR),\ BRR = f_{PCLK1} / (16*\text{Baud rate})$$

For example, in our application, we used 9600 as baud rate, and the $f_{PCLK1}$ is 8 MHz.

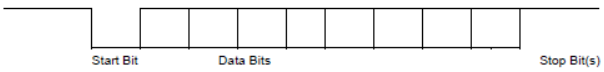


Figure 2 frame format for UART data

## 2.2. Serial Peripheral Interface (SPI)

So, what is SPI? SPI is a very simple serial data protocol. This means that bytes are send serially instead of in parallel. SPI is a standard protocol that is used mainly in typical embedded systems. It

falls in the same family as I2C or RS232. SPI is primarily used between micro-controllers and their immediate peripheral devices. It's commonly found in cell phones, PDA's, and other mobile devices to communicate data between the CPU, keyboard, display, and memory chips.
The SPI (Serial Peripheral Interface)-bus is a master/slave, 4-wire serial communication bus. The four signals are clock (SCLK), master output/slave input (MOSI), master input/slave output (MISO), and slave select (SS). Whenever two devices communicate, one is referred to as the "master" and the other as the "slave". The master drives the serial clock. Data is simultaneously transmitted and received, making it a full-duplex protocol. Rather than having unique addresses for each device on the bus, SPI uses the SS line to specify which device data is being transferred to or from. As such, each unique device on the bus needs its own SS signal from the master. If there are 3 slave devices, there should be 3 SS leads from the master, one to each slave as shown in Figure 3.

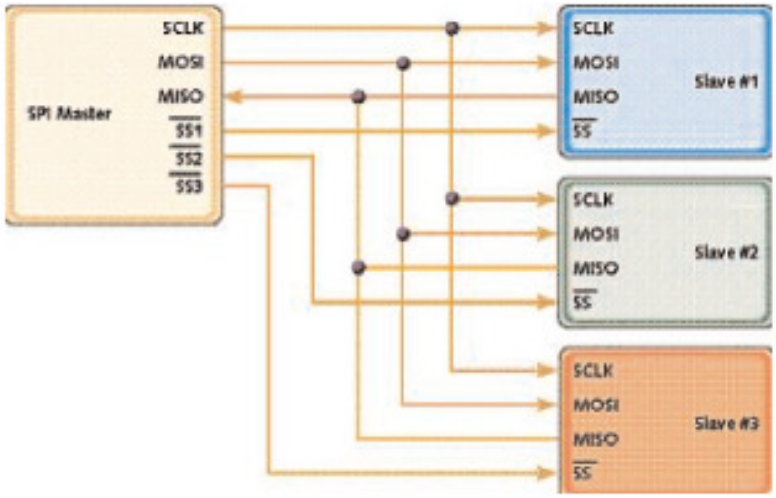


Figure 3: common SPI configuration

This means there is one master, while the number of slaves is limited by the number of chip select lines. When an SPI data transfer occurs, an 8-bit data word is shifted out of MOSI while a different 8-bit data word is being shifted in on MISO. This can be viewed as a 16-bit circular shift register. When a transfer occurs, this 16-bit shift register has shifted 8 positions, thus exchanging the 8-bit data between the master and slave devices. A pair of registers, clock polarity (CPOL) and clock phase (CPHA) determine the edges of the clock on which the data is driven. Each register has two possible states which allows for four possible combinations, all of which are incompatible with one another. So a master/slave pair must use the same parameter values to communicate. If multiple slaves are used that are fixed in different configurations, the master will have to reconfigure itself each time it needs to communicate with a different slave [2].

### 2.3. Inter-Integrated Circuit (I2C)

Inter-Integrated Circuit (I2C) bus provides good support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. I2C is easy to use for linking multiple devices together since it has a built-in addressing scheme. Philips originally developed I2C for communication between the devices inside of a TV set. Examples of simple I2C-compatible devices found in embedded systems include EEPROMs, thermal sensors, and real-time clocks. I2C is also used as a control interface to signal processing devices that have separate, application-specific data interfaces. For instance, it's commonly used in multimedia applications, where typical devices include RF tuners, video decoders and encoders, and audio processors. In all, Philips, National Semiconductor, Xicor, Siemens, and other manufacturers offer hundreds of I2C-compatible devices [3].

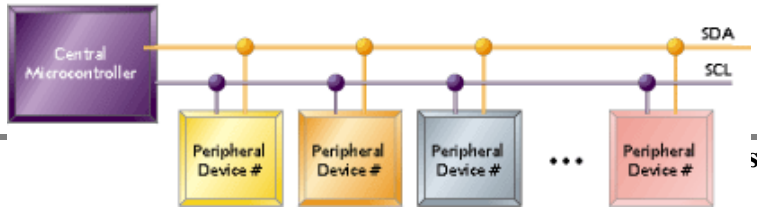

Figure 4: I2C is a two-wire serial bus

The I2C bus uses a bi-directional Serial Clock Line (SCL) and Serial Data Lines (SDA) as shown in figure 4. Both lines are pulled high via a resistor (Rp)(see figure 5). Resistor Rs is optional, and used for ESD protection for 'Hot-Swap' devices. Three speed modes are specified: Standard; 100kbps, Fast mode; 400kbps, High speed mode 3.4Mbps. I2C, due to its two-wire nature (one clock, one data) can only communicate in half-duplex mode. The maximum bus capacitance is 400pF, which sets the maximum number of devices on the bus and the maximum line length. The interface uses 8 bit long bytes, MSB (Most Significant Bit) first, with each device having a unique address. Any device may be a Transmitter or Receiver, and a Master or Slave. Data and clock are sent from the Master; data is valid while the clock line is high. The link may have multiple Masters and Slaves on the bus, but only one Master may be active at any one time. Slaves may receive or transmit data to the Master. $V_{DD}$ may be different for each device, but all devices have to relate their output levels to the voltage produced by the pull-up resistors ($R_P$).

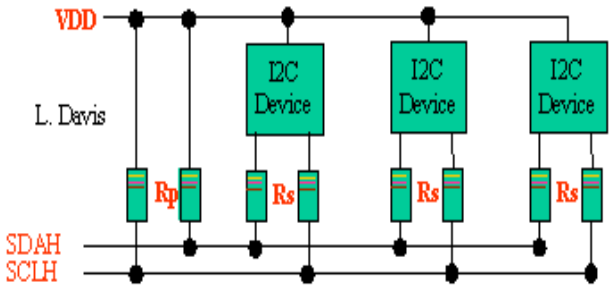


Figure 5: I2C Circuit

As you can see in Figure 6, the master begins the communication by issuing the start condition (S). The master continues by sending a unique 7-bit slave device address, with the most significant bit (MSB) first. The eighth bit after the start, read/not-write (R/ώ), specifies whether the slave is now to receive (0) or to transmit (1). This is followed by an ACK bit issued by the receiver, acknowledging receipt of the previous byte. Then the transmitter (slave or master, as indicated by the bit) transmits a byte of data starting with the MSB. At the end of the byte, the receiver (whether master or slave) issues a new ACK bit. This 9-bit pattern is repeated if more bytes need to be transmitted.

Figure 6: I2C's communication format

In a write transaction (slave receiving), when the master is done transmitting all of the data bytes it wants to send, it monitors the last ACK and then issues the stop condition (P). In a read transaction (slave transmitting), the master does not acknowledge the final byte it receives. This tells the slave

that its transmission is done. The master then issues the stop condition. The I2C signaling protocol provides device addressing, a read/write flag, and a simple acknowledgement mechanism. There are a few more elements to the I2C protocol, such as general call (broadcast) and 10-bit extended addressing. Beyond that, each device defines its own command interface or address-indexing scheme. Most often, the I2C master is the CPU or microcontroller in the system. Some microcontrollers even feature hardware to implement the I2C protocol [4].

## 2.4. Controller Area Network (CAN)

In the mid–1980s, the third party supplier Bosch developed the Controller Area Network (CAN), It was first integrated in Mercedes production cars in the early 1990s. Today, it has become the most widely used network in automotive systems and it is estimated [5] that the number of CAN nodes sold per year is currently around 400 million (all application fields). Today almost every automobile manufacturer uses CAN controllers and networks to control devices such as: windshield wiper motor controllers, rain sensors, airbags, door locks, engine timing controls, anti-lock braking systems, power train controls and electric windows, to name a few. Due to its electrical noise tolerance, minimal wiring, excellent error detection capabilities and high speed data transfer, CAN is rapidly expanding into other applications such as industrial control, marine, medical, aerospace and more.
The CAN bus is a balanced (differential) 2-wire interface running over a Shielded Twisted Pair (STP), Un-shielded Twisted Pair (UTP), or ribbon cable. Each node uses a Male 9-pin D connector. Non Return to Zero (NRZ) bit encoding is used with bit stuffing to ensure compact messages with a minimum number of transitions and high noise immunity. The CAN Bus interface uses an asynchronous transmission scheme where any node may begin transmitting anytime the bus is free. Messages are broadcast to all nodes on the network. In cases where multiple nodes initiate messages at the same time, bitwise arbitration is used to determine which message is of higher priority.
The standard CAN data frame can contain up to 8 bytes of data for an overall size of, at most, 135bits, including all the protocol overheads such as the stuff bits as shown in figure below.

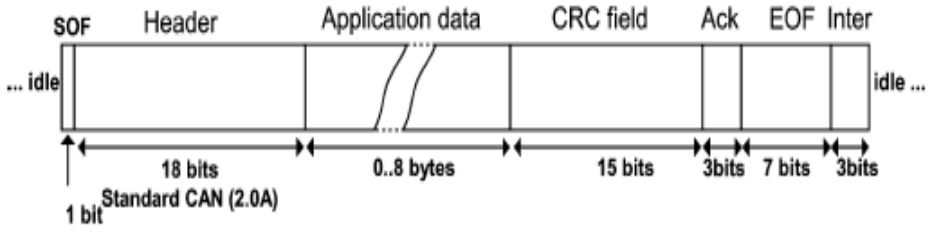


Figure 7: format of CAN data frame

The sections of the frames are:

- The header field , which contains the identifier of the frame, the remote transmission request (RTR) bit that distinguishes between data frame (RTR set to zero) and data request frame (RTR set to 1) and the data length code (DLC) used to inform of the number of bytes of the data field.
- The data field, having a maximum length of 8 Bytes.
- The 15-bit cyclic redundancy check (CRC) field, which ensures the integrity of the data transmitted.
- The Acknowledgment field (Ack). On CAN, the acknowledgment scheme solely enables the sender to know that at least one station, but not necessarily the intended recipient, has received the frame correctly.
- The end-of-frame (EOF) field and the intermission frame space, which is the minimum number of bits separating consecutive messages.

In CAN, number of different data rates is defined, with 1Mb/s being the fastest, and 5kb/s the slowest. All modules must support at least 20kb/s. Cable length depends on the data rate used. Normally, all

devices in system transfer information at uniform and fixed bit rates. The maximum line length can be thousands of meters at low speeds; 40 meters at 1Mbps is typical. Termination resistors are used at each end of the cable [6].

# III. THE GATEWAY

Real-time applications are typically more difficult to design than non-real-time applications. Real-time applications cover a wide range, but most real-time systems are *embedded*. Small systems of low complexity are designed with loops that calls modules to perform the desired functions/operations. Interrupt service routines (ISR) handle asynchronous events and critical operations must be performed by ISRs to ensure that they are dealt with in a timely fashion. Because the execution time of typical code is not constant, the time for successive passes through a portion of the loop is nondeterministic. Furthermore, if a code change is made, the timing of loop is affected [7].
As different protocols have their own advantages and disadvantages to reckon with, the attempt has been made to define a gateway which will suffice the need for a particular system using components suitable to it [8]. The design is implemented and tested by using ARM7 RISC processor. The ARM7 board consist of two CAN nodes, a SPI and an I2C node. The data is fed through the keyboard via PS2 port or through the 'hyper terminal' (UART) and the respective data is displayed on the LCD which is communicating through I2C protocol. However, the available on-chip communication ports of ARM7 are utilized. The block schematic of the design is shown in figure 8.

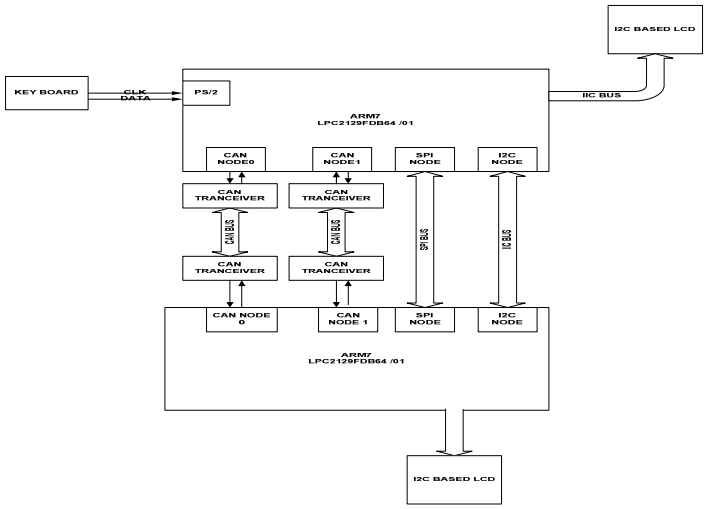

Figure 8: Block schematic of the gateway design

The MCP2551 CAN transceiver is used to serve as interface between a CAN node and the physical bus. The data to be transferred is first loaded into a wrapper, a memory, (LPC2129 16KB SRAM is used), then this is loaded into the data register and the data to be transferred through a particular protocol is selected. The data should be transferred in the format of desired protocol so the frame generator will attach the data in that frame and in the mean time baud rate synchronisation is taken care. For simplicity the baud rate chosen here is 9600. The whole frame is broken down into bytes and then transmitted serially. When frame transmission is complete the receiver takes an appropriate action for checking, analysing and acknowledging the receipt. The data received is stored in message RAM for analysis, in which three control signals are checked for frame start time, ready for reading and end of the frame data. Once the frame reception in complete the mode of frame analysis is changed to write from read. In the second phase the frames are read out of the desired protocol port. For transmission through that port the data can be placed in the frame format of the desired node.

# IV. RESULTS AND DISCUSSION

The figures 9, 10, 11 and 12 are the snap shots describing the connections made and the results obtained for communication through I2C, SPI and CAN respectively. The figure 9 is setup for connection to the hyper terminal and the figure 10 is the connection of I2C nodes and the data to be transmitted is displayed on the two row LCD display.

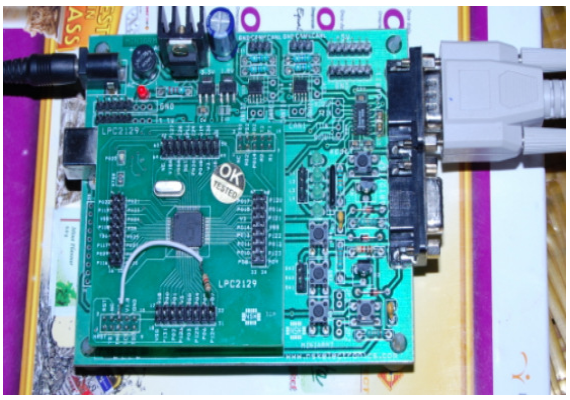

Figure 9: board connections to the UART

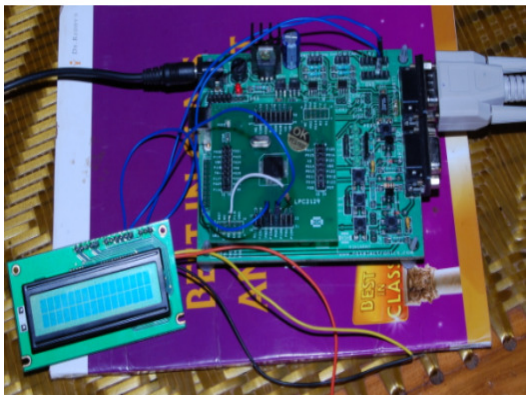

Figure 10: Communication through I2C

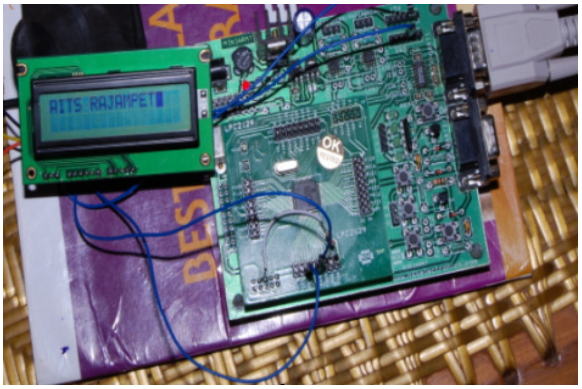


Figure 11: Communication through SPI

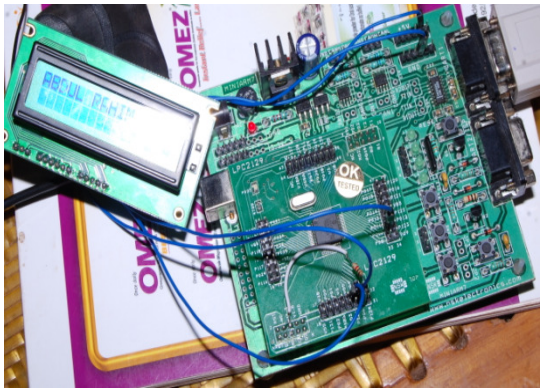

Figure 12: Communication through CAN Bus

The figure 11 shows the connection to SPI node and the data transfer is displayed "AITS RAJAMPET" which was typed in PC, transferred through hyper terminal and from the board 1 to board 2, the transmission is through SPI. Similarly the figure 12 shows the communication through CAN bus and the data transferred "ABDUL RAHIM" is displayed. The selection procedure can be GUI based or in the switch modes.

## V. CONCLUSIONS AND FUTURE SCOPE

The multi-protocol integration for an embedded system is developed and tested. The protocols have been serial communicating as they are regularly used in embedded boards. UART is tested by interfacing the main embedded board with the computer. I2C drivers are developed to read the RTC and displayed on LCD. The SPI drivers were developed to interface memory in which the data typed is stored. As this is interfacing the devices of smaller size, power or low I/O count, makes application in the portable systems [9]. And lastly CAN drivers are developed and tested for data transfer from one transceiver to another. The gateway is developed and tested for trans-communication between UART to UART or I2C or SPI or CAN.

The gateway is very useful in communicating between one protocol to another protocol in a heterogeneous systems as the embedded systems are. For example mobile phones, the data typed by using one protocol and transmit & displayed on the LCD this is another protocol. The protocols

selected for implementation are event triggered and they are non deterministic used in non-critical applications. For Safety critical applications like brake-by-wire, steer-by-wire, etc., these protocols are inefficient and hence time-triggered protocols should be used (like, TTP/C, Flexray etc). In future I look forward to implementation with these protocols also.
The known difficulty in time triggered protocols being the clock synchronization of the nodes used as well as the description in scheduling the process in deterministic approach requires more stable clock. Since most of the time triggered protocols adopt TDMA technique the added components increase the size and cost of implementation [10]. The time triggered protocols are designed for hard real-time embedded systems, hence strict designed accuracy is required as compared to the on designed above, which is basically for soft real-time embedded systems.

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# MULTI-CRITERIA ANALYSIS (MCA) FOR EVALUATION OF INTELLIGENT ELECTRICAL INSTALLATION

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***ABSTRACT***

*Because the electrical installations are nowadays a lot of options and variants, it is necessary to evaluate these complex installation process from several perspectives and objectively. Due to the complexity of evaluation of electrical installation is design a methodology that uses multi-criteria analysis - MCA.*

***KEYWORDS:*** *Intelligent wiring system, Classical wiring system, Economic evaluation*

## I. INTRODUCTION

Companies today offer almost the same range of products for intelligent electrical installation, based mostly on three main bus standards – KNX, LON and Nikobus. The basic requirements include operating system installations and lighting, wiring socket, visualization, control heating, cooling and ventilation, control of blinds, awnings, blinds and curtains, windows, doors, gates and gateways, optimizing energy consumption and working with electronic security system and fire signalling. Most companies dealing with electrical installation system offers these features and differ mostly only premium features, price, etc., but the basic idea remains the same - increased comfort, safety and energy saving. [2, 7]

To be selected the best electrical installation, you need to use the appropriate method for evaluation of the alternatives from which to choose - a multi-criteria analysis. However, this method encompass all the criteria under which it would be possible to assess the installation options, it would be appropriate to prepare an independent scientific work or study dealing with the analysis based on a large set of relevant criteria established by experts or a group of designers who are dedicated to design intelligent systems, and conventional wiring. In this study, it would be possible to pay attention to general set of smart wiring, or a classic set where they are both variants of wiring so that it is possible to choose the best option for the specified criteria.

Work is due to clarity divided into smaller units. First introduced to the basic idea of the MCA and is a defined option of electrical installation. For the analysis is selected method - weighted SUM-WSA, which is described in another part of the work. The main part is an analysis of options of the electrical installation using this method and quantitative method of paired comparisons of criteria.

## II. MULTICRITERIA ANALYSIS

Multi-criteria analysis (multi-criteria decision making) is selected as one of the options listed in that situation potentially viable options on the basis of large number of criteria.

In addition to formulating a list of indirect objective of the analysis is necessary to have a list of options from which the decision will be selected. This list can be specified explicitly as a final list of options or implied terms of specifications, which must comply with the decision option that could be deemed admissible. [5, 8]

If there is available a list of decision criteria as well as a list of options, it is necessary to consider what form should have the final decision. Multi-criteria analysis basically is instrumental to simulation of decision-making situations in which is defined set of alternatives and group of criterions for evaluation of options. The general procedure involves the MCA at the level of resolution selected five relatively independent steps [5]:

- A purpose-oriented set of evaluation criteria
- Establishment of evaluation criteria weights
- Determine the standard values of criteria weights
- Partial evaluation of options
- Choosing the best option or sorting options

To describe a design methodology for evaluation by the MCA, however, will suffice these defined versions, see. Table 1.

Table 1.Options of electrical installation.

| **Functions** | **Option** | | | |
|---|---|---|---|---|
| | **A** | **B** | **C** | **D** |
| Installation devices for switching and protection | o | o | o | o |
| **Socket wiring** | | | | |
| Sockets for normal consumption | o | o | o | o |
| Sockets - Kitchen | o | o | o | o |
| Sockets with surge protection | o | o | o | o |
| **Lighting control** | | | | |
| Lighting control switching | o | o | o | o |
| Lighting control dimming | - | - | o | o |
| Lighting control - PIR detectors | - | - | - | o |
| Link light on the twilight switch | - | - | - | o |
| Lighting scenes | - | - | - | o |
| **Control of heating, air conditioning - AHU** | | | | |
| Conventional heating control thermostat | o | o | o | o |
| Heating control actuators Alpha 0-10V | - | - | o | o |
| AHU Performance Management | - | - | o | o |
| Monitoring of emergency conditions AHU | - | - | o | o |
| Management flue chimney | - | - | - | o |
| Control of under floor heating according to MRC | - | - | - | o |
| Ventilation of bathrooms and toilets | o | o | o | o |
| **Control of shutters, blinds** | | | | |
| Shutter control switch | o | o | o | o |
| Control of external blinds | - | - | o | o |
| Complete control of external shutters | - | - | - | o |
| Adjust of lugs | - | - | - | o |
| **Security system, AV systems** | | | | |
| IA (Intruder Alarm) | o | o | o | o |
| FA (Fire Alarm) | o | o | o | o |
| Integrated IA | - | - | o | o |
| Integrated FA | - | - | o | o |
| TV | o | o | o | o |
| **RF control** | | | | |
| Link to external panel EZS | - | - | - | o |
| Elect. lock the front door - RF | - | - | - | o |
| Control garage door - RF | - | - | - | o |
| **User Interface** | | | | |
| Communication with the user via the GSM | - | - | o | o |
| Managing and monitoring the entire system - SCADA / HMI Reliance | - | - | - | o |
| Visualization - LCD Touch Panel | - | - | - | o |
| Software Win Home Server | - | - | - | o |

### 2.1 Determination of standard values of the criteria

Defining of the set of sample values of the criteria usually associated with the term standard. Standard can be understood in two ways:

- detail the nature of the processed object - a model with which they are rated more options compared in order to obtain a copy of this object
- character building - a model solution, the properties are deliberately reduced to the essential properties of an object and these are compared in ratings [9]

### 2.2. Partial evaluation of options

Evaluation whether an option under consideration meets certain way and to some extent, the desired objectives. The subject of evaluation is the degree of compliance with the objectives considered variants as individual criteria. There are several possible ways and methods to assess the resulting variations. The basic procedure for the partial evaluation is partial evaluation of alternatives and the synthesis of sub-evaluation of options in their overall evaluation. [9]

### 2.3. Multicriteria evaluation methods

Most methods of multicriteria evaluation of options require cardinal information about the relative importance of criteria that can be expressed using the vector weights of the criteria. The weights of the criteria defined above using the paired comparison of quantitative criteria and subsequent lines of geometric mean. For more extensive processing of multi-criteria analysis of options would be appropriate wiring method as a weighted SUM - WSA. [9]

### 2.3.1. Method weighted SUM-WSA

Weighted sum method requires cardinal information criterial matrix Y and vector v constructs the weights of the criteria for overall assessment of each variant, so it can be used to search for one best option, and for ordering options from best to the worst. The method of weighted sum method is a special case of utility functions. Reaches a variant according to criteria j ai certain value $y_{ij}$, brings the user benefits that can be expressed by a linear function of utility. First created normalized criterial matrix R = ($r_{ij}$), whose elements are obtained from criterial matrix Y = ($y_{ij}$), using the transformation formula, [5]:

$$r_{ij} = \frac{Y_{ij} - D_j}{H_j - D_j} \qquad (1)$$

In the previous formula, a linear transform criteria values so that $r_{ij} \in \langle 0,1 \rangle$, $D_J$ criteria corresponding to the minimum value in column j a $H_j$ corresponds to the maximum value of the criteria in column j. The pre-conditions is that the criterion to maximize the column j-col.
Criterion matrix Y=($y_{ij}$). In this table correspond to columns and rows defined criteria ranked options. The matrix can be written as [5]:

$$\begin{array}{c} \\ a_1 \\ a_2 \\ \vdots \\ a_k \end{array} \begin{array}{c} \begin{array}{cccc} f_1 & f_2 & \cdots & f_k \end{array} \\ \begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1k} \\ y_{21} & y_{22} & \cdots & y_{2k} \\ \vdots & & & \\ y_{p1} & y_{p2} & \cdots & y_{pk} \end{bmatrix} \end{array} \qquad (2)$$

When using an additive form of multi-criteria utility function is then equal to the option, [5] :

$$u(a_i) = \sum_{j=1}^{k} v_j \cdot r_{ij} \qquad (3)$$

The option, which reaches a maximum value of utility, $u_i$ is chosen as the best, or can be arranged based on their declining value of the benefits. [5]

### 2.4. Quantitative method of paired comparisons of criteria

This method uses the so-called Saaty matrix S=($s_{ij}$), where i, j = 1,2 ,..., k where $s_{ij}$ represent matrix elements, which are interpreted as estimates of the proportion of weights of the i-th and j-th criterion. The scale is determined by the values 1,2,3 ,..., 9 and the reciprocal values. The corresponding value of the verbal scale:
1 - equivalent to the criteria i and j

3 - slightly preferred the criterion i j
5 - strongly preferred the criterion i j
7 - strongly preferred the criterion i j
9 - absolutely preferred criterion i j
A value of 2, 4, 6, 8 represent intermediate steps. In our case, for simplification, the intermediate stage is unused.
For creation of Saaty matrix we define criteria $f_1$, $f_2$ ,..., $f_k$. Mutual comparison of these criteria, according to the above scale is created by a set of elements $s_{ij}$ Saaty matrix $S=(s_{ij})$. [9]
General registration Saaty matrix [5]:

$$\begin{array}{c} \\ f_1 \\ f_2 \\ \vdots \\ f_k \end{array} \begin{array}{c} \begin{array}{cccc} f_1 & f_2 & \cdots & f_k \end{array} \\ \begin{bmatrix} 1 & s_{12} & \cdots & s_{1k} \\ 1/s_{12} & 1 & \cdots & s_{2k} \\ \vdots & & & \\ 1/s_{1k} & 1/s_{2k} & \cdots & 1 \end{bmatrix} \end{array} \qquad (4)$$

Saaty matrix defined for the analysis of the various wiring options. The sample is designed to create the basic criteria of the matrix and subsequent analysis. [5, 9, 6]

Table 2.Saaty matrix.

| | **Acquisition costs** | **Operating costs** | **Saving energy** | **System maintenance** | **The possibility of heating** | **The possibility of lighting control** | **Reliability** | **Complexity of installation** | **Aesthetics** |
|---|---|---|---|---|---|---|---|---|---|
| **Acquisition costs** | 1 | 5 | 3 | 9 | 3 | 3 | 5 | 7 | 9 |
| **Operating costs** | 0,20 | 1 | 1 | 5 | 3 | 3 | 7 | 3 | 7 |
| **Saving energy** | 0,33 | 1,00 | 1 | 9 | 5 | 5 | 5 | 9 | 7 |
| **System maintenance** | 0,11 | 0,20 | 0,11 | 1 | 1 | 1 | 3 | 3 | 7 |
| **The possibility of heating** | 0,33 | 0,33 | 0,20 | 1,00 | 1 | 1 | 5 | 9 | 7 |
| **The possibility of lighting control** | 0,33 | 0,33 | 0,20 | 1,00 | 1,00 | 1 | 5 | 9 | 7 |
| **Reliability** | 0,20 | 0,14 | 0,20 | 0,33 | 0,20 | 0,20 | 1 | 9 | 9 |
| **Complexity of installation** | 0,14 | 0,33 | 0,11 | 0,33 | 0,11 | 0,11 | 0,11 | 1 | 5 |
| **Aesthetics** | 0,11 | 0,14 | 0,14 | 0,14 | 0,14 | 0,14 | 0,11 | 0,20 | 1 |

A simple way of determining the weights of the criteria entered from the matrix S consists in calculating the geometric mean of each row of the matrix.

$$g_i = \sqrt[k]{\prod_{j=1}^{k} s_{ij}}; i, j = 1,2,...,k \qquad (5)$$

Furthermore, the weights are normalized so that the following condition is fulfil, [5] :

$$\sum_{i=1}^{k} v_i = 1; v_i \geq 0 \qquad (6)$$

Standards can be related to, [5] :

$$v_i = \frac{g_i}{\sum_{i=1}^{k} g_i}; i, j = 1,2,...,k \quad (7)$$

# III. RESULTS

The above defined Saaty matrices are computed the geometric mean of all lines of standardization and the weights of criteria:

Table 3. Table geometric diameters and weights of criteria.

| Criterion | $g_i$ | $v_i$ |
|---|---|---|
| **Acquisition costs** | 4,1718 | 0,303 |
| **Operating costs** | 2,2225 | 0,161 |
| **Saving energy** | 3,0615 | 0,222 |
| **System maintenance** | 0,8132 | 0,059 |
| **The possibility of heating** | 1,2414 | 0,090 |
| **The possibility of lighting control** | 1,2414 | 0,090 |
| **Reliability** | 0,5682 | 0,041 |
| **Complexity of installation** | 0,2842 | 0,021 |
| **Aesthetics** | 0,1741 | 0,013 |
| **Sum of weights of all criteria** | - | 1 |

After defining the weights of criteria should be followed in the analysis of determining the values of standard criteria. Table 3 clearly shows how the distribution of weights for a given selection criteria.

# IV. DISCUSSION

However for this is necessary preferably the group of experts as well as more extensive type of scientific work, which would be engaged only in problems of multi-criteria analysis for evaluation of individual options of electrical installation.

# V. CONCLUSION AND FUTURE SCOPE

This proposal addresses the use of multi-criteria analysis for comparing the electrical variations based on defined criteria. This methodology is designed for the most part in general because of the possibility of further development in the larger work. This is an outline of options objectively and comprehensively evaluate variants of wiring and help in selecting the most appropriate wiring. Further development work could be focused on the issue of the use of sophisticated methods of choosing a technical solution based on the wiring not only prices but also on many other criteria such as comfort, service, durability, etc. The focus of work should be a discussion of wiring systems from a global perspective where the objective evaluation and selection of a suitable electro-installation is no longer possible to use common approaches, given the magnitude of such systems and their mutual ties. There is some use of the methods of multicriteria analysis (MCA), which would affect the extensiveness of solution and could use the results of this work.

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# EFFICIENT IMPLEMENTATIONS OF DISCRETE WAVELET TRANSFORMS USING FPGAS

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***ABSTRACT***

*Recently the Wavelet Transform has gained a lot of popularity in the field of signal and image processing. This is due to its capability of providing both time and frequency information simultaneously, hence giving a time-frequency representation of the signal. The traditional Fourier Transform can only provide spectral information about a signal. Moreover, the Fourier method only works for stationary signals. In many real world applications, the signals are non-stationary. One solution for processing non-stationary signals is the Wavelet Transform. Currently, there is tremendous focus on the application of Wavelet Transforms for real-time signal processing. This leads to the demand for efficient architectures for the implementation of Wavelet Transforms. Due to the demand for portable devices and real-time applications, the design has to be realized with very low power consumption and a high throughput. In this paper, different architectures for the Discrete Wavelet Transform filter banks are presented. The architectures are implemented using Field Programmable Gate Array devices. Design criteria such as area, throughput and power consumption are examined for each of the architectures so that an optimum architecture can be chosen based on the application requirements. In our case study, a Daubechies 4-tap orthogonal filter bank and a Daubechies 9/7-tap biorthogonal filter bank are implemented and their results are discussed. Finally, a scalable architecture for the computation of a three-level Discrete Wavelet Transform along with its implementation using the Daubechies length-4 filter banks is presented.*

***KEYWORDS:*** *Daubechies wavelet, discrete wavelet transform, Xilinx FPGA.*

## I. INTRODUCTION

In general, signals in their raw form are time-amplitude representations. These time-domain signals are often needed to be transformed into other domains like frequency domain, time-frequency domain, etc., for analysis and processing. Transformation of signals helps in identifying distinct information which might otherwise be hidden in the original signal. Depending on the application, the transformation technique is chosen, and each technique has its advantages and disadvantages.

The properties of Wavelet Transform allow it to be successfully applied to non-stationary signals for analysis and processing, e.g., speech and image processing, data compression, communications, etc. [5]. Due to its growing number of applications in various areas, it is necessary to explore the hardware implementation options of the Discrete Wavelet Transform (DWT).

An efficient design should take into account aspects such as area, power consumption, throughput, etc. Techniques such as pipelining, distributed arithmetic, etc., help in achieving these requirements. For most applications such as speech, image, audio and video, the most crucial problems are the memory storage and the global data transfer. Therefore, the design should be such that these factors are taken into consideration.

In this paper, Field Programmable Gate Arrays (FPGAs) are used for hardware implementation of the DWT [3, 4]. FPGAs have application specific integrated circuits (ASICs) characteristics with the advantage of being reconfigurable. They contain an array of logic cells and routing channels (called interconnects) that can be programmed to suite a specific application. At present, the FPGA based

ASIC market is rapidly expanding due to demand for DSP applications. FPGA implementation could be challenging as they do not have good arithmetic capabilities when compared with the general purpose DSP processors. However, the most important advantage of using an FPGA is because it is reprogrammable. Any modifications can be easily accomplished and additional features can be added at no cost which is not the case with traditional ASICs.

## II. DIFFERENT WAVELET FILTER BANK ARCHITECTURES

There are various architectures for implementing a two channel filter bank. A filter bank basically consists of a low pass filter, a high pass filter, decimators or expanders and delay elements. We will consider the following filter bank structures and their properties, specifically with reference to DWT [1, 2].

### 2.1. Direct Form Structure

The direct form analysis filter consists of a set of low pass and high pass filters followed by decimators. The synthesis filter consists of up samplers followed by the low pass and high pass filters as shown in figure 1.

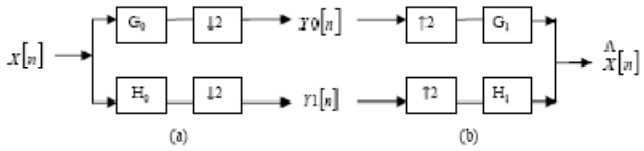


Figure 1: Direct form structure (a) Analysis filter bank (b) Synthesis filter

In the analysis filter bank, x[n] is the discrete input signal, $G_0$ is the low pass filter and $H_0$ is the high pass filter. ↓2 represents decimation by 2 and ↑2 represents up sampling by 2. In the analysis bank, the input signal is first filtered and then decimated by 2 to get the outputs $Y_0$ and $Y_1$. These operations can be represented by equations1 and 2.

$$Y_0[k] = \sum_n X[n].G_0[2k \quad n] \tag{1}$$

$$Y_1[k] = \sum_n X[n].H_0[2k - n] \tag{2}$$

The output of the analysis filter is usually processed (compressed, coded or analyzed) based on the application. This output can be recovered again using the synthesis filter bank. In the synthesis filter bank, $Y_0$ and $Y_1$ are first up sampled by 2 and then filtered to give the original input. For perfect output the filter banks must obey the conditions for perfect reconstruction.

### 2.2. Poly phase Structure

In the direct form analysis filter bank, it is seen that if the filter output consists of, say, N samples, due to decimation by 2 we are using only N/2 samples. Therefore, the computation of the remaining unused N/2 samples becomes redundant. It can be observed that the samples remaining after down sampling the low pass filter output are the even phase samples of the input vector $X_{even}$ convoluted with the even phase coefficients of the low pass filter $G_{0even}$ and the odd phase samples of the input vector $X_{odd}$ convoluted with the odd phase coefficients of the low pass filter $G_{0odd}$. The poly phase form takes advantage of this fact and the input signal is split into odd and even samples (which automatically decimates the input by 2), similarly, the filter coefficients are also split into even and odd components so that $X_{even}$ convolves with $G_{0even}$ of the filter and $X_{odd}$ convolves with $G_{0odd}$ of the filter. The two phases are added together in the end to produce the low pass output. Similar method is

applied to the high pass filter where the high pass filter is split into even and odd phases $H_{0even}$ and $H_{0odd}$. The poly phase analysis operation can be represented by the matrix equation 3.

$$\begin{bmatrix} G_{0_{even}} G_{0_{odd}} \\ H_{0_{even}} H_{0_{odd}} \end{bmatrix} \times \begin{bmatrix} X_{even} \\ z^{-1} X_{odd} \end{bmatrix} = H_p \begin{bmatrix} X_{even} \\ z^{-1} X_{odd} \end{bmatrix} = \begin{bmatrix} Y_0 \\ Y_1 \end{bmatrix} \qquad (3)$$

The filters with $G_{0even}$ and $G_{0odd}$ are half as long a $G_0$, since they are obtained by splitting $G_0$. Since, the even and odd terms are filtered separately, by the even and odd coefficients of the filters, the filters can operate in parallel improving the efficiency. The figure 2 illustrates poly phase analysis and synthesis filter banks.

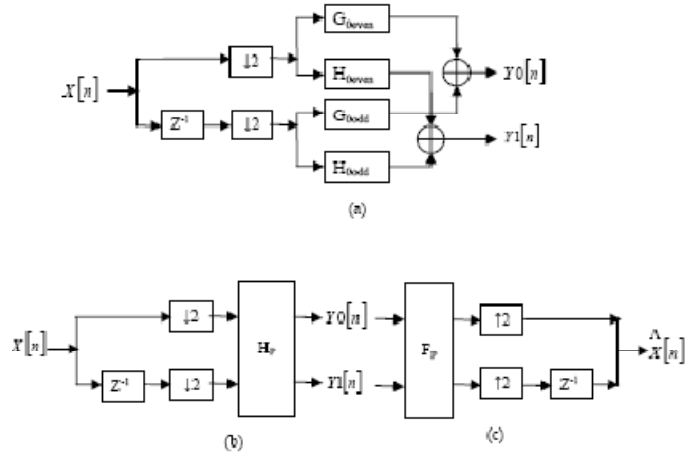


Figure 2: Polyphase structure of (a) Analysis filter bank (b) Equivalent representation of Analysis filter bank (c) Synthesis Filter bank

In the direct form synthesis filter bank, the input is first up sampled by adding zeros and then filtered. In the poly phase synthesis bank, the filters come first followed by up samplers which again, reduces the number of computations in the filtering operations by half. Since, the number of computations is reduced by half in both the analysis and synthesis filter banks; the overall efficiency is increased by 50%. Thus, the poly phase form allows efficient hardware realizations.

### 2.3. Lattice Structure

In the above structure, the poly phase matrix, $H_P(z)$ can be replaced by a lattice structure. The filter bank, $H_P(z)$ can be obtained if the filters $G_0(z)$ and $H_0(z)$ are known. Similarly, if $H_P(z)$ is known, the lattice structure can be derived by representing it as a product of simple matrices. The wavelet filter banks have highly efficient lattice structures which are easy to implement. The lattice structure reduces the number of coefficients and this reduces the number of multiplications. The structure consists of a design parameter *k* and a single overall multiplying factor. The factor *k* is collected from all the coefficients of the filter. For any *k*'s, a cascade of linear phase filters is linear phase and a cascade of orthogonal filters is orthogonal. The complete lattice structure for an orthogonal filter bank is shown in figure 3, where β is the overall multiplying factor of the cascade.

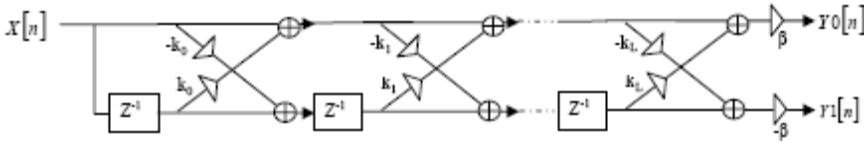


Figure 3. Lattice structure of an orthogonal filter bank

The lattice structure improves the filter bank efficiency as it reduces the number of computations performed. If the direct form requires 4L multiplications, the poly phase requires 2L multiplications, and the lattice requires just L+1 multiplications. The number of additions is also reduced in the lattice form.

### 2.4. Lifting Structure

The lifting scheme proposed independently by Herley and Swelden is a fast and efficient method to construct two-channel filter banks. It consists of two steps: lifting and dual lifting. The design starts with the Haar filter or the Lazy filter which is a perfect reconstruction filter bank with $G_0(z) = H_1(z)=1$ and $H_0(z) = G_1(z) = z^{-1}$. The lifting steps are:

Lifting: $H'(z) = H(z) + G(-z)\, S(z^2)$ for any $S(z^2)$.

Dual Lifting: $G'(z) = G(z) + H(-z)\, T(z^2)$ for any $T(z^2)$.

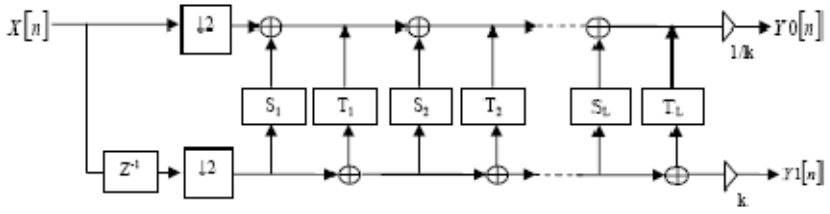


Figure 4. Lifting implementation

The lifting implementation is shown in figure 4. The lifting and dual lifting steps are alternated to produce long filters from short ones. Filters with good properties which satisfy the perfect reconstruction properties can be built using this method [18, 19].

## III. COMPARISON OF IMPLEMENTATION OPTIONS

For hardware implementation, the choice of filter bank structure determines the efficiency and accuracy of computation of the DWT. All structures have some advantages and drawbacks which have to be carefully considered and based on the application, the most suitable implementation can be selected. It is observed that the direct form is a very inefficient method for DWT implementation. This method is almost never used for DWT computation. The poly phase structure appears to be an efficient method for DWT computation. But the lattice and lifting implementations require fewer computations than the poly phase implementation and therefore are more efficient in terms of number of computations. However, the poly phase implementation can be made more efficient than the lattice and lifting schemes in case of long filters by incorporating techniques like Distributed Arithmetic. Also, the lattice structure cannot be used for all linear phase filters and imposes restrictions on the length of the filters. In the case of the lattice and lifting schemes, the filtering units cannot operate in parallel as each filtering unit depends on results from the previous filtering unit. In the case of convolution poly phase implementation, the units can operate in parallel, and therefore the filtering operations have less delay. However, pipelining can be used in the other schemes to reduce the delay. Often, for implementation purposes, the real number filter coefficients are quantized into binary digits. This introduces some quantization error. In the lifting scheme, the inaccuracy due to quantization is accumulated with each step. Thus, the lifting scheme constants must be quantized with better accuracy than the convolution filter constants i.e., the lifting constants need to be represented by more number of bits.

## IV. DISTRIBUTED ARITHMETIC TECHNIQUE

### 4.1 DA-based approach for the filter bank

Distributed Arithmetic (DA) has been one of the popular techniques to compute the inner product equation in many DSP FPGA applications [8, 11]. It is applicable in cases where the filter coefficients

are known a priori. The inner sum of products is rearranged so that the multiply and accumulate (MAC) operation is reduced to a series of look-up table (LUT) calls, and two's complement (2C) shifts and adds. Therefore, the multipliers which occupy large areas are replaced by small tables of pre-computed sums stored on FPGA LUTs which reduce the filter hardware resources.
Consider the following inner product calculation shown in 4(a) where c[n] represents an N-tap constant coefficient filter and x[n] represents a sequence of B-bit inputs:

$$y = \sum_{n=0}^{N-1} c[n].x[n] \qquad 4\ (a)$$

$$= \sum_{n=0}^{N-1} c[n].\sum_{b=0}^{B-1} x_b[k].2^b \qquad 4\ (b)$$

$$= \sum_{b=0}^{B-1} 2^b.\sum_{n=0}^{N-1} c[n].x_b[n] \qquad 4\ (c)$$

In equation 4(a), the inputs can be replaced as in 4(b) where $x_b[k]$ denotes the $b^{th}$ bit of $k^{th}$ sample of x[n]. Rearranging equation 4(b) gives 4(c). All the possible values of the inner function in (c) can be pre-computed and stored in an LUT. Now, the equation can be implemented using an LUT, a shifter and an adder. The architectures for the conventional MAC operation, represented by equation 4(a), and the DA-based shift-add operation, represented by equation 4(c) are shown in figure 5 for a 4-tap filter.

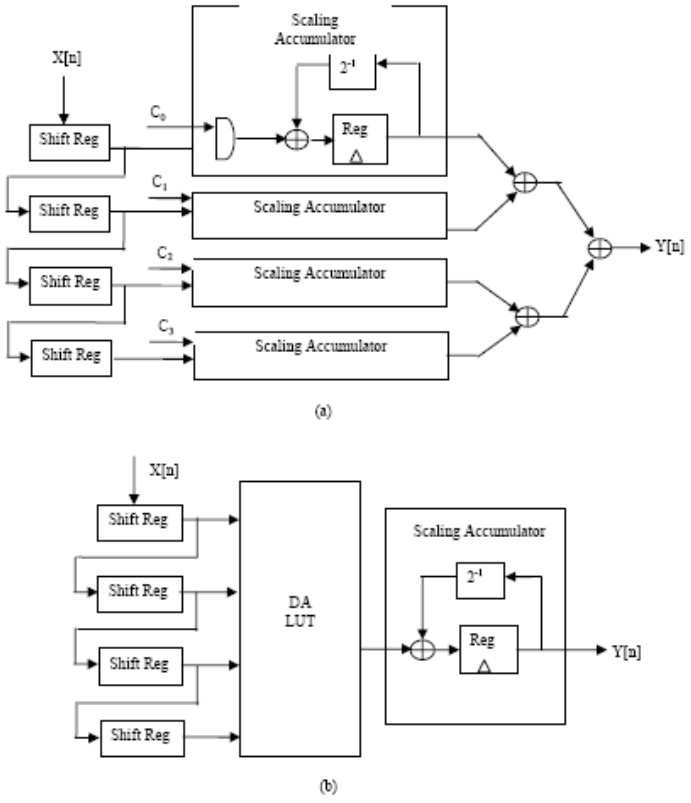


Figure 5. (a) Conventional MAC and (b) shift-add DA architectures.

In the DA architecture, the input samples are fed to the parallel-to-serial shift register cascade. For an N-tap filter and B-bit input samples, there are N shift registers of B-bits each. As the input samples are shifted serially through the B-bit shift registers, the bit outputs (one bit from each of N registers) of the shift register cascade are taken as address inputs by the look-up table (LUT). The LUT accepts the N bit input vector $x_b$, and outputs the value which is already stored in the LUT. For an N-tap filter

a $2^N$ word LUT is required. The LUT output is then shifted based on the weight of $x_b$ and then accumulated. This process is followed for each bit of the input sample before a new output sample is available. Thus for a B-bit input precision a new inner product *y* is computed every B clock cycles.
Consider a four-tap serial FIR filter with coefficients $C_0$, $C_1$, $C_2$, $C_3$. The DA-LUT table is as shown in table 1. The table consists of the sums of the products of the N bit input vector $x_b$ (N = 4 in this case) and the filter coefficients for all possible combinations.

Table 1. DALUT FOR 4 Tap Filter

| Address | Data |
|---|---|
| 0000 | 0 |
| 0001 | $C_0$ |
| 0010 | $C_1$ |
| 0011 | $C_0+C_1$ |
| : | : |
| : | : |
| : | : |
| 1110 | $C_1+C_2+C_3$ |
| 1111 | $C_0+C_1+C_2+C_3$ |

In conventional MAC-based filter, the throughput is based on the filter length. As the number of filter taps increase, the throughput decreases. In case of DA-based filter, the throughput depends on the input bit precision as seen above and is independent of the filter taps. Thus the filter throughput is de-coupled from the filter length. But when the filter length is increased, the throughput remains the same while the logic resources increase. In case of long filters, instead of creating a large table, it can be partitioned into smaller tables and their outputs can be combined. With this approach, the size of the circuit grows linearly with the number of filter taps rather than exponentially.
For a DWT filter bank, the equation 4(c) can be extended to equation 5(a) and 5(b) to define the low pass and high pass filtering operations.

$$y_l = \sum_{b=0}^{B-1} 2^b \cdot \sum_{n=0}^{N-1} G_0[n].x_b[n] \qquad 5\ (a)$$

$$y_h = \sum_{b=0}^{B-1} 2^b \cdot \sum_{n=0}^{N-1} H_0[n].x_b[n] \qquad 5\ (b)$$

The poly phase form of the above filters can be obtained by splitting the filters and the input, x[n] into even and odd phases to obtain four different filters. Since the length of each filter is now halved they require much smaller LUTs [13, 14].

## 4.2 Parallel Distributed Arithmetic for Increased Speed

DA-based computations are inherently bit-serial. Each bit of the input is processed before each output is computed [9]. For a B-bit input, it takes B clock cycles to compute one output. Thus, this serial distributed arithmetic (SDA) filter has a low throughput. The speed can be increased by partitioning the input words into smaller words and processing them in parallel. As the parallelism increases, the throughput increases proportionally, and so does the number of LUTs required. Filters can be designed such that several bits of the input are processed in a clock period. Partitioning the input word into M sub-words requires M-times as many memory LUTs and this increases the storage requirements. But, now a new output is computed every B/M clock cycles instead of every B cycles. A fully parallel DA (PDA) filter is achieved by factoring the input into single bit sub-words which achieves maximum speed. A new output is computed every clock cycle. This method provides exceptionally high-performance, but comes at the expense of increased FPGA resources. Figure 6 shows a parallel DA architecture for an N-tap filter with 4-bit inputs.

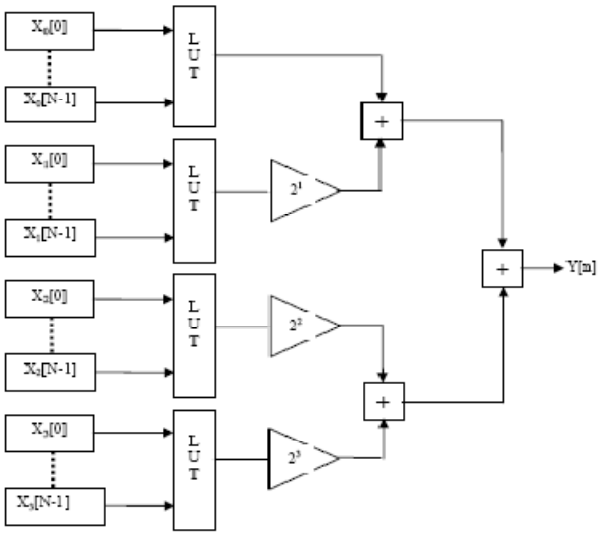


*Figure 6. Parallel DA Architecture*

In some applications, the same filter is applied to different inputs. In this case, instead of using two separate filters, a single filter can be shared among the different inputs. Sharing of filters decreases the filter sample rate but this method is very efficient in terms of the logic resources consumed. A multi-channel filter can be realized using virtually the same amount of logic resources as a single channel version of the same filter. The trade-off here is between the logic resources and filter sample rate.

### 4.3 A Modified DA-based approach for the filter bank

Unlike in the conventional DA method where the input is distributed over the coefficients, in this case the coefficient matrix is distributed over the input. It is seen that in the previous architecture, as the input bit precision increases there is an exponential growth in the LUT size and this increases the amount of logic resources required. The advantage of the present architecture over the previous one is that, in this method we do not require any memory or LUT tables. This reduces the logic resources consumed tremendously [10].

Consider the following inner product equation 6(a) where c[n] represents the M-bit coefficients of an N-tap constant coefficient filter and x[n] represents the inputs.

$$y = \sum_{n=0}^{N-1} c[n].x[n] \qquad 6\ (a)$$

$$= \sum_{m=0}^{M-1} c_m[k] 2^m \sum_{n=0}^{N-1} x[n] \qquad 6\ (b)$$

$$= \sum_{m=0}^{M-1} 2^m . \sum_{n=0}^{N-1} c_m[n].x[n] \qquad 6\ (c)$$

In equation 6(a) the coefficients can be replaced as in equation 6(b) where $c_m[k]$ denotes the $m^{th}$ bit of $k^{th}$ coefficient of c[n]. Rearranging equation 3.6(b) gives 6(c). The inner function, in 6(c) can be designed as a unique adder system based on the coefficient bits consisting of zeros and ones. The output, *y*, can then be computed by shifting and accumulating the results of the adder system accordingly based on the coefficient bit weight. Thus the whole equation can be implemented using just adders and shifters [20, 21].

# V. IMPLEMENTATION OF DWT FILTER BANKS WITH FIELD PROGRAMMABLE GATE ARRAYS

Field Programmable Gate Arrays (FPGAs) are used to synthesize and test the architectures in this paper [7, 12]. FPGAs are programmable logic devices made up of arrays of logic cells and routing channels. They have ASIC characteristics such as reduced size and power dissipation, high throughput, etc., with the added advantage that they are reprogrammable. Therefore, new features can be easily added and they can be used as a tool for comparing different architectures. Currently, Altera Corporation and Xilinx Corporation are the leading vendors of programmable devices. The architecture of the FPGAs is vendor specific. Among the mid-density programmable devices, Altera's FLEX 10K and Xilinx XC4000 series of FPGAs are the most popular ones[6]. They have attractive features which make them suitable for many DSP applications. FPGAs contain groups of programmable logic elements or basic cells. The programmable cells found in Altera's devices are called Logic Elements (LEs) while the programmable cells used in Xilinx's devices are called the Configurable Logic Blocks (CLBs). The typical design cycle for FPGAs using Computer Aided Design (CAD) tools is shown in figure 7.

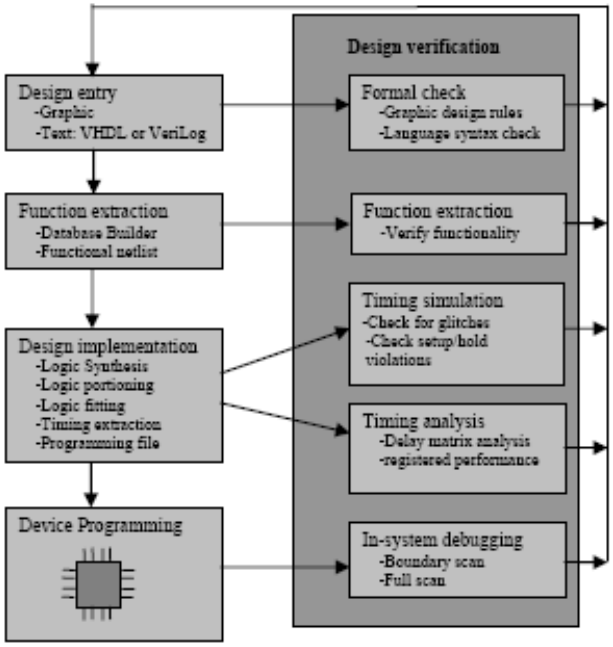


*Figure 7. CAD Design Cycle*

The design is first entered using graphic entry or text entry. In the next stage the functionality of the design is extracted. Then the design is targeted on a selected device and its timing is extracted. Finally the actual hardware device is programmed. At every stage the appropriate verification is done to check the working of the design. For design entry, text is preferred as it allows more control over the design compared to graphic design entry.

# VI. IMPLEMENTATION AND RESULTS

The Altera device EPF10K70RC240 with speed grade 2 is chosen for implementation purpose so that the whole design can fit into one device. It is a 5V device and some of its features are listed in Table 2.

Table 5.1 Features of EPF10K70 devices

| Feature | EPF10K70 |
|---|---|
| Typical gates (logic and RAM) | 70,000 |
| Logic Elements (LEs) | 3,744 |
| Logic Array blocks (LABs) | 468 |
| Embedded Array Blocks (EABs) | 9 |
| Total RAM bits | 18,432 |

The architecture is implemented for an input signal of 15 samples using the orthogonal Daubechies length-4 filter. The simulation waveforms generated by the Quartus simulator to verify the functionality of the design. Figure 8 shows the simulation results of the implemented architecture. Input samples of 8-bit precision are used. The coefficients at every level are scaled to have the same number of bits as the input. This allows the use of the same PEs for different levels of computation of the DWT. Thus, the architecture is modular and is easily scalable to obtain higher level of octaves.

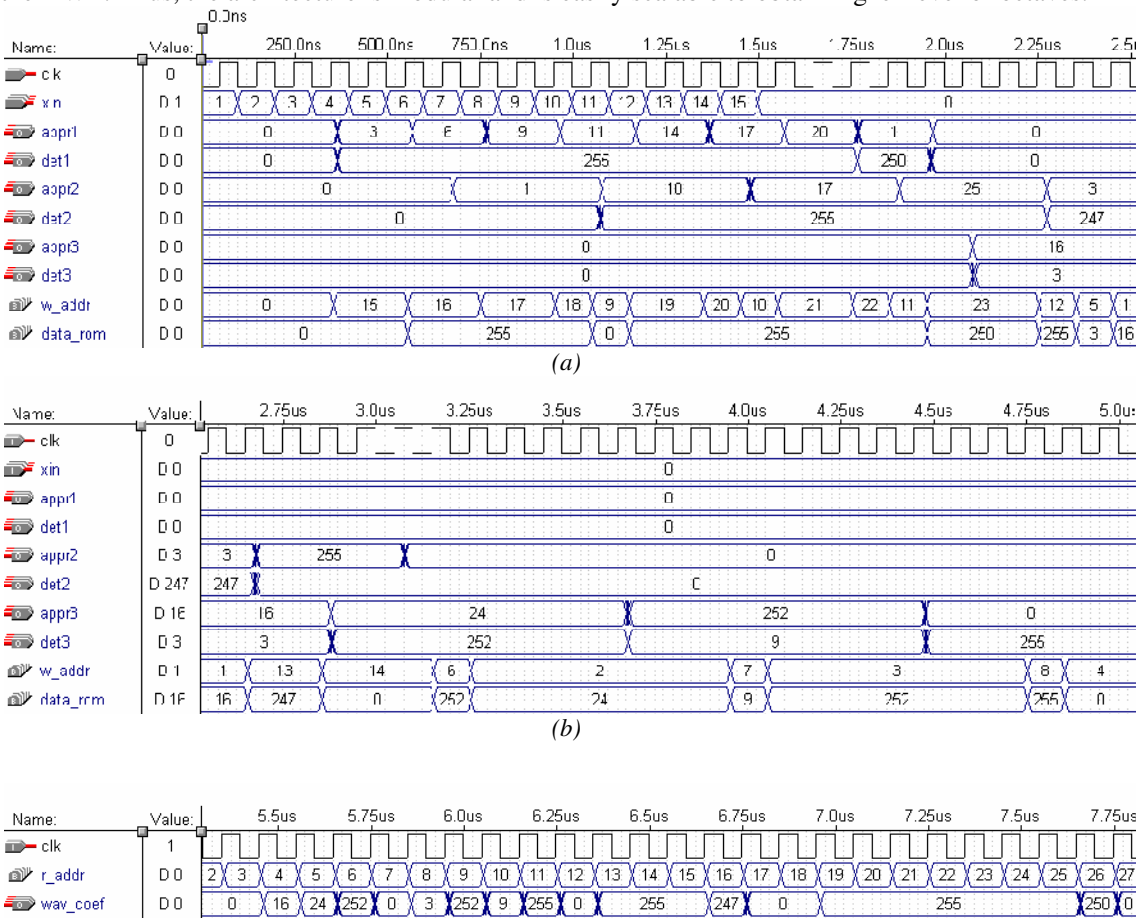


*Figure 8. Simulation results of the 3-level DWT architecture.*

The hardware resources required for the implementation can be derived from the report file generated by Quartus software. The number of logic cells (LCs) used was found to be 2794, which corresponds to 74% of the total LCs available in the device. The maximum operating frequency was found to be 20.83 MHz. The power consumption calculated was 3094.32mW. The supply voltage, $V_{cc}$, of the

EPF10K70 device is 5V, the standby current, $I_{CCSTANDBY}$ is 0.5 mA and its $I_{CC}$ coefficient, K is 85. The average ratio of logic cells toggling at each clock, $tog_{LC}$, is taken to be the typical value of 0.125.

# VII. CONCLUSION

The Discrete Wavelet Transform provides a multiresolution representation of signals. The transform can be implemented using filter banks. In this paper, different architectures for the Discrete Wavelet Transform have been discussed [16, 17]. Each of them can be compared on the basis of area, performance and power consumption. Based on the application and the constraints imposed, the appropriate architecture can be chosen. For the Daubechies length-4 orthogonal filter, three architectures were implemented, i.e., the poly phase architecture, the poly phase with fully parallel DA architecture, and the poly phase with modified DA architecture. It is seen that, in applications which require low area and power consumption, e.g., in mobile applications, the poly phase with modified DA architecture is most suitable and for applications which require high throughput, e.g., real-time applications, the poly phase with DA architecture is more suitable.

The biorthogonal wavelets, with different number of coefficients in the low pass and high pass filters, increases the number of operations and the complexity of the design, but they have better SNR than the orthogonal filters. For the Daubechies 9/7 biorthogonal filter, two different architectures were implemented, i.e., the poly phase architecture, and the poly phase with modified DA architecture. It is seen that the poly phase architecture has better throughput while the poly phase with modified DA architecture has lower area and lower power consumption.

A scalable architecture for computation of higher octave DWT has been presented. The architecture was implemented using the Daubechies length-4 filter for a signal length of 15. The simulation results verify the functionality of the design. The proper scheduling of the wavelet coefficients written to the RAM ensures that, when the coefficients are finally read back from the RAM, they are available in the required order for further processing. The proposed architecture is simple since further levels of decomposition can be achieved using identical processing elements. It is easily scalable to different signal lengths and filter orders for use in different applications. he architecture enables fast computation of DWT with parallel processing [ 22]. It has low memory requirements and consumes low power.

# VIII. FUTURE WORK

Synthesis filter banks to compute the inverse DWT, i.e., IDWT can be implemented using similar architectures for the corresponding analysis filter banks.

The architectures of the filter banks can be further improved using techniques such as Reduced Adder Graph, Canonic Signed Digit coding and Hartley's common sub expression sharing among the constant coefficients. Also, in the case of orthogonal filters with mirror coefficients, the transpose form of the filters yields a good architecture; this can be implemented and compared with the others.

The proposed higher octave DWT architecture can be extended to include symmetric signal extension. The use of symmetric extension in image compression applications reduces the distortion at boundaries of reconstructed image and provides improved SNR.

In memory intensive applications such as image and video processing, memory accesses could be the dominant source of power dissipation, as reading and writing to memory involves switching of highly capacitive address busses. Methods such as gray code addressing can be incorporated into the architecture to reduce this power dissipation.

As the DWT hierarchy increases, the required precision of the wavelet coefficients also increases. In the proposed architecture, the coefficients at all levels are scaled to have the same precision. While this reduces the hardware requirements, the accuracy of the coefficients is compromised as the number of levels increases. Therefore, the architecture can be modified to allow increased precision as the DWT level increases so as to achieve higher accuracy.

The proposed architecture can also be extended to 2-dimensional DWT computation. This can be achieved by computing the 1-dimensional DWT along the rows and columns separately. This operation requires large amount of memory and involves extensive control circuitry.

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# REAL TIME CONTROL OF ELECTRICAL MACHINE AND DRIVES: A REVIEW

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## *ABSTRACT*

*Over the last two decades, the available computer has become both increasingly powerful and affordable. This, in turn, has led to the emergence of highly sophisticated applications that not only enable high-fidelity simulation of dynamic systems but also automatic code generates for implementation in real time control of electric machine-drives. Today, electric drives, power electronic systems and their controls have become more and more complex, and their use is widely increasing in all sectors such as power systems, traction, hybrid vehicles, industrial and home electronics, automotive, naval and aerospace systems, etc. Advances in Microprocessors, Microcomputers, and Microcontrollers such as DSP, FPGA, dSPACE etc. and Power Semiconductor devices have made tremendous impact on performance electric motor drives. Due to advancement of the software tools like MATLAB/SIMULINK with its Real Time Workshop (RTW) and Real Time Windows Target (RTWT), real time simulators are used extensively in many engineering fields, such as industry, education and research institutions. As a result, inclusion of the real time simulation applications in modern engineering provides great help for the researcher and academicians. An overview of the Real Time Simulations of Electrical Machines Drives is herewith presented which is used in modern engineering practices. This paper discusses various real time simulation techniques such as Real Time Laboratory (RT Lab), Rapid Control Prototyping (RCP) and Hardware in the Loop (HIL) that can be used in modern engineering.*

***KEYWORDS***: *Rapid Control Prototyping (RCP), Hardware in the Loop (HIL), Real Time Workshop.*

## I. INTRODUCTION

Nowadays as a consequence of the important progress in the power semiconductor technologies, real time control of the electrical machines has gained more popularity in the arena of engineering. Due to the increasing complexity and cost of projects, and the growing pressure to reduce the time-to-market, testing and validation of complex systems has become more and more important in the design process. With the great advancement in processor and software technology and their cost decreases, it has become possible to use gradual and complete approach in system design, integration and testing. This approach, which was traditionally reserved for large and complex projects (power systems, aeronautics,) is the Real-Time (RT) simulation. Research on high level modeling, new converter-inverter topologies and control strategies are the major research areas in electrical drives. A system consisting of a loaded motor, driven by a power electronics converter is a complex and nonlinear system. Thus, performing system-level testing is one of the major steps in developing a complex product in a comprehensive and cost effective way requires real-time simulations. One of the most demanding aspects for real-time control systems is to connect the inputs and outputs of the tested control system to a real-time simulation of the target process.

In view of its implication that all control loops are closed via the simulator, this method is often called Hardware-in-the-Loop (HIL) simulation. By using the HIL simulations, we can evaluate different subsystems interaction. In HIL simulation, a device under test is run fully connected to a real-time simulated dynamic equivalent of an apparatus. A unique feature of this approach is that it even permits a gradual change-over from simulation to actual application, as it allows to initiation from a pure simulation to a gradually integrated real electrical and mechanical subsystems and finally into the loop as they become available. An HIL simulation can help reduce development cycles, cut overall costs, prevent costly failures, and test a subsystem exhaustively before integrating it into the system. One of the reasons for real time simulations with HIL is when a particular device is very difficult to model. Therefore it is convenient to use this device directly in the simulations instead of modeling it. Digital Real time simulations are required by hardware in the loop applications and their use allows rapid prototyping and minimizing the design process cost. The real time system structure will allow the implementation of advanced motor drives control algorithms and evaluation of their performance in real time [1,53]. Algorithms implemented in FPGA circuit are even more complicated to test because of number of internal signals. These signals are only accessible through test modules implemented inside the circuit. dSPACE real time platform allows simulation and verification environments to be created from Simulink models. In this way, the same model can be used through the whole development cycle of the control algorithm. dSPACE also allows simulations to be performed in several phases of the design, from a single module to system level. It is also possible to use Simulink in co-simulations with ModelSim to simulate VHDL model together with the Simulink model. This paper presents overview of the various real time simulation technologies and their engineering applications [7-30].

## II. BASIC CONCEPT OF THE REAL TIME CONTROL & SIMULATION

The literature about real-time systems presents digital control or computer controlled systems as one of its most important practical application in the field of electrical machines and drives. It is more natural that these applications should be treated as part of digital control. Despite this control system literature rarely includes extensively real-time control of electrical machines and it does not normally pay attention to real-time aspects beyond algorithms and choice of sampling times. The implementation of digital control systems and real-time systems of electrical machines golong together and they should be connected more or less later in the electrical machines due to advancement of the power semiconductor devices and various digital controllers. In general, real-time issues are gradually becoming “transparent” to the control of the various electrical machines. This transparency has been considerably increased in the last few years with the advent of software tools like MATLAB/Simulink with its RTW (Real Time Workshop) and RTWT (Real Time Windows Target). They make the implementation of real-time experiments easier and save time, but on the other hand they put more distance with regard to the real life problems, which can emerge during the real-time implementation of control system of electrical machines. It is possible to find in the available literature several definitions for real-time systems. Here, a definition that does not contradict the one given in the IEEE POSIX Standard (Portable Operation System Interface for Computer Environments) will be assumed.

“A real-time system is one in which the correctness of a result not only depends on the logical correctness of the calculation but also upon the time at which the result is made available”

It is again appropriate to quote one of the great scientists in automatic control, Karl Astrom

“Many important aspects on implementation are not covered in textbooks. A good implementation requires knowledge of control systems as well as certain aspects of computer science. It is necessary that we have engineers from both fields with enough skills to bridge the gap between the disciplines. Typical issues that have to be understood are windup, real-time kernels, computational and communication delays, numeric’s and man machine interfaces. Implementation of control systems is far too important to be delegated to a code generator. Lack of understanding of implementation issues

is in my opinion one of the factors that has contributed most to the notorious GAP between theory and practice."

This definition emphasizes the notion that time is one of the most important entities of the system and that there are timing constraints associated with systems tasks. Such tasks normally control or react to events that take place in the outside world, which are happening in "real time". Thus, a real-time task must be able to keep up with external events, with which it is concerned. It should be noted here that real-time computing is not equivalent to fast computing. Fast computing aims at getting the results as quickly as possible, while real-time computing aims at getting the results at a prescribed point of time within defined time tolerances.

Nowadays, it is very difficult to choose a software/hardware configuration for real-time experiments because there are many manufacturers who offer a variety of well designed systems. Thus, it would prudent to be caution at the moment to define the specifications for such systems. Today it is very common to use two computers in a host/ target configuration to implement real-time control systems. The host is a computer without real-time requirements, in which it develops environment, data visualization and control panel in the form of a Graphic User Interface (GUI) reside. The real-time system runs on the target, which can be a second computer or an embedded systems based on a board with a DSP (Digital Signal Processor), a Power PC or a Pentium family processor. The main features of the real –time software, as distinct from other software are, that the control algorithms must be run at their scheduled sample intervals and their existing associate software components, which interact with sensors and actuators. Generally, two methods of the real time control algorithms implementations are used. They are Manual writing of the code and Automatic generation of the controller, using a code translator that produces a real time code directly from the controller model [4]. The main idea using real time control is to smoothen transition from the non real analysis and simulation to the real time experiments and implementation. The various digital real time controller and simulation solutions can be divided into the categories as given in Table.1 [4].

A typical real time control and simulation is shown in Fig.1[4].The Real time simulation requires selection of control strategies, structures and parameter values. The integrated real-time control and simulation environment is a solution enabling the designer to perform the simulations and real time

Table No 1 Various Real Time Controllers

| Solution | Reliability | Flexibility | Advanced Algorithms | Cost | Rapid Prototyping Ability |
|---|---|---|---|---|---|
| PLC | High | Medium | Low | High | Medium |
| Microcontrollers | Medium | Low | Low | Low | Low |
| VME Industrial Comp. | High | Medium | Medium | High | Medium |
| DSP | Medium | Medium | Medium | Medium | High |
| PC+ data acq. board | Low | High | High | Low | High |

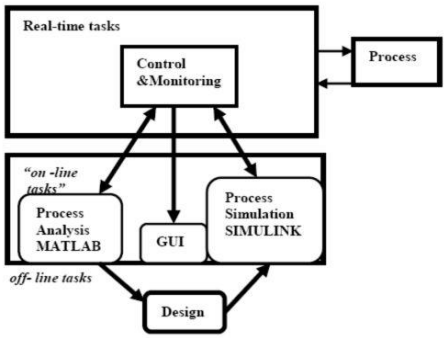


Fig.1 Typical Real Time Control System.

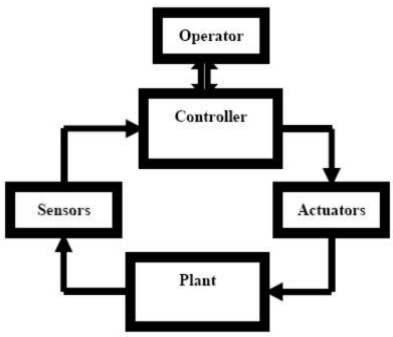


Fig. 2 Block diagram Real Time control for Electrical Machines.

experiments in a structured and simple manner. The system shown in Fig.1 [4] consists of three parts: a Real Time Kernel (RTK), an "on-line" operating analysis, simulation and visualizations tools, and an **"**off-line" design support libraries. The real-time kernel (RTK) performs the controller algorithms and data logging. Data collected in the buffer of the RTK can be analyzed in "on line" mode using the appropriate software. If necessary, the control algorithms can be redesigned in off line mode using non real facilities and then verified by simulation method and finally downloaded to real time controller. "On-line" simulation provides the best conditions for the parameters tuning [4-5]. The basic real time control system for electrical machines –drives is shown in Fig.2 [3]. A power electronic system, similar a kin to any control system, is usually made of a controller and a plant as shown in Fig. 2[3]; A power circuit consists of power source, power electronics converter and loads. These are usually connected in closed loop by means of sensors sending feedback signals from the plant to the controller and an interface (actuators) to level the signals sent from the controller to the power switches (Firing pulse unit, gate drives, etc)[3].

# III. REAL TIME CONTROL TECHNIQUES

Now days, as a consequence of the important progress made in electrical machines and drives because of advancement in power semiconductor devices. With advancement in the digital controllers such as Microprocessor/Microcontroller, Digital Signal Processors (DSP), Field Programmable Gate Array (FPGA ), dSPACE and other Artificial Intelligence (AI) techniques such as Fuzzy Logic, Neural Network can now satisfactorily be implemented for real time applications.[5,8]. Traditionally, validation of systems was done by non-real-time simulation of the concept at early stages in the design, and by testing the system once the design was implemented however this method has two major drawbacks: first, the leap in the design process, from off-line simulation to real prototype, is so wide that it is prone to many troubles and problems related to the integration at once of different modules; second, the off-line, non-real-time, simulation may become tediously long for any moderately complex systems, especially for Electrical Machines drives with switching power electronics [3].Various techniques that can be used for real time control and simulation of electrical machines and drives are as under:-

## 3.1 Microprocessor/Microcontrollers:

Conventional controllers have been replaced by the new dynamic microprocessor based control techniques. The advancement of microprocessor technology has followed a rapid pace since the advent of the first 4-bit microprocessor in 1971. From simple 4-bit architecture with limited capabilities, microprocessors have evolved towards complex 64-bit architecture in 1992 with tremendous processing power. The evolution of microcontrollers has followed that of microprocessor, and consists of three main families: MCS-52, MCS-96 and i960. These families are based on 8-bit CISC, 16-bit CISC and 32-bit and 64-bit RISC microprocessor architecture respectively. The digital technology is developed in an order as outlined here: General-purpose microprocessors, microcontrollers, advanced processors (DSP's, RISC processors, parallel processors), ASIC's and SoC. The recent developments of control techniques for several kinds of electrical machines require better and modern machine drivers, since digital control techniques usually require microprocessor computation for their implementation. A microprocessor based electrical machines control using PWM modulation was implemented by using PMACP16-200 microprocessor for induction motor and results were supported by the experimental setup [6]. As seen in rapid changes in the technology of microprocessor, a newly developed Motorola MC68HC11E-9 microcontroller based fully digital control system has been developed to control the induction motor. The high-performance microprocessor and PC based real time control schemes for electrical machines have been presented in [6-8] and the controller performance was checked and verified experimentally [6-10].

## 3.2 Digital Signal Processors (DSP)/ Field Programmable Gate Array (FPGA)

Digital signal processors began to appear roughly around 1979 and today, advanced Digital Signal Processors, RISC (Reduced Instruction Set Computing) processors, and parallel processors provide ever more high computing capabilities for the most demanding applications. With the great advances in the microelectronics and Very Large Scale

Integration (VLSI) and Very High Speed Integrated Circuit Description Language (VHDL) technology, high-performance DSP's can be effectively used to realize real time simulation of electrical machines. The basic functions of real time control for electric drive are shown in Fig.3 [8].The real time simulation of electric machine–drives has been developed and successfully integrated in the first course of power electronics and electric drives [8-14].

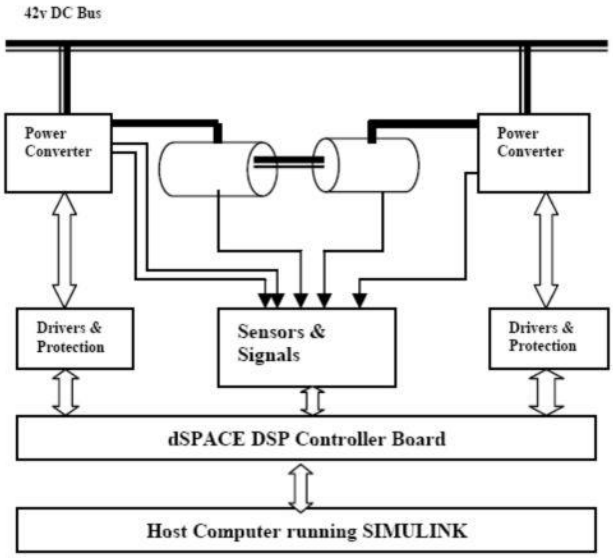


Fig. 3 Real Time Simulation Electric Drives Laboratory.

New emerging technologies in semiconductor industry offered the means to create high-performance digital components allowing implementation of more complex control applications. Embedded Systems (ES) are computers incorporated in devices in order to perform application-specific functions. Application Specific Integrated Circuit (ASIC) is a generic term which is used to designate any integrated circuit designed and built specifically for a particular application. ES can contain a variety of computing devices, such as microcontrollers, Application Specific Integrated Circuits (ASICs), Application Specific Integrated Processors (ASIPs), and Digital Signal Processors (DSPs). Recently, the System-on-Chip (SoC)(Eshraghian,2006;Nurmi, 2007) capabilities have provided the opportunity to have more performance digital control solution[19].There is now renewed interest in devoting to Field Programmable Gate Arrays (FPGAs) for full integration of all control functions. New FPGA technology (Rodriguez-Andina *et al*., 2007) containing both reconfigurable logic blocks and embedded cores, becomes quite mature for high-speed power control applications. Hard Ware (HW) and Soft Ware (SW) components interact in order to perform a given task. Such systems need a co-design expertise to build a flexible embedded controller that can execute real time closed-loop control. The power of these FPGAs has been made readily available to embedded system designers and SW programmers through the use of SW and HW tools. Field-programmable gate arrays (FPGA's) are a special class of ASIC's which differ from mask programmed gate arrays in that their programming is done by end-users at their site with no IC masking steps. The main advantage of FPGAs is the reconfiguarablity of the hardware as compared to DSP processors where in the latter hardware resources are fixed and cannot be reconfigured. During the last ten years embedded systems have moved towards a System-on-a-Chip (SoC) and high-level multi chip module solutions. A SoC design is defined as a complex IC that integrates the major functional elements of a complete end-product into a single chip or chipset [17-20]. Today System-on-a Chip (SoC) devices target high performance applications in which transition from fast time to market is of prime

importance. The evolution of VLSI and microprocessor technologies is expected to continue with an accelerating pace during the next decade. The FPGA based real time simulation of electrical machines has been implemented [19-27].

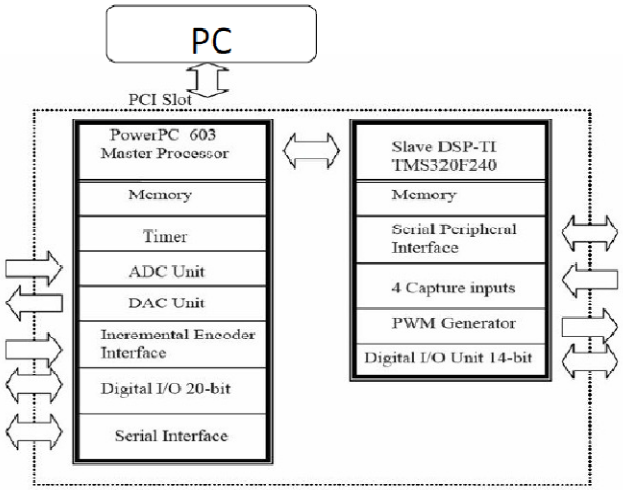


Fig.4 Block Diagram of a dSPACE DS1104 R&D Controller Board.

### 3.3 dSPACE Controller

Testing and verification of motor control algorithms is very demanding and time consuming. Test systems use usually electrical connections to signal lines or pins to get information from a tested device. Algorithms implemented in FPGA circuit are even more complicated to test because of the amount of internal signals. These signals are accessible only through test modules implemented inside the circuit [32]. dSPACE hardware platform is based on Digital Signal Processors (DSP). This platform has two characteristics which discern it from other similar products. In the first characteristic microprocessor board is mounted in the PCI slot of a personal computer, where as in the other system uses MATLAB/Simulink as a software development tool. Hardware platform consists of two DSPs, which share different application-communication tasks in order to achieve real-time application running.

dSPACE uses all Simulink features for creating a user algorithm[28].dSPACE software package includes additional Simulink toolboxes which define different hardware characteristics like timers, counters, PWM generators, encoders, etc[31].When a user algorithm is created in Simulink, the target DSP code must be generated. MATLAB's Real time workshop and the specific builder, installed with dSPACE software package, provides building and downloading of user algorithms which are possible directly from Simulink. When the user algorithm is downloaded, real time debugging, parameters adjustment and signals observing, are realized with the Control Desk software package. dSPACE real time platform allows simulation and verification environments to be created from Simulink models [33]. This way, the same model can be used throughout the whole development cycle of the control algorithm. dSPACE also allows simulations to be performed in several phases of the design, from a single module to a system level. It is also possible to use Simulink in co simulations with ModelSim' to simulate VHDL model together with the Simulink model [30-32]. dSPACE real time platform including powerful power PC processor with general purpose I/O device as shown in Fig. 4 [32]. It also includes separate DSP processor that can be used for PWM-outputs and inputs. dSPACE is capable of executing DTC modulator with rest of the motor control algorithms as well as emulate electric drive system in real time [32].The real time simulation of the electrical drives has been presented.[31-32].

### 3.4 Artificial Intelligence Control

Amongst recent trends, there is an increased interest in combining artificial intelligence controls with real time control techniques. In this paper, a review on the different techniques used, based on the

fuzzy logic and neural network in vector control of induction motor drive, are presented[27,30,36].The efficiency of the controller has been verified through hardware and MATLAB implementation [29].The real time implementation of IRFOC using dSPACE controller is presented. The performance of complete vector control of the single phase induction motors and PI controllers have been investigated and verified experimentally [31].

# IV. COMPARISION OF VARIOUS REAL TIME SIMULATION TECHNIQUES

In the past motor controller were typically developed and used by using a real motor drive in early design process. However today, it is more common to test controller using simulated motor model in a real time environment. Testing and verification of motor control algorithms is very demanding and time consuming. The various controller and their performance for real time control of electrical machine are listed in Table.-I.DSP is optimised for digital signal processing however it is not optimised for the specific algorithms implemented in software are results in poor performance. FPGA provides the means for achieving hardware performance and software versatility. The main advantages of FPGA are the reconfiguarablity of the hardware as compared to DSP processors in which the hardware resources are fixed and cannot reconfigured. The bit length of digital word is not limited in FPGA where in DSP and other processors it is limited. Algorithms implemented in FPGA circuit are even more complicated to test because of number of internal signals. These signal are only accessible through test modules implemented inside the circuit. Space hardware platform is based on DSP and Microprocessors. dSPACE real time platform allows simulation and verification environments to be created from Simulink model. Artificial Intelligence techniques such as neural network, fuzzy logic leads to improved performance when properly tuned. They are easy to extend and modify and also can be easily made adaptive by the incorporation of new data or information, as they become available.

# V. APPLICATIONS OF THE REAL TIME SIMULATION IN ELECTRICAL MACHINE DRIVES

Real time application can be used in modern engineering and technologies as:

## 5.1 Rapid Control Prototyping (RCP):

A critical aspect in the deployment of motor drives lies in the early detection of defects in the design process. Rapid prototyping of motor controllers is one methodology that enables the control engineer to quickly deploy control algorithms and detect eventual problems. This is typically performed using a small real-time simulator called a Rapid Control Prototyping system (RCP) connected in closed-loop with a physical prototype of the drive to be controlled. Modern RCPs take advantage of a graphical programming language (such as Simulink) with automatic code generation support. Later in the design process, when this code has been converted and fitted into a production controller (using mass-production low-cost devices), the same engineer can verify it against the same physical motor drive, often a prototype or a preproduction unit[22]. In RCP applications, an engineer will use a real-time simulator to quickly implement a controller and connect it to the real plant. This methodology implies that the real motor drive is available at the RCP stage of the design process. Furthermore, this set-up requires a 2nd drive (such as a DC motor drive) to be connected to the motor drive under test to emulate the mechanical load. This is a complex setup; however it has been proven to be very effective in detecting problems earlier in the design process. In cases where a physical drive is not available, or where only costly prototypes are available, an HIL-simulated motor drive can be used during the RCP development stage. In such cases, the dynamometer, real IGBT converter, and motor are replaced by a real-time virtual motor drive model. This approach has a number of advantages. For example, the simulated motor drive can be tested with borderline conditions that would otherwise damage a real motor. In addition, setup of the controlled-speed test bench is simplified since the virtual shaft speed is set by a single model signal, as opposed to using real bench, where a 2nd drive would be needed to

control the shaft speed. Other advantages of using a virtual motor drive system include the ability to easily study the impact of motor drive parameter variations on the controller itself [3].A typical rapid control prototyping is shown in Fig.5[3].

Rapid Control Prototyping (RCP) consists of quickly generating a functioning prototype of the controller, and to test and iterate this control algorithm on a real-time platform with real input/output devices. Rapid control prototyping differs from HIL in that the control strategy is simulated in real-time and the "plant," or system under control, is real The applications of RT-LAB real-time system for rapid control prototyping are numerous;(a) It is found in the development of a biped locomotor applicable to medical and welfare fields [10];(b) In autonomous control to manoeuvring a ship along a desired paths at different velocities [3], where RT-Lab is used for rapid prototyping of the ship real-time feedback controller;(c) In real-time control of a multilevel converter using the mathematical theory of resultants]; and in several research and teaching labs for the control of electric motors. A typical setup using the Drive Lab experimental set has been implemented [44-68].

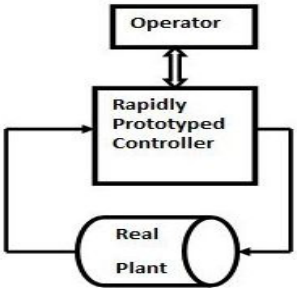


Fig .5 Rapid Control Prototyping.

### 5.2 Hardware –in –the –Loop testing (HIL)

Hardware-in-the-loop (HIL) Simulation of either the controller (Rapid Control Prototyping) or the plant (plant-in-the-loop, or generally called hardware-in the-loop) is shown in Fig.6[3]. At this stage, a part of the designed system is built and available to be integrated to the other part that is being simulated in real-time. If the hardware (controlled equipment) is available, rapid control prototyping and testing is done with the real hardware.

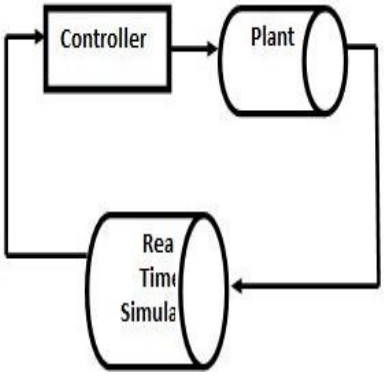


Fig.6 Hardware in the Loop Simulation.

But, for complex systems, like a hybrid car power drive, or a complex industrial drive, in most cases, the controller will be ready before the hardware it controls; so, HIL testing, where the real hardware is replaced by its RT digital model, is used to debug and refine the controller. This is done with a key characteristic of this design process: i.e. code generation. The block diagram based model is automatically implemented in real-time through fast and automatic code generation. The long, error prone hand coding is avoided; prototyping and iterative testing is therefore greatly accelerated [3]. HILS differs from pure real-time simulation by the use of the "real" controller in the loop (motor

drive controller, electronic control unit for automotive, FADEC for aerospace, etc). This controller is connected to the rest of the system that is simulated by input/outputs devices. So unlike RCP, in HILS, it is the plant that is simulated and the controller is real. Hence, aircraft flight simulators can be considered as a form of HIL simulation.HIL permits repetition and variation of tests on the actual or prototyped hardware without any risk for people or system. Tests can be performed under realistic and reproducible conditions. They can also be programmed and automatically executed [48].The HIL simulation is discussed in detail [46-61].

### 5.3 Software in the loop (SIL)

SIL represents the third logical step beyond the combination of RCP and HIL as shown in Fig.7. With a powerful enough simulator, both controller and plant can be simulated in real time in the same simulator. SIL has the advantage over RCP and HIL that no inputs and outputs are used, thereby preserving signal integrity. In addition, since both the controller and plant models run on the same simulator, timing with the outside world is no longer critical; it can be slower or faster than real-time with no impact on the validity of results, making SIL ideal for a class of simulation called accelerated simulation. In accelerated mode, a simulation runs faster than real-time, allowing for a large number of tests to be performed in a short period. For this reason, SIL is well suited for statistical testing such as Monte-Carlo simulations. SIL can also run slower than real-time. In this case, if the real-time simulator lacks computing power to reach real-time, a simulation can still be run at a fraction of real-time, usually faster than on a desktop computer.

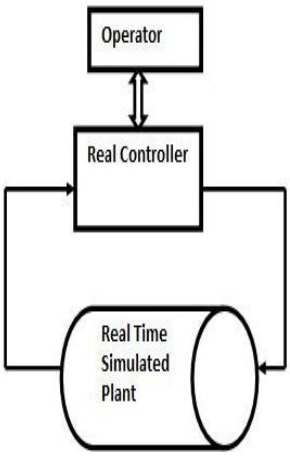


Fig.7 SIL Simulation

### 5.4 Rapid Batch Simulation (RBS)

RBS is typically used to accelerate simulation in massive batch run tests, such as aircraft parameter identification using aircraft flight data [44-70]

### 5.5 RT Lab Real Time Platform

RT-LAB is an integrated real-time software platform that enables model-based design by the use of rapid prototyping and HIL simulation and testing of control systems, according to the V-cycle design process. RT-LAB is a powerful, modular, distributed, real-time platform that lets the engineer and researcher to quickly implement block diagram. Simulink models on PC platform thus supporting the model-based design method by the use of rapid prototyping and hardware-in-the-loop simulation of complex dynamic systems [3]. The major elements integrated in this real-time platform are: distributed processing architecture, powerful processors, high precision and very fast input/output interface, hard real-time scheduler and modelling libraries and solvers specifically designed for the highly non-linear motor drives, power electronics and power systems. The RT Lab applications are verified experimentally [44-70].

# VI. CONCLUSION

This paper presents a literature survey on the artificial intelligence based on real time control of electrical machine-drives. An overview of various real time simulation techniques of electrical machines –drives and its applications in modern engineering technologies has been presented. The real time simulation allows for physical controller to be simulated so that its performance can be evaluated. Once the controller is designed in MATLAB/SIMULINK, it can be physically implemented using the rapid control prototyping of the dSPACE platform. FPGA based digital platform is more suitable for real time control of electrical machines. The FPGA based real time control of electrical machine is to able to support both software and hardware customisation. It allows inserting additional interfaces and controllers as software tasks to enable system use with control application. The fully System on Chip(SOC) integrated real time control system provides for lower cost and high speed execution. The use of FPGA's in real time control applications not only increases the performance of the system but also reduces the cost and size of the controller. dSPACE platform and MATLAB/SIMULINK environment gives powerful tools for teaching and research for electrical machine-drives. Artificial intelligence techniques do not require any mathematical modelling, that is why these techniques are more popular in real time control. All these techniques work well under normal operating conditions. The various approaches available for real time control such as RT real time platform, Rapid Control Prototyping (RCP) and Hardware in the Loop Simulation (HIL) of the electrical machine drives have been discussed elaborately. At present most of the electric drive have been controlled using dSPACE. Therefore, a review report on microcontrollers, DSPs, FPGAs and dSPACE are also discussed in detail. The real time simulation allows for physical controller to be simulated system so that it performance can be evaluated. Once the controller is designed in MATLAB/SIMULINK, it can be physically implemented using the rapid control prototyping of the dSPACE platform. The various approaches available for real time control such as RT real time platform, Rapid Control Prototyping (RCP) and Hardware in the Loop Simulation (HIL) of the electrical machine drives have been discussed systematically. HIL simulation is a valuable technique that has been used for decades in the development and testing of complex systems such as missiles, aircraft, and spacecraft. By taking advantage of low-cost, high-powered computers and I/O devices, the advantages of HIL simulation can be realized by a much broader range of system developers. As modern engineering becoming more complex and costlier, simulation technologies are becoming increasingly crucial to their success. An attempt is made to provide quick references for the researcher, practising engineers and academicians those are working in the area of the real time control.

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# IMPLEMENTATION OF PATTERN RECOGNITION TECHNIQUES AND OVERVIEW OF ITS APPLICATIONS IN VARIOUS AREAS OF ARTIFICIAL INTELLIGENCE

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***ABSTRACT*:**

*A pattern is an entity, vaguely defined, that could be given a name, e.g. fingerprint image, handwritten word, human face, speech signal, DNA sequence. Pattern recognition is the study of how machines can observe the environment, learn to distinguish patterns of interest from their background, and make sound and reasonable decisions about the categories of the patterns. The goal of pattern recognition research is to clarify complicated mechanisms of decision making processes and automatic these function using computers. Pattern recognition systems can be designed using the following main approaches: template matching, statistical methods, syntactic methods and neural networks. This paper reviews Pattern Recognition, Process, Design Cycle, Application, Models etc. This paper focuses on Statistical method of pattern Recognition.*

***KEYWORDS:*** *Pattern, Artificial Intelligence, statistical pattern recognition, Biometric Recognition, Clustering of micro array data.*

## I. INTRODUCTION

Humans have developed highly sophisticated skills for sensing their environment and taking actions according to what they observe, e.g., recognizing a face, understanding spoken words, reading handwriting, distinguishing fresh food from its smell. [1]This capability is called Human Perception: We would like to give similar capabilities to machines. Pattern recognition as a field of study developed significantly in the 1960s. It was very much an interdisciplinary subject, covering developments in the areas of statistics, engineering, artificial intelligence, computer science, psychology and physiology, among others. Human being has natural intelligence and so can recognize patterns. [3]A pattern is an entity, vaguely defined, that could be given a name, e.g. fingerprint image, handwritten word, human face, speech signal, DNA sequence. [1]Most of the children can recognize digits and letters by the time they are five years old, whereas young people can easily recognize small characters, large characters, handwritten, machine printed. The characters may be written on a cluttered background, on crumpled paper or may even be partially occluded. Pattern recognition is the study of how machines can observe the environment, learn to distinguish patterns of interest from their background, and make sound and reasonable decisions about the categories of the patterns. [5]But in spite of almost 50 years of research, design of a general purpose machine pattern recognizer remains an elusive goal. The best pattern recognizers in most instances are humans, yet we do not understand how humans recognize patterns. The more relevant patterns at your disposal, the better your decisions will be. This is hopeful news to proponents of artificial intelligence, since computers can surely be taught to recognize patterns. Indeed, successful computer programs that help banks score credit applicants, help doctors diagnose disease and help pilots land airplanes.[4] Some examples of Pattern Recognition Applications to state here are as follows:

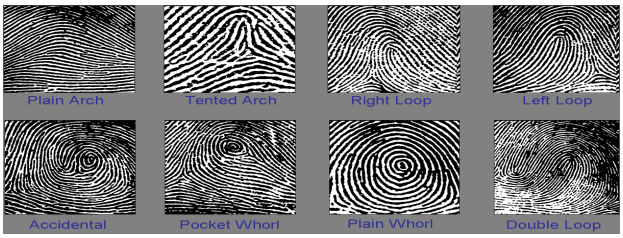


Figure1: Fingerprint recognition.

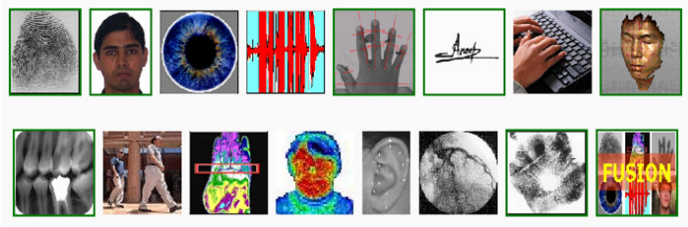


Figure2 : Biometric recognition.

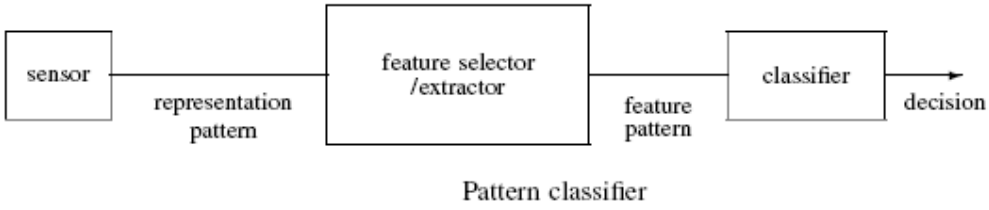


Figure3 : Pattern Classifier

## II. PATTERN

A pattern is an entity, vaguely defined, that could be given a name, e.g. fingerprint image, handwritten word, human face, speech signal, DNA sequence. Patterns can be represented as (i) Vectors of real-numbers,(ii)Lists of attributes(iii)Descriptions of parts and their relationships. Similar patterns should have similar representations. Patterns from different classes should have dissimilar representations. Choose features that are robust to noise and favor features that lead to simpler decision regions[23].

## III. PATTERN RECOGNITION

Pattern recognition techniques are used to automatically classify physical objects (2D or 3D) or abstract multidimensional patterns (*n* points in *d* dimensions) into known or possibly unknown categories. A number of commercial pattern recognition systems exist for character recognition, handwriting recognition, document classification, fingerprint classification, speech and speaker recognition, white blood cell (leukocyte) classification, military target recognition among others. Most machine vision systems employ pattern recognition techniques to identify objects for sorting, inspection, and assembly. The design of a pattern recognition system requires the following modules: sensing, feature extraction and selection, decision making, and system performance evaluation. The availability of low cost and high resolution sensors (e.g., CCD cameras, microphones and scanners) and data sharing over the Internet have resulted in huge repositories of digitized documents (text, speech, image and video). Need for efficient archiving and retrieval of this data has fostered the development of pattern recognition algorithms in new application domains (e.g., text, image and video retrieval, bioinformatics, and face recognition). [38]

# IV. GOAL OF PATTERN RECOGNITION

1) Hypothesize the *models* that describe the two populations.
2) Process the sensed data to eliminate noise.
3) Given a sensed pattern, choose the model that best represents it.

# V. VARIOUS AREAS OF PATTERN RECOGNITION

1) **Template matching:-** The pattern to be recognized is matched against a stored template while taking
Into account all allowable pose (translation and rotation) and scale changes.
2) **Statistical pattern recognition:**- Focuses on the statistical properties of the patterns (i.e., probability
Densities)
3) **Artificial Neural Networks:**- Inspired by biological neural network models.
4) **Syntactic pattern recognition: -** Decisions consist of logical rules or grammars[13]

Generally, Pattern Recognition Systems follow the phases stated below.

1) Data acquisition and sensing: Measurements of physical variables, Important issues: bandwidth, resolution, sensitivity, distortion, SNR, latency, etc.
2) Pre-processing: Removal of noise in data, Isolation of patterns of interest from the background.
3) Feature extraction: Finding a new representation in terms of features.
4) Model learning and estimation: Learning a mapping between features and pattern groups and categories.
5) Classification: Using features and learned models to assign a pattern to a category.
6) Post-processing: Evaluation of confidence in decisions, Exploitation of context to improve performance, Combination of experts.

### 5.1 Important issues in the design of a PR system

- Definition of pattern classes.
- Sensing environment.
- Pattern representation.
- Feature extraction and selection.
- Cluster analysis.
- Selection of training and test examples.
- Performance evaluation.

# VI. DESIGN OF A PATTERN RECOGNITION SYSTEM:

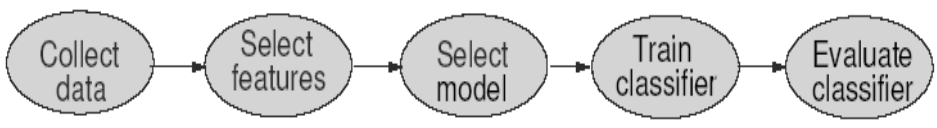


Figure 4: The Design Cycle

Patterns have to be designed in various steps expressed below:
*Step 1)* **Data collection:** During this step Collect training and testing data. Next the question arises How can we know when we have adequately large and representative set of samples?
*Step 2)* **Feature selection:** During this step various details have to be investigated such as Domain dependence and prior information ,Computational cost and feasibility, Discriminative features,

Similar values for similar patterns, Different values for different patterns, Invariant features with respect to translation, rotation and Scale, Robust features with respect to occlusion, distortion, deformation, and variations in environment.

*Step 3)* **Model selection:** During this phase select models based on following criteria: Domain dependence and prior information., Definition of design criteria, Parametric vs. non-parametric models, Handling of missing features, Computational complexity Various types of models are : templates, decision-theoretic or statistical, syntactic or structural, neural, and hybrid. Using these models we can investigate how can we know how close we are to the true model underlying the patterns?

*Step 4)* Training**:** Training phase deals with How can we learn the rule from data?

Supervised learning: a teacher provides a category label or cost for each pattern in the training set.

Unsupervised learning: the system forms clusters or natural groupings of the input patterns.

Reinforcement learning: no desired category is given but the teacher provides feedback to the system such as the decision is right or wrong.

*Step) 5* **Evaluation:** During this phase in the design cycle some questions have to be answered such as how can we estimate the performance with training samples? How can we predict the performance with future data? Problems of over fitting and generalization.[18]

### 6.1 Models in Pattern Recognition

Pattern recognition systems can be designed using the following main approaches: (i) Template Matching, (ii) Statistical methods, (iii) Syntactic methods and (iv) Neural networks. This paper will introduce the fundamentals of statistical pattern recognition with examples from several application areas. Techniques for analyzing multidimensional data of various types and scales along with algorithms for projection, dimensionality reduction, clustering and classification of data will be explained.[1,2]

**Table 1: Models in Pattern Recognition**

| Approach | Representation | Recognition Function | Typical Criterion |
|---|---|---|---|
| Template Matching | Samples, pixels, curves | Correlation, distance measure | Classification error |
| Statistical | Features | Discriminant function | Classification error |
| Syntactic or Structural | Primitives | Rules , grammar | Acceptance error |
| Neural Network | Samples ,pixels, features | Network Function | Mean square error |

## VII. PROCESS FOR PATTERN RECOGNITION SYSTEMS

As the figure 5 shows pattern recognition process has following steps.

1) Data acquisition and sensing: Measurements of physical variables like bandwidth, resolution, sensitivity, distortion, SNR, latency, etc.
2) Pre-processing: Removal of noise in data, Isolation of patterns of interest from the background.
3) Feature extraction: Finding a new representation in terms of features
4) Model learning and estimation: Learning a mapping between features and pattern groups and categories.
5) Classification: Using features and learned models to assign a pattern to a category.
6) Post-processing: Evaluation of confidence in decisions, Exploitation of context to improve performance Combination of experts.

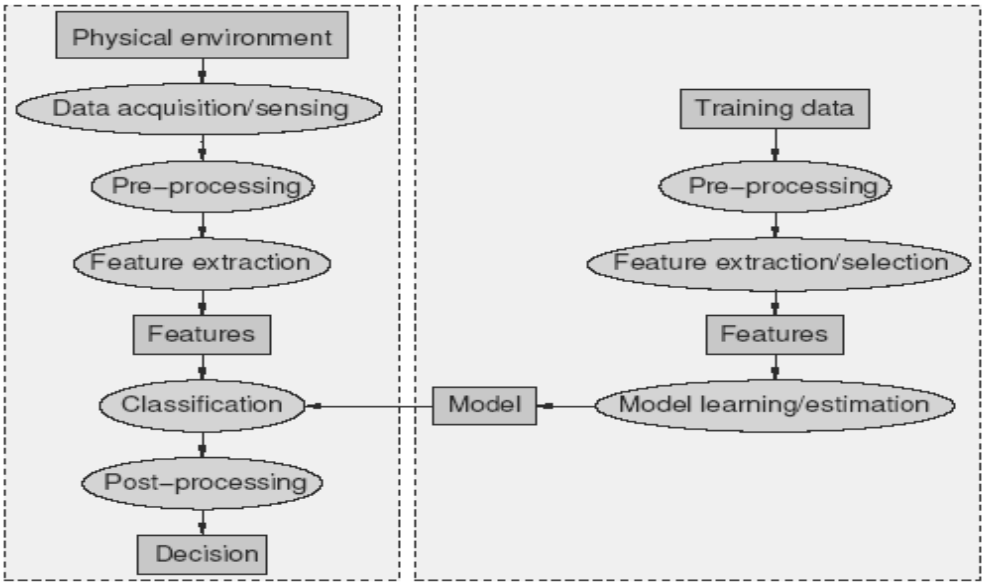


Figure5: Process Diagram for Pattern Recognition system

# VIII. PATTERN RECOGNITION APPLICATIONS

Overall Pattern recognition techniques find applications in many areas: machine learning, statistics, mathematics, computer science, biology, etc. There are many sub-problems in the design process; many of these problems can indeed be solved. More complex learning, searching and optimization algorithms are developed with advances in computer technology. There remain many fascinating unsolved problems. Pattern Recognition Applications to state here are English handwriting Recognition ,any other foreign language e.g. Chinese handwriting recognition, Fingerprint recognition, Biometric Recognition , Cancer detection and grading using microscopic tissue data, Land cover classification using satellite data, Building and non-building group recognition using satellite data ,Clustering of micro array data.[16]

**Table 2: Some of the examples of Pattern Recognition Applications**

| Problem Domain | Applications | Input Pattern | Pattern Classes |
|---|---|---|---|
| Bioinformatics | Sequence Analysis | DNA/Protein Sequence | Known types of genes or pattern |
| Data Mining | Searching for meaningful patterns | Points in multidimensional space | Compact and well separated clusters |
| Document Classification | Internet search | Text Document | Semantic Categories |
| Document Image Analysis | Optical character recognition | Document image | Alphanumeric characters, word |
| Industrial Automation | Printed circuit board inspection | Intensity or range image | Defective/ non- defective nature of product |
| Multimedia Database retrieval | Internet search | Video clip | Video genres (e.g. Action ,dialogue etc) |
| Biometric recognition | Personal identification | Face, iris, fingerprint | Authorized users for access control |
| Remote sensing | Forecasting crop yield | Multi spectral image | Land use categories ,growth patterns of crop |
| Speech recognition | Telephone directory | Speech waveform | Spoken words |
| Medical | Computer aided diagnosis | Microscopic image | |
| Military | Automatic target recognition | Optical or infrared image | Target type |
| Natural language processing | Information extraction | Sentences | Parts of speech |

# IX. STATISTICAL PATTERN RECOGNITION

Statistical pattern recognition is a term used to cover all stages of an investigation from problem formulation and data collection through to discrimination and classification, assessment of results and interpretation. Some of the basic terminology is introduced and two complementary approaches to discrimination described.[24]

### 9.1 Steps in Statistical pattern recognition

1. Formulation of the problem: gaining a clear understanding of the aims of the investigation and planning the remaining stages.
2. Data collection: making measurements on appropriate variables and recording details of the data collection procedure (ground truth).
3. Initial examination of the data: checking the data, calculating summary statistics and producing plots in order to get a feel for the structure.
4. Feature selection or feature extraction: selecting variables from the measured set that are appropriate for the task. These new variables may be obtained by a linear or nonlinear transformation of the original set (feature extraction). To some extent, the division of feature extraction and classification is artificial.
5. Unsupervised pattern classification or clustering. This may be viewed as exploratory data analysis and it may provide a successful conclusion to a study. On the other hand, it may be a means of preprocessing the data for a supervised classification procedure.
6. Apply discrimination or regression procedures as appropriate. The classifier is designed using a training set of exemplar patterns.
7. Assessment of results. This may involve applying the trained classifier to an independent test set of labeled patterns.
8. Interpretation. [57]

The above is necessarily an iterative process: the analysis of the results may pose further hypotheses that require further data collection. Also, the cycle may be terminated at different stages: the questions posed may be answered by an initial examination of the data or it may be discovered that the data cannot answer the initial question and the problem must be reformulated. The emphasis of this book is on techniques for performing steps 4, 5 and 6.

### 9.2 Statistical pattern recognition Approach

In the statistical approach, each pattern is represented in terms of d features or measurements and is viewed as a point in a d-dimensional space. The goal is to choose those features that allow pattern vectors belonging to different categories to occupy compact and disjoint regions in a d-dimensional feature space. The effectiveness of the representation space (feature set) is determined by how well patterns from different classes can be separated. Given a set of training patterns from each class, the objective is to establish decision boundaries in the feature space which separate patterns belonging to different classes. In the statistical decision theoretic approach, the decision boundaries re determined by the probability distributions of the patterns belonging to each class, which must either be specified or learned . One can also take a discriminate analysis-based approach to classification: First a parametric form of the decision boundary (e.g., linear or quadratic) is specified; then the ªbestº decision boundary of the specified form is found based on the classification of training patterns. Such boundaries can be constructed using, for example, a mean squared error criterion. The direct boundary construction approaches are supported by Vapnik's philosophy [162]: ªIf you possess a restricted amount of information for solving some problem, try to solve the problem directly and never solve a more general problem as an intermediate step. It is possible that the available information is sufficient for a direct solution but is insufficient for solving a more general intermediate problem.[57]

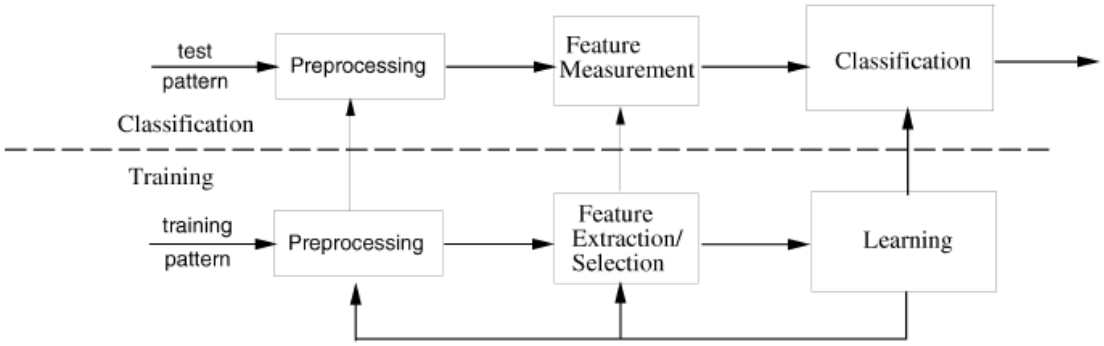


**Figure6 : Model for statistical pattern recognition**

## X. RESULT & DISCUSSION.

Pattern recognition is a field of study developing significantly from 1960s. It was very much an interdisciplinary subject, covering developments in the areas of statistics, engineering, artificial intelligence, computer science, psychology and physiology, among others. Pattern Recognition is such a field in Artificial Intelligence which has applications in varied domain such as Bioinformatics, Data Mining, Document Classification, Document Image Analysis, and Industrial Automation, Multimedia, Database retrieval, Biometric recognition, Remote sensing, Speech recognition, Medical, Military, Natural language processing. Statistical pattern recognition Approach, in the statistical approach, each pattern is represented in terms of d features or measurements and is viewed as a point in a d-dimensional space. The goal is to choose those features that allow pattern vectors belonging to different categories to occupy compact and disjoint regions in a d-dimensional feature space

## XI. AWARENESS OF RELATED WORK

There are various examples of Pattern Recognition Applications namely Bioinformatics, Data Mining Document Classification, Document Image Analysis, Industrial Automation, Multimedia Database retrieval, Biometric recognition, Remote sensing, Speech recognition,, Medical,, Military, Natural language processing where various Input Pattern such as DNA/Protein Sequence ,Points in multidimensional space, Text Document, Document image, Intensity or range image, Video clip, Face, iris, fingerprint, Multi spectral image, Speech waveform, Microscopic image, Optical or infrared image, Sentences to match the pattern classes such as Known types of genes or pattern ,Compact and well separated clusters ,Semantic Categories ,Alphanumeric characters, word, Defective/ non- defective nature of product ,Video genres (e.g. Action ,dialogue etc) ,Authorized users for access control Land use categories ,growth patterns of crop ,Spoken words, Target type, Parts of speech. The researcher has a wide interest in this field and is trying to do research in Biometric recognition and maintenance of attendance in some organizations in India

## XII. CONCLUSIONS

Pattern Recognition plays a very vital role in Artificial intelligence. But now a day's pattern recognition has become a day to day activity in everyday's life. As human beings have limitations in recognizing various items, the field of pattern recognition is becoming very popular. The goal of pattern recognition research to clarify complicated mechanisms of decision making processes and automatic these function using computers is implemented in day to day life. Pattern recognition has various applications in numerous fields as data mining, biometrics, sensors, speech recognition, medical, military, natural language processing etc. Statistical pattern recognition is used to cover all stages of an investigation from problem formulation and data collection through to discrimination and classification, assessment of results and interpretation. Here each pattern is represented in terms of d

features or measurements and is viewed as a point in a d-dimensional space. The authors have deep interest in the same field and my further research will explore the same area. Pattern recognition applications include Sequence Analysis, Searching for meaningful patterns, Internet search, Optical character recognition, Printed circuit board inspection, Internet search, Personal identification, Forecasting crop yield, Telephone directory, Computer aided diagnosis, Automatic target recognition, Information extraction. Various approaches in Pattern Recognition are Template Matching, Statistical, Syntactic or Structural and Neural Network. In Statistical pattern recognition the analysis of the results may pose further hypotheses that require further data collection. Also, the cycle may be terminated at different stages: the questions posed may be answered by an initial examination of the data or it may be discovered that the data cannot answer the initial question and the problem must be reformulated. Pattern recognition techniques find applications in many areas: machine learning, statistics, mathematics, computer science, biology, etc. There are many sub-problems in the design process. Many of these problems can indeed be solved. More complex learning, searching and optimization algorithms are developed with advances in computer technology. There remain many fascinating unsolved problems

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# ANALYTICAL CLASSIFICATION OF MULTIMODAL IMAGE REGISTRATION BASED ON MEDICAL APPLICATION

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***ABSTARCT***

*In the last two decades, computerized image registration has played an important role in medical imaging. One of the important aspects of image registration is multimodal image registration, where is used in many medical applications such as diagnosis, treatment planning, computer guided surgery. Not specified the relationship between the intensity values of corresponding pixels, the difference between images contrast in some areas than other areas, mapping the intensity values in an image to multiple intensity value in other images, are challenging problems in multimodal image registration. Due to importance of image registration in medical, identification this challenges seem necessary. This paper will have a comprehensive analysis on several types of multimodal image registration methods and will express its affect on medical images. To reach this goal, each method will investigate according to its affect on the field of medical imaging and challenges facing each method will evaluate analytically. So that recognition these challenges play an effective role in choosing an appropriate registration method.*

***KEYWORDS***: Image registration, medical image registration, multimodal image registration, information theory

## I. INTRODUCTION

Image registration is the problem of alignment two or more image of different viewpoint, at different times or with different kinds of imaging sensors. Registration is important application in many image processing and is used in many medical imaging applications. One of the important aspects of image registration is multimodal image registration, so that different sensors are used for imaging of an image. In this case, the image registration provide tools for gathering information from various device and are created a more detailed views.In recent years, multimodal image registration is one of the challenging problems in medical imaging. Due to changes in the rotation and size, differences in brightness and images contrast, is difficult for a physician to combine mentally all image information carefully. Moreover, the radiotherapy techniques using manual adjustment on the MRI and CT brain images may require several hours to be analysis [1, 2]. Therefore, an image registration technique is required until to transfer all image information to a general information system.

Essentially, image registration methods are divided into three categories based on landmark, segmentation and voxel. Major challenges in multimodal image registration are variety of intensity images obtained from different sensors. Since voxel based methods is applied directly on image gray values, they are more general. Due to importance of medical images, speed and accuracy of registration process should be considered. Accordingly, this paper introduces the medical image registration methods and will be introduced types of multimodal image registration, then these measure compare with measures such as speed, accuracy, computational complexity. Finally, we were trying to evaluate this methods effect in the field of medical imaging. The rest of this paper is organized as follows: In section 2, the related work and proposed definitions for image registration and multimodal medical image registration is introduced. We describe medical image registration

methods in section 3. In section 4, the proposed framework for classification of multimodal methods is presented and section 5 evaluates these methods. Section 6 includes the conclusion.

# II. RELATED WORK

Generally, image registration is the process of image component transformation to a coordinate system that from image processing viewpoint, the most interesting and possibly most difficult step is to determine the proper transformation that transform these components to normal coordinates [3]. A system for performing image registration algorithms uses of machine vision, image processing, machine learning and artificial intelligence [2, 4]. In recent decades, imaging changes identification in remote sensing has been much attention [5, 6]. In radiographic, images automatically compare and match and in mammography, cancer cases is easily determined [7, 8]. Image registration can be applied in the diagnosis and identification steps, such as face detection, handwriting recognition, stereo matching and motion analysis [3, 4]. One of the important aspects of image registration is when various devise used to imaging of a scene. .Therefore, an image registration technique is required to transfer all image information to a general information system. In this case, the goal is to display images so that to facilitate diagnostic for physicians to find the desired image information similarities and differences [9]. More recently developed fully automated methods essentially revolve around entropy [10] and mutual information [11, 12]. In this way we can understand that image registration in recent years applied to one of the important areas in image processing.

# III. MEDICAL IMAGE REGISTRATION METHODS

Image registration is the problem of alignment two or more image of different viewpoint, at different times or with different kinds of imaging sensors. Registration is important application in many image processing and is used in many medical imaging applications. One of the important aspects of image registration is multimodal image registration, so that different sensors are used for imaging of an image. In this case, the image registration provide tools for gathering information from various device and are created a more detailed views.In recent years, multimodal image registration is one of the challenging problems in medical imaging. Image registration is used in analyzing medical images for diagnosis, in machine vision for stereo matching, in astrophysics to adjust images with different frequencies and many other areas. In medicine, patients often in order to better diagnosis or treatment is imaging with multiple radiology sensors. Due to changes in rotation or difference in image contrast, is difficult for a physician to combine mentally all image information carefully. Therefore, an image registration technique is necessary to transfer all image information to an overall system.

As shown in Figure (1), image registration is used to gather information from various sensors and provide more detailed views. Main methods of image registration are divided into three categories: intrinsic, extrinsic and non image. Since intrinsic methods are used mainly for multimodal image registration, these methods will review.

Intrinsic methods are classified into landmark, voxel and segmentation based.

Landmark extraction and image segmentation in some registration methods is difficult while voxel based methods are practical and more general [13].

## 3.1 Landmark based registration

Landmarks are based on anatomy i.e. clear and visible points, which usually are determined by the user interaction or are geometric i.e. local areas such as maximum curvature, corners, etc, so that usually are defined in an automated method. In landmark based registration, a set of specific points is compared with the first image content. These algorithms use of criteria such as average distance between every landmark or distance between landmark with the lowest frequency.

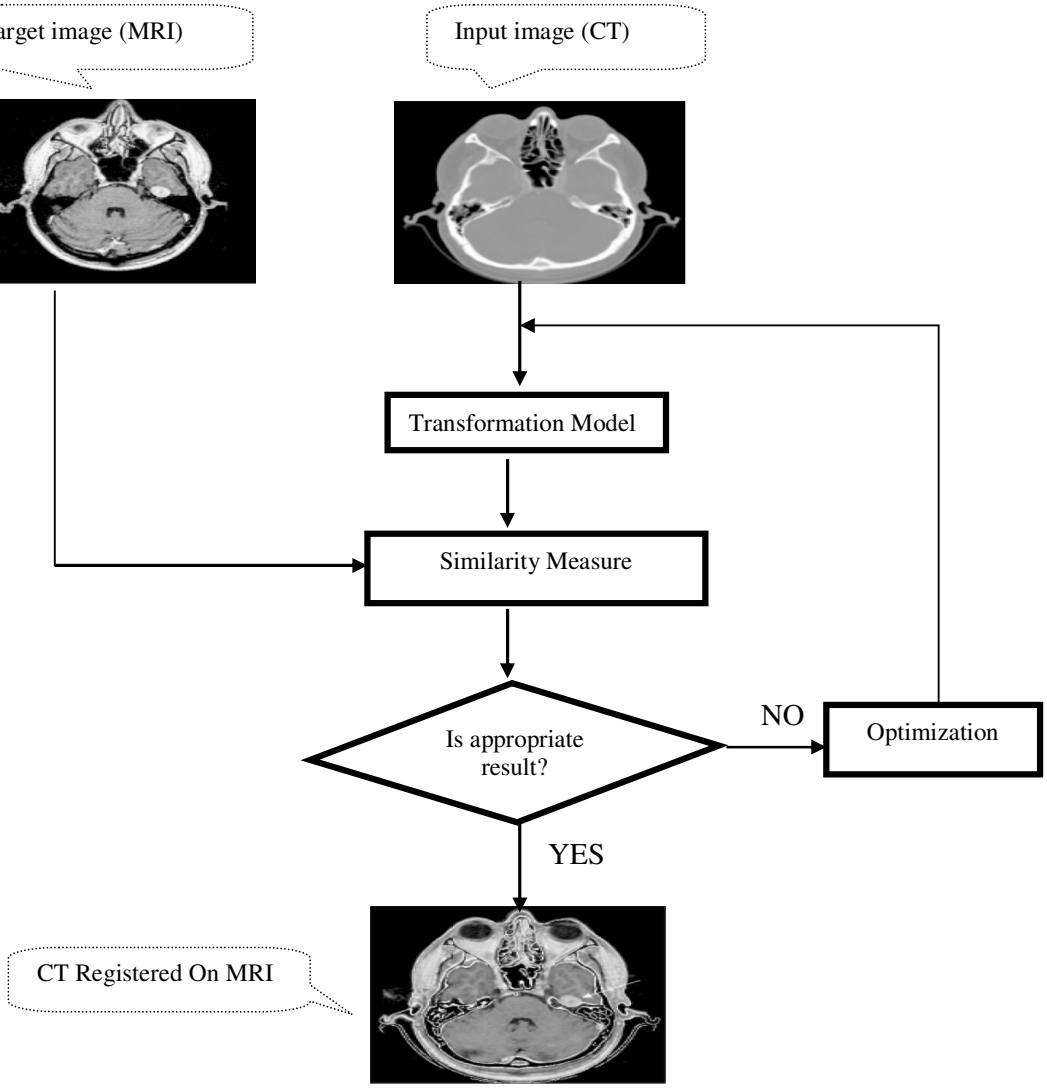


Figure (1): a multimodal image registration system

### 3.2 Segmentation based registration

Segmentation based registration is rigid where have been extracted from similar image structures to be registered, and they can also be deformable model where an extracted structure from one image is elastically deformed to fit the second image. Rigid model based approaches are probably the most popular methods currently in clinical use. Their popularity relative to other approaches is due to the head-hat method which relies on the segmentation of the skin surface from CT, MR and PET images of the head. Another cause is the fast chamfer matching technique for alignment of binary structure by means of a distance transform.

### 3.3 Voxel based registration

This method directly is applied on the image gray values and does not require to preprocessing and user interaction. There are two distinct methods: decrease the content of gray value image to a series of scalars and orientations. Second for all images content, has been used through the registration process. Methods using all image content, can be applied to almost every field of medicine with the use of any transformation to be used. as shown in figure (2), Since multimodal image registration is affected by the intensity and methods based on the intensity are applied of gray values image, these

category of methods are used for multimodal image registration.

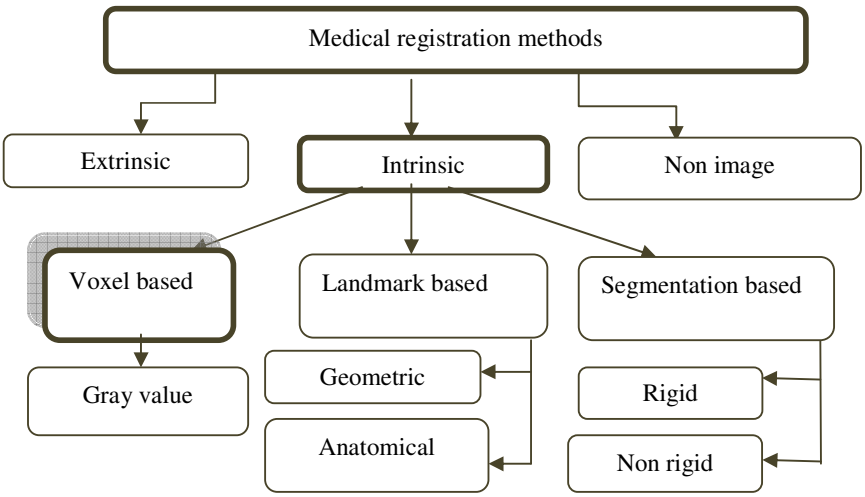


Figure (2): medical registration methods classification

# IV. PROPOSED FRAMEWORK FOR MULTIMODAL IMAGE REGISTRATION METHODS

Multimodal image registration is one of challenging issue in the field of medical imaging. Therefore, choose the method with minimum error for medical image registration may seem important. In this section, various methods of multimodal image registration and the challenges of each method will explained. In medicine, patients often in order to better diagnosis or treatment is imaging with multiple radiology sensors. Due to changes in rotation or difference in image contrast, is difficult for a physician to combine mentally all image information carefully. Therefore, an image registration technique is necessary to transfer all image information to an overall system. As shown in figure (3), using this classification, a suitable method for multimodal medical image registration can be selected. This section includes the proposed framework for classification of multimodal image registration methods and applications and challenges of each method in the field of medical imaging will be evaluated.

## 4.1 Information theory based methods

In recent decades, Information theory is used to effectively in multimodal image registration. In this part, measures of information theory and its applications in medical image registration is expressed.

### 4-1-1- Entropy

Shannon entropy for an image is calculated based on probability distribution of image gray values. When different sensors are used for imaging, display the intensity of an area in two images, is different. Consequently, the aim is reducing variance than the registration obtained .

The histogram in entropy based methods contains the combination of gray values in each of the two images for all corresponding points. When images are aligned correctly, joint histogram shows exact clusters of gray values.

In order to measure the joint histogram distribution of two images, Shannon entropy is used, its formula is shown in equation (1).

$$H(I_1, I_2, T_\alpha) = -\sum_{a,b} p_{I_1,I_2}(a,b) \log p_{I_1,I_2}(a,b) \quad (1)$$

$$a = I_1(x_1, y_1) \quad (2)$$

$$b = I_2(T_\alpha(x_1, y_1)) \quad (3)$$

$I_1$ and $I_2$ are two images that geometrically marked with $T_\alpha$ transformation, So that pixels $(x_1, y_1)$ in $I_1$ with an intensity, is correspond to the pixel $T_\alpha(x_1, y_1)$ in the $I_2$ with b intensity . While $P_{I1, I2}(a, b)$, that

express a highly probable value pairs in the image $I_1$ and $I_2$ is correspond to the image intensity b. with finding $T_{a,}$ is minimized entropy transformation and images registered [14] .

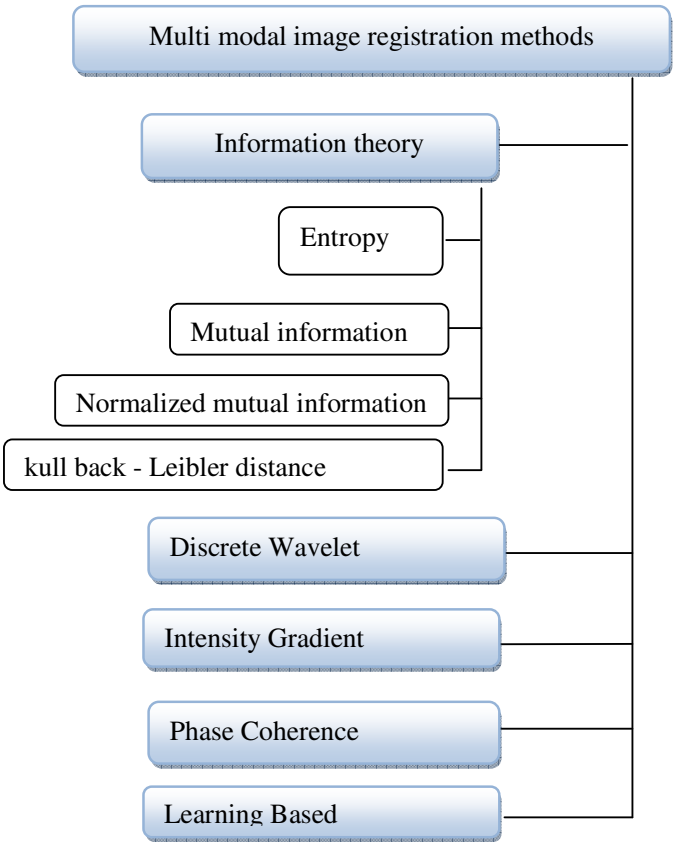


Figure (3): classification of multimodal image registration methods

### 4-1-2- Mutual Information

Shannon entropy problem is that lower values can lead to false match. For example, if only one element have been within the area of overlap of the two images, is produced a sharp peak in the joint distribution, Thus reduced the amount of entropy. Mutual information is one of the automatic image registration methods in medical imaging where it offers a measure of dependence between two images.

Equation (4) is mutual information definition so that I ($I_1$, $I_2$, $T_\alpha$) is mutual information measure that aligned with $T_\alpha$ transformation.

$$I(I_1,I_2,T_\alpha)=H(I_1)+H(I_2)-H(I_1,I_2,T_\alpha) \qquad (4)$$

H ($I_1$), H ($I_2$) is based on border probability of intensity values in overlapping area of images.

### 4-1-3- Normalized Mutual Information

Size of parts with overlapping images, to impress the measure of mutual information in two ways: First, low overlapping, reduces the number of samples, so that is low statistical power of estimating the probability. Second, with increasing misalignment, which usually is associated with reduced overlap, the measure of mutual information increases. When total entropy increase marginal entropy is connected faster. Thus, a measure of normalized mutual information was provided less sensitive to changes that are overlapping [14].

**4-1-4-Kull back–Leibler Distance**

This method is based on a priori knowledge of the expected joint intensity distribution estimated from aligned training images. One of the key features is the use of the expected joint intensity distribution between two pre-aligned, training images as a reference distribution. The goal is to align any two images of the same or different acquisitions such that the expected distribution and the observed joint intensity distribution are well matched. In other words, the registration algorithm aligns two different images based on the expected outcomes. The difference between distributions is measured using the Kullback - Leibler distance (KLD). The KLD value tends to zero when the two distributions become equal. The registration procedure is an iterative process and is terminated when the KLD value becomes sufficiently small [15]. The Kullback - Leibler distance between the two distributions is given by equation (5):

$$D(PT \,||\, \mathrm{Pref}) = \sum_{i1,i2=0}^{255} \mathrm{PT(i1,i2)} \log \frac{\mathrm{PT(i1,i2)}}{\mathrm{Pref(i1,i2)}} \qquad (5)$$

The idea behind the registration technique is thus, to find a transformation $T_0$, acting on the floating image, that minimizes the KLD between the joint intensity distribution $P_{T0}$ and the reference distribution $P_{\mathrm{ref}}$. Or, in formula (6):

$$T_0 = \arg\min_T D\,(P_T \,||\, P_{\mathrm{ref}}) \qquad (6)$$

### 4.2 Discrete wavelet

In this method, firstly multimodal images are decomposed by wavelet transformation. Then calculated an energy mapping of detailed images from the subclass and is used genetic algorithm to obtain the absolute minimum total distance between the energy maps [16].

### 4.3 Intensity Gradient

The idea of applying this method is to determine similarity between images based on all images so that the image structure can be defined by changes in intensity. In this method, an image intensity change can be detected via the image gradient and considered the normalized gradient field, which is purely geometric information. Computation gradient is less sensitive and allow deal with noisy image [17].

### 4.4 Phase Correlation

The main challenge in automatic multimodal image registration is inconsistency in the intensity values and or contradiction between patterns and missing data between images. A method based on local phase dependency is not sensitive to the variation intensity, contrast or noise and provides efficient method for providing important characteristic of image. In multimodal image registration, a feature extraction method based on local fuzzy correlation measure is described. This feature show the behavior of local phase structure at various scales in near sharp image features. With a reference image and an input image, algorithm making the mapping of local fuzzy dependency for both images and estimation of transformation parameters will do registration using an objective function [18].

### 4.5 Learning Based Method

In learning based methods, Instead of using a universal, but a priori fixed similarity criterion such as mutual information, a similarity measure is learned, such that the reference and correctly deformed floating images receive high similarity scores. In other words, objective function is to maximize the correlation between input and reference images and to achieve the desired results, not preset preprocessing images [19, 20].

Multi modal image registration is the task of inferring a spatial transformation T for a reference image $I_r$ and its corresponding floating image $I_f$. Given a similarity function s that quantifies the compatibility of aligned reference-floating image pairs, the optimal transformation of ($I_r$, $I_f$) is found by maximizing the similarity over all possible transformations, such as equation (7):

$$T^* = \arg\max_{T \epsilon \tau} s\,(I_r, I_f \circ T) \quad (7)$$

Our goal is to train a similarity function s over a sample of pre-aligned image pairs such that the empirical cost of mis-registration. Figure (4) show an overview of a learning-based image registration system.

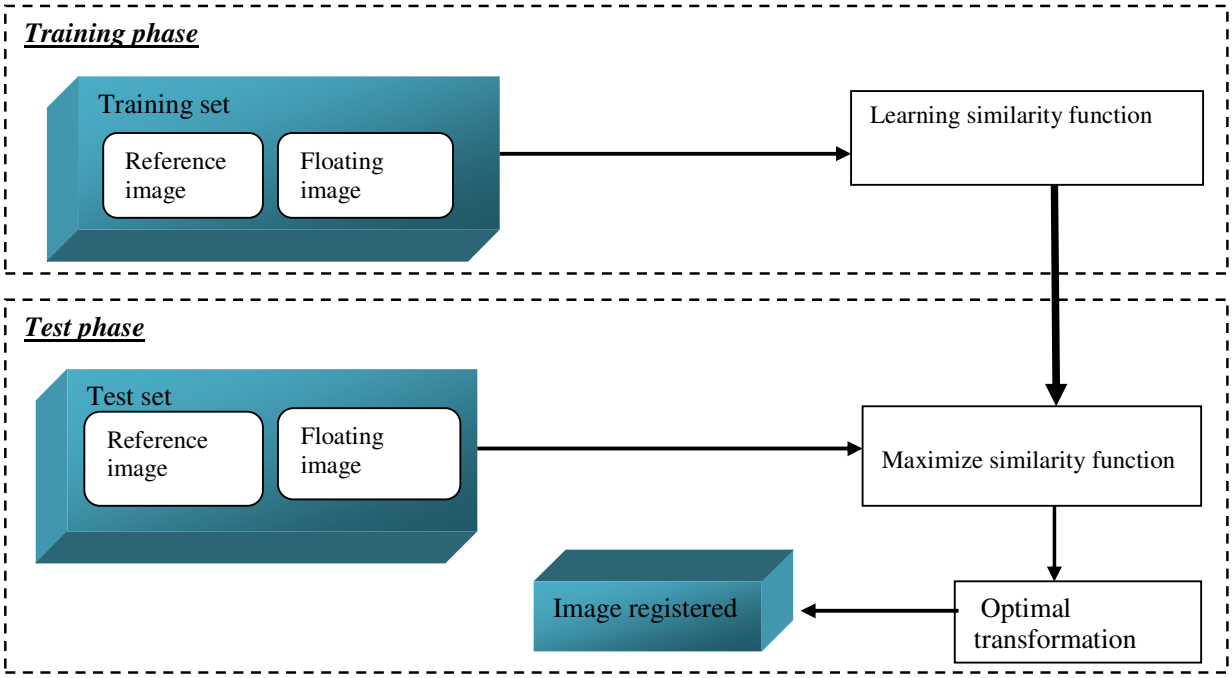


Figure (4): An Overview of a learning-based image registration system

## V. EVALUATION OF MULTIMODAL MEDICAL IMAGE REGISTRATION VARIOUS METHODS

Generally, multi modal image registration methods are divided into three categories based on landmark, segmentation and voxel. As was expressed earlier, multimodal registration have more publicity on some medical images, Since medical imaging requires two principles accuracy and speed, in selecting an appropriate method of multimodal image registration according to these principles are important. Table (1) and table (2) evaluate amount of influence each of these methods on multimodal medical image registration process. The functional measures that considered in our evaluation of multimodal medical image registration are as follows:

- User Interaction: A multimodal image registration method usually is intensity based. They are in general fully automatic without the need for user interaction.
- Speed: A multimodal image registration method must guarantee high speed.
- Accuracy: A multimodal image registration approach must provide high accuracy in dealing with medical data.
- Computational complexity: This property express that how many iteration dose the algorithm need to find the optimal solution.
- According to studied the evaluation criteria can be seen that, methods based on voxel are effectiveness than other methods.

## VI. CONCLUSION

Not specified the relationship between the intensity values of corresponding pixels, the difference

between images contrast in some areas than other areas, mapping the intensity values in an image to multiple intensity value in other images, are challenging problems in multimodal image registration. Due to importance of image registration in medical, identification this challenges seem necessary. This paper had a comprehensive analysis on several types of multimodal image registration methods and expressed its affect on medical images area. To reach this goal, each method was investigated according to its affect on the field of medical imaging. Results of several studies, indicate that among several existing methods in multimodal image registration, voxel based methods is more important. Because of voxel based methods are applied on the image intensity values, are more important. Since, the main challenge in multimodal registration is diversity of image intensity obtained from different sensor, select the method that can identify the multimodal image registration main requirements (speed and accuracy) in the medical field, is the other objectives of this paper.

**Table (1): evaluation of multimodal medical image registration methods**

| Computational complexity | Accuracy | Speed | User interaction | Challenge | Similarity measure example | General approach | Evaluation / approach | |
|---|---|---|---|---|---|---|---|---|
| high | low | low | interactive | User interaction | Nearest Iterative point | Determine the geometric features matching interactive | landmark | Multi modal medical image registration |
| Almost low | Almost low | Almost low | Automatic and semi automatic | Dependency between accuracy and segmentation | Chamfer | alignment of binary structures by means of a distance transform | segmentation | |
| low | high | high | automatic | ……. | Information theory | using all the image content with computation of gray value | voxel | |

Table (2): Multimodal registration methods analysis

| accuracy | speed | User interaction | Challenge | General approach | evaluation / approach | |
|---|---|---|---|---|---|---|
| low | high | automatic | Local maximum | Measuring joint histogram distribution with different intensity | Information theory | Multimodal registration |
| Almost high | Almost high | automatic | Don't responsible in depth and internal area of image | Fast wavelet transform for energy mapping from first function | Wavelet transform | |
| high | high | automatic | Observed based | definition image structure using intensity change with gradient calculation | Intensity Gradient | |
| Almost low | Almost low | Semi automatic | Don't responsible with change in rotation or size | A feature based method based on Phase dependency that use of weighted mutual information | Phase Coherence | |
| high | high | automatic | Network train | Maximize the similarity using a learning based method | Learning based | |

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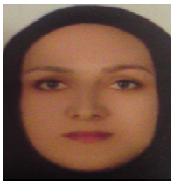

# OVERVIEW OF SPACE-FILLING CURVES AND THEIR APPLICATIONS IN SCHEDULING

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## *ABSTRACT*

*Space-filling Curves (SFCs) have been extensively used as a mapping from the multi-dimensional space into the one-dimensional space. A space-filling curve (SFC) maps the multi-dimensional space into the one-dimensional space. Mapping the multi-dimensional space into one-dimensional domain plays an important role in every application that involves multidimensional data. Modules that are commonly used in multi-dimensional applications include searching, scheduling, spatial access methods, indexing and clustering. Space-filling curves are adopted to define a linear order for sorting and scheduling objects that lie in the multi-dimensional space. Space filling curves as the basis for scheduling has numerous advantages, scalability in terms of the number of scheduling parameters, ease of code development and maintenance. This paper elaborates the space-filling curves and their applicability in scheduling, especially in transaction and disk scheduling in advanced databases.*

## *KEYWORDS*

*Scheduling, Space-filling Curve, Real-time Database, Disk Scheduling, Transaction Scheduling.*

## I. INTRODUCTION

Many people have devoted their efforts to find a solution to the problem of efficiently scheduling task or transaction with multi-dimensional data. This problem has gained attention in the last years with the emergence of advanced database system and operating system such as real-time databases, real-time operating system which need to schedule and process the task or transaction in an efficient way. Hence, techniques that aim to reduce the dimensionality of the data usually have better performance. One such way of doing this is to use a space-filling curve. A space-filling curve can transform the higher dimensional data into a lower dimensional data using some mapping scheme.

Space-filling Curves (SFCs) have been extensively used as a mapping from the multi-dimensional space into the one-dimensional space. A space-filling curve (SFC) [1] maps the multi-dimensional space into the one-dimensional space. Mapping the multi-dimensional space into one-dimensional domain plays an important role in every application that involves multidimensional data. Multimedia databases, geographical information systems, QoS routing, image processing, parallel computing, data mapping, circuit design, cryptology and graphics are examples of multi-dimensional applications. Modules that are commonly used in multi-dimensional applications include searching, scheduling, spatial access methods, indexing and clustering [2, 3, 4].

A space-filling curve is a way if mapping the multi-dimensional space into the one-dimensional space. An SFC acts like a thread that passes through every cell element (or pixel) in the multi-dimensional space so that every cell is visited exactly once. Thus, space-filling curves are adopted to define a linear order for sorting and scheduling objects that lie in the multi-dimensional space. Figure 1 gives examples of six two-dimensional space-filling curves. Using space-filling curves as the basis for scheduling has numerous advantages, like:

- Scalability in terms of the number of scheduling parameters,
- Ease of code development and maintenance,
- The ability to analyze the quality of the schedules generated, and
- The ability to automate the scheduler development process in a way similar to automatic generation of programming language compilers.

Mapping from the multi-dimensional space into the one-dimensional domain provides a pre-processing step for multi-dimensional applications. The pre-processing step takes the multi-dimensional data as input and outputs the same set of data represented in the one-dimensional domain. The idea is to keep the existing algorithms and data structure independent of the dimensionality of data. The objective of the mapping is to represent a point from the D-dimensional space by a single integer value that reflects the various dimensions of the original space.

The rest of the paper is organized as follows. Section 2 surveys some of the related work on space-filling curves. Section 3 describes about mapping in space-filling curves. Section 4 describes about space filling curves application in scheduling transaction in active and real-time database. Section 5 describes again its usage in disk request scheduling in multimedia databases. Finally we conclude in section 5.

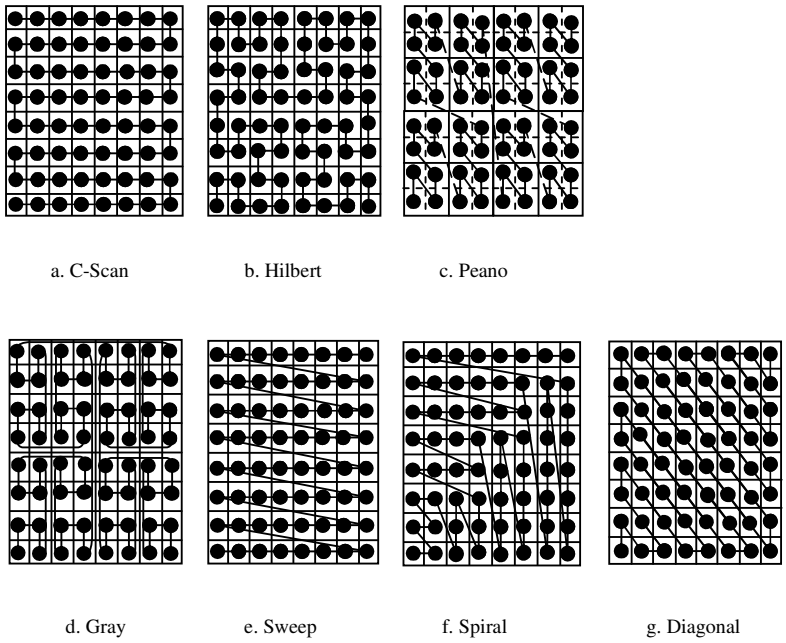


Figure1. Space-Filling curves examples.

## II. RELATED WORK

The notion of space-filling curves has origins in the development (in 1883) of the concept of the Cantor set. Peano in 1890 and Hilbert in 1891 provided explicit descriptions of such curves. In 1890 Peano discovered a densely self-intersecting curve that passes through every point of the unit square. Purpose was to construct a continuous mapping from the unit interval onto the unit square. Peano was motivated by Georg Cantor's earlier counterintuitive result that the infinite number of points in a unit interval is the same cardinality as the infinite number of points in any finite-dimensional manifold, such as the unit square. The problem Peano solved was whether such a mapping could be continuous, i.e., a curve that fills a space [4].

Bokhari & Aref [5] apply 2D and 3D Hilbert curves to binary dissection of nonuniform domains while taking into account shape, area, perimeter, or aspect ratio of regions. Ou et al. [6] propose a partitioning based on SFCs that is scalable, proximity improving and communication minimizing. Aluru and Sevilgen [7] discuss load balancing using SFCs. They show how nonuniform and dynamically varying data grids can be mapped onto SFCs, which can then be partitioned over processors. Chatterjee et al. [8] show the applications of Hilbert curves to matrix multiplication. Recent research by Zhu and Hu [9] also describes the use of Hilbert curves for load balancing. In [10], Jagadish presents an analysis of the Hilbert curve for representing two-dimensional space. Moon et al. [11] analyze the clustering properties of the Hilbert curve and compare the performance of Hilbert curves with Z-curves. This paper also includes a good historical survey.

## III. MAPPING IN SPACE FILLING CURVES

A space-filling curve must be everywhere self-intersecting in the technical sense that the curve is not injective. If a curve is not injective, then one can find two "subcurves" of the curve, each obtained by considering the images of two disjoint segments from the curve's domain. The two subcurves intersect if the intersection of the two images is non-empty. One might be tempted to think that the meaning of "curves intersecting" is that they necessarily cross each other, like the intersection point of two non-parallel lines, from one side to the other. But two curves (or two subcurves of one curve) may contact one another without crossing, as, for example, a line tangent to a circle does.

In general, space-filling curves start with a basic path on a k-dimensional square grid of side 2. The path visits every point in the grid exactly once without crossing itself. It has two free ends, which may be joined with other paths. The basic curve is said to be of order 1. To derive a curve of order i, each vertex of the basic curve is replaced by the curve of order i, which may be appropriately rotated and/or reflected to fit the new curve [5].

The basic Peano curve for a 2*2 grid, denoted N1, is shown in Figure 2. To derive higher orders of the Peano curve, replace each vertex of the basic curve with the previous order curve. Figure 2 also shows the Peano curve of order 2 and 3.

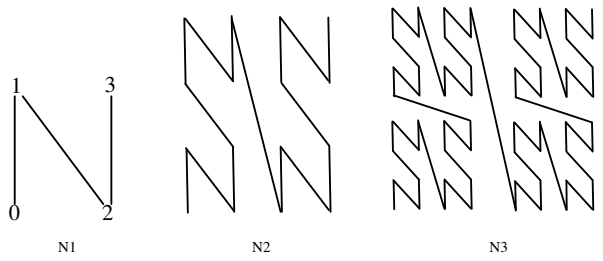


Figure 2. Peano curves of order 1, 2 and 3.

The basic reflected binary gray-code curve of a 2*2 grid denoted R1 is shown in figure 3 (a). The procedure to derive higher orders of this curve is to reflect the previous order curve over the x-axis and then over the y-axis. Figure 3 (a) also shows the reflected binary gray-code curve of order 2 and 3.

The basic Hilbert curve of a 2*2 grid, denoted H1, is shown in figure 3 (b). The procedure to derive higher orders of the Hilbert curve is to rotate and reflect the curve at vertex 0 and at vertex 3. The curve can keep growing recursively by following the same rotation and reflection pattern at each vertex of the basic curve [Lu, 2003]. Figure 3 (b) also shows the Hilbert curves of order 2 and 3. An algorithm to draw this curve is described in [Griffiths, 1986].

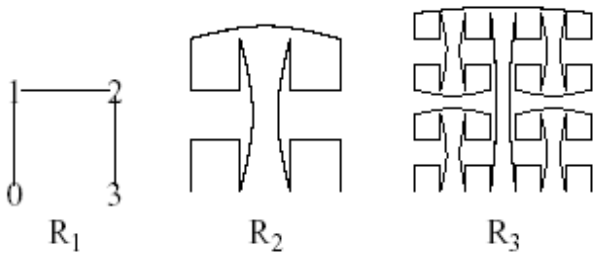


Figure 3 (a). Reflected binary gray-code curves of order 1, 2 and 3.

The path of a space-filling curve imposes a linear ordering, which may be calculated by starting at one end of the curve and following the path to the other end. [Orenstein & Merrett, 1984] used the term **z-**ordering to refer to the ordering of the Peano curve.
The Space-filling curves are used for scalability, fairness and intentional bias [Mokbel & Aref, 2001]. The SFC are scalable, when any new parameter comes into picture a new dimension can be added or number of points per dimension can be increased. The space-filling curve is said to be fair if it results in similar irregularity for all dimensions. The notion of irregularity is the measure of goodness for the mapping of each space-filling curve.

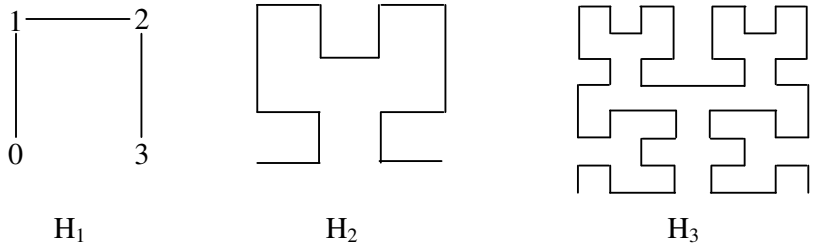


Figure 3 (b). Hilbert curves of order 1, 2 and 3.

## IV. SCHEDULING TRANSACTIONS USING SFC IN DATABASES

In [12] a new transaction-scheduling scheme is proposed for real-time database system based on three-dimensional design by integrating the characteristics of value, deadline and criticalness. Here space-filling curves can be used as they are adopted to define linear order for sorting or scheduling. The space filing curves unnaturally considers value, deadline and criticalness information and gives a scheduling sequence. A CPU request is modeled by multiple parameters, (e.g., the real-time deadline, the criticalness, the priority, etc.) and represented as a point in the multi-dimensional space where each parameter corresponds to one dimension. Using a space-filling curve, the multi-dimensional CPU request is converted to a one-dimensional value.
A CPU request *T* takes a position in the thread path according to its space-filling curve value. They are then stored in the priority queue q according to their position in the thread path. The CPU scheduler walks through the thread path by serving all CPU requests in queue according to their path position, which is their one-dimensional value with a lower value indicating a higher priority. Figure 4 gives an illustration of an SFC-based CPU scheduler.

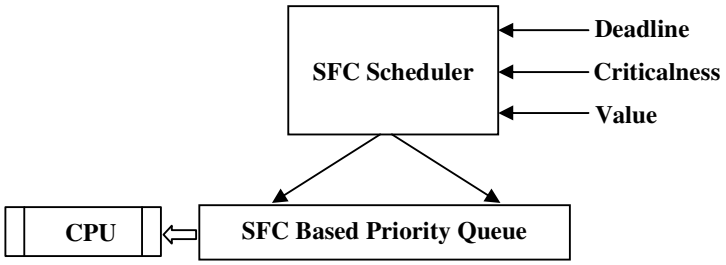


Figure 4. Space filling curve based CPU scheduler.

The space filling curves converts 3-dimensional space using the idea of bit interleaving which is used and described in [3, 5]. Every point in the space takes a binary number that results from interleaving bits of the two dimensions. The bits are interleaved according to the interleaving vector (0,1,0,1). This corresponds to taking the first and third bits from dimension 0 (x) and taking the second and fourth bits from dimension 1(y). The result of applying this bit interleaving is shown Table 1.
The sequence of few transactions obtained after mapping from 3-D to 1-D is shown in table 3.1 below.

**Table 1. Mapping Table from 3-D to 1-D.**

| Point | Dimensions | | | Bit | Decimal code |
|---|---|---|---|---|---|
| | 0 | 1 | 2 | | |
| (0,1,2) | 000 | 001 | 010 | 000001010 | 10 |
| (2,1,4) | 010 | 001 | 100 | 001100010 | 98 |
| (0,0,7) | 000 | 000 | 111 | 001001001 | 73 |
| (7,0,7) | 111 | 000 | 111 | 101101101 | 365 |
| (7,4,2) | 111 | 100 | 010 | 110101100 | 428 |

The evaluation results and comparison with different algorithms for CPU scheduling in [5, 12] show that the CPU utilization of our algorithm (SFCP) is maximum and success ratio is better.

## V. DISK-SCHEDULING ALGORITHMS BASED ON SPACE-FILLING CURVES

The problem of scheduling a set of tasks with time and resource constraints is known to be NP-complete [13]. Several heuristics have been developed to approximately optimize the scheduling problem. Traditional disk scheduling algorithms [14] are optimized for aggregate throughput. These algorithms, including SCAN, LOOK, C-SCAN, and SATF (Shortest Access Time First), aim to minimize seek time and/or rotational latency overheads.
They offer no QoS assurance other than perhaps absence of starvation. Deadline-based scheduling algorithms [13, 15, 16] have built on the basic earliest deadline first (EDF) schedule of requests to ensure that deadlines are met. These algorithms, including SCAN-EDF and feasible-deadline EDF, perform restricted reorderings within the basic EDF schedule to reduce disk head movements while preserving the deadline constraints. Like previous work on QoS-aware disk scheduling, space-filling curves explicitly recognize the existence of multiple and sometimes-antagonistic service objectives in the scheduling problem.
A more general model of mapping service requests in the multi-dimensional space into a linear order that balances between the different dimensions is given [4, 5]. Disk schedulers based on space-filling curves generalize traditional disk schedulers.
In the QoS-aware disk scheduler, a disk request is modeled by multiple parameters, (e.g., the disk cylinder, the real-time deadline, the priority, etc.) and represented as a point in the multi-dimensional space where each parameter corresponds to one dimension. Using a space-filling curve, the multi-dimensional disk request is converted to a one-dimensional value. Then, disk requests are inserted

into a priority queue according to their one-dimensional value with a lower value indicating a higher priority. Figure 5 gives an illustration of an SFC-based disk scheduler**.**

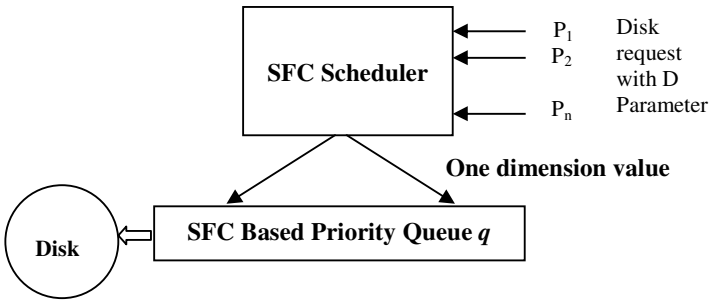


Figure 5. SFC-based disk scheduler

A new conditionally-preemptive disk scheduling algorithm is proposed [5] with SFC which trade-off between the fully-preemptive and the non-preemptive disk schedulers. In the conditionally-preemptive disk-scheduling algorithm, a newly arrived disk request $T_{new}$ preempts the process of walking through a full cycle if and only if it has significantly higher priority than the currently served disk request.
In [3] describes many benefits of SFC in disk scheduling minimizing priority inversion, avoiding starvation, effective disk utilization in context of real-time constraints based request by considering other parameter associated with request.

## VI. CONCLUSION

In this paper, we describe and review space-filling curves. Space-filling curve techniques have certain unique properties like map the multiple QoS parameters into the one-dimensional space. These properties have been used in recently for scheduling CPU transaction and disk request in real-time environment. Also their mapping and advantages are explored. Our brief description and study about SFC, we say that SFC can further be used in many more application area just like scheduling task in real-time operating system where each task is having its own important associated with multiple parameter or dimension.

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# COMPACT OMNI-DIRECTIONAL PATCH ANTENNA FOR S-BAND FREQUENCY SPECTRA

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## *ABSTRACT*

*This paper presents a novel design of a microstrip patch antenna with compact nature and the study of various antenna parameters to suit the applications such as WiMax operating in the frequency range of 3.3 – 3.5 GHz and in other applications like fixed satellite services, maritime mobile services etc. covering 2 - 4 GHz of S-band frequency spectra. It is experimental observed that by placing stubs on the patch with air filled dielectric medium, the resonant frequency of the antenna can be lowered by a considerable amount resulting in compactness. Proposed antenna can be used as a compact antenna system where limited size is a requirement. Measurement results showed the satisfactory performance over S-band frequency spectra with the improved antenna parameters. Details of the antenna design procedure and results are discussed and presented.*

## *KEYWORDS*

*Co-axially fed, slots, WiMax, frequency, fixed satellite services.*

## I. INTRODUCTION

Wireless applications have undergone quick progress in recent years. One such particular wireless application that has experienced this trend is WiMax. According to the guideline by Telecom Regulatory Authority of India (TRAI) – Draft Recommendation on Growth of Broadband [1] on the provision of WiMax service, the allocated spectrum band in India is 3.3 - 3.5 GHz. The proposed antenna operates in the frequency range of 3.3 – 3.5 GHz and is useful in WiMax application.

WiMax antenna requires low profile, light weight and broad bandwidth with moderate gain. The microstrip antenna suits these features very well except for its narrow bandwidth. The conventional microstrip antenna couldn't fulfill these requirements as its bandwidth usually ranges from 1 - 2 % [2]. Although the required operating frequency range is from 3.3 – 3.5 GHz, atleast double the bandwidth is required to avoid the expensive tuning operation and not to cause any uncritical during manufacturing. Therefore, there is a need to enhance the bandwidth, gain and to achieve compactness for applications mentioned above.

In the early studies conducted and surveyed, a compact circular microstrip patch antenna with a switchable circular polarization (CP) is designed for 2.4 GHz, the impedance bandwidth and CP bandwidth of the antenna are up to 150 MHz and 35 MHz [3] respectively. The stacked rectangular microstrip antenna (SRMSA) using a co-axial probe feed method achieved a bandwidth of 1.63 % by embedding T-slots in the lower patch of the SRMSA [4]. A design of a coplanar waveguide (CPW) feed square microstrip antenna with circular polarization (CP) is described in [5] and has achieved 2.4% bandwidth. A compact single layer monopulse microstrip patch antenna array [6] for the application of monopulse radar has been designed, manufactured and tested and the design achieved a bandwidth of 5.6%. A novel, low profile compact microstrip antenna which achieved gain of - 4 dBi and bandwidth of 30 MHz is presented in [7]. A planar compact inverted U-shaped patch antenna with high-gain operation for Wi-Fi system has been proposed and investigated and provided relatively wider impedance bandwidth of 162 MHz covering the 2.45 GHz band (2400–2484 MHz) [8]. A dual-resonant patch antenna applicable to active radio frequency identification (RFID) tags is designed. The measurement results reveal that the antenna has the return loss less than –10 dB within the bandwidth of 42 MHz (from 911 to 953 MHz), which totally covers the 5 MHz bandwidth from 920

to 925 MHz [9]. A V-shaped microstrip patch antenna for 2.4 GHz is designed, fabricated, and experimentally measured and this design provided 50 MHz impedance bandwidth determined from 10 dB return loss for 2.4 GHz frequency band [10]. This paper examines a study of novel design of patch for improving the impedance bandwidth, gain and achieving compactness of the microstrip patch antenna on FR4 material for S-band frequency spectra applications.

## II. ANTENNA DESIGN AND PATCH STRUCTURE

Figure.1 depicts the front view of the designed antenna. A FR4 dielectric superstrate having dielectric permittivity $\epsilon_r$ = 4.4 having thickness $h$ = 1.66 mm with air filled dielectric substrate $\epsilon_o \approx 1$ of thickness $\Delta$ = 8.5 mm is sandwiched between the superstrate and ground plane. A copper plate with the dimension $L_g$ = $W_g$ = 40 mm with thickness of $h_1$ = 1.6 mm is used as a ground plane. The fabricated patch and the ground plane were fixed firmly together with plastic spacers along the four corners of the antenna. The geometry of the patch antenna 1 and 2 (PA 1 and PA 2) is as shown in figure 2 (a) and (b). The patch dimensions are, width $W$ = 23.28 mm and length $L$ = 17.76 mm. Stubs are placed on the patch with dimensions $c$ = 2 mm, $d$ = 1 mm, $e$ = 2 mm, $f$ = 1 mm, $g$ = 2 mm, $h$ = 2 mm, $i$ = 1 mm, $j$ = 2 mm, $k$ = 1 mm, $l$ = 1 mm so as to obtain the improvement in bandwidth, gain and to achieve compactness. The patch along with stub dimensions are taken in terms $\lambda_{0,}$ where $\lambda_0$ is the operating wavelength. The patch antenna incorporated with the short stub along the radiating and non radiating edges introduces a capacitance that suppresses some of the inductance introduced by the feed due to the thick substrate, and a resonance of stub can be obtained. In this work, co-axial or probe feed method is used as its main advantage is that, the feed pin can be placed at any place on the patch to have impedance match with its input impedance (50 ohms) and hence the feed pin is placed along the center line of Y-axis at a distance $f_p$ from the top edge of the patch as shown in Figure. 1.

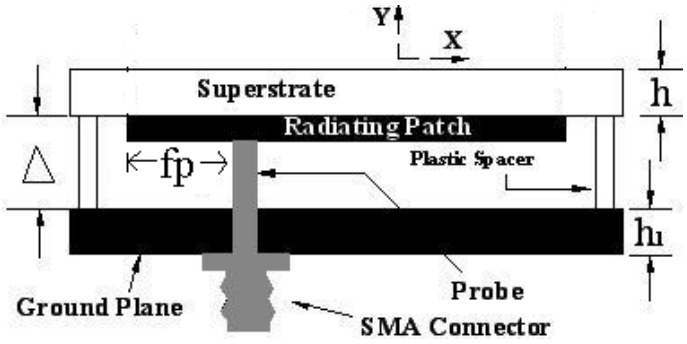
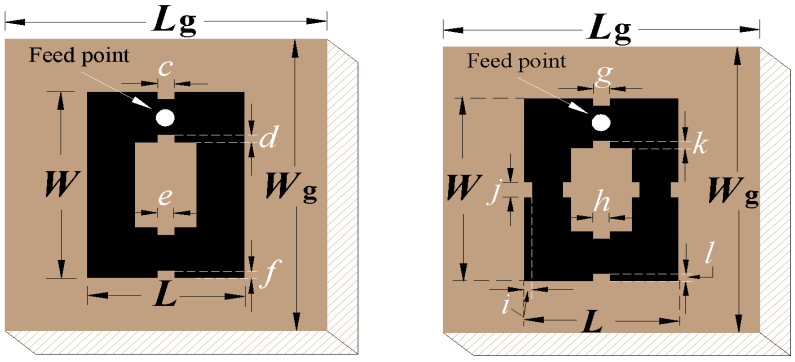



Figure 1. Front view of the designed antenna




(a) (b)

Figure 2. Patch structure. a) PA 1 and b) PA 2

## III. RESULTS AND DISCUSSION

The designed patch antennas have been experimentally studied using Vector Network Analyzer (Rohde and Schwarz, Germany make ZVK model 1127.8651). Figure 3 shows the measured return loss (RL) versus frequency characteristics for PA 1 and PA 2 at their respective resonant frequencies. Plot result shows that patch antenna (PA 1) resonates at 3.63 GHz with the total available impedance bandwidth 210 MHz that is 5.77 % covering the frequency range 3.53 GHz to 3.74 GHz and 250 MHz (7.02 %) impedance bandwidth resonating at 3.57 GHz covering 3.43 GHz to 3.68 GHz of S-band for patch antenna 2 (PA 2). It is also noted that minimum of -12.80 dB and -13.34 dB return loss is available at respective resonant frequencies for PA 1 and PA 2. Hence, the resonating frequencies are significantly lowered due to the use of stubs on the patch in comparison to the designed frequency 3.85 GHz for the simple microstrip patch antenna. The designed antennas also achieved a compactness of 11 % and 15 % for PA 1 and PA 2. A gain of 2.75 dB and 3.60 dB at resonant frequencies of 3.63 GHz and 3.57 GHz for PA 1 and PA 2 is also significant.

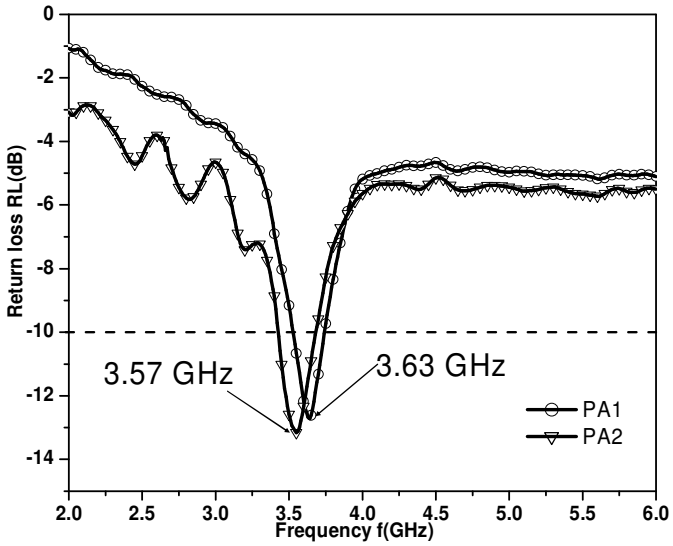
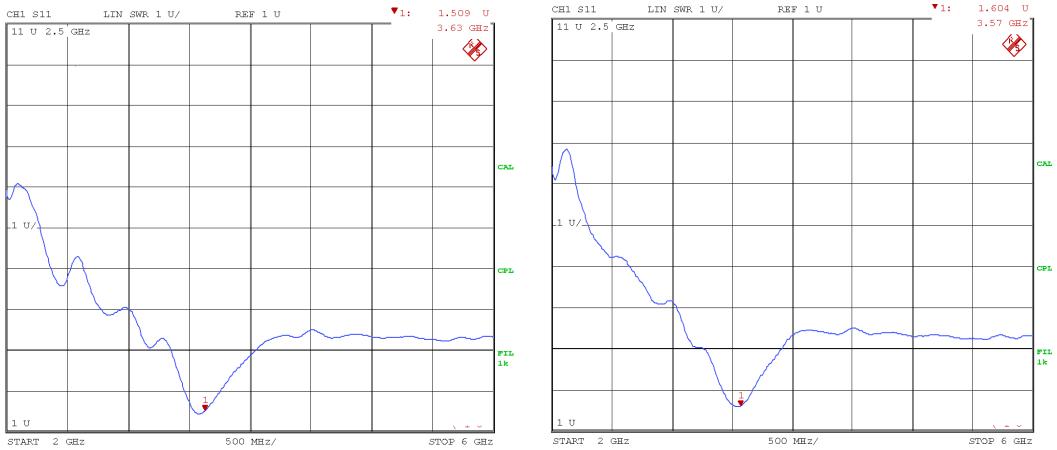



Figure 3. Measured return loss (RL) versus frequency (f) characteristics

The voltage standing wave ratio (VSWR) is a measure of impedance mismatch between the transmission line and its load. Figure 4 shows the VSWR characteristics of the designed antennas (PA 1 and PA 2) showing the values 1.509 and 1.604 that are less than 2 also justifying less reflected power at the respective resonant frequencies 3.63 GHz and 3.57 GHz.




(a) (b)

Figure 4. VSWR characteristics. a) PA 1 and b) PA 2

The radiation patterns of the designed antennas at the resonant frequencies are also measured and plotted. For the measurement of radiation pattern, the antenna under test (AUT), i.e., the designed antennas and standard pyramidal horn antenna are kept in the far field region. The AUT, which is the receiving antenna, is kept in phase with respect to transmitting pyramidal horn antenna. The received power by AUT is measured from $0^o$ to $180^o$ with the rotational motion at steps of $10^o$ each. Notably, it is seen that the antennas display good omni-directional radiation patterns at resonating frequencies as shown in Figure 5.

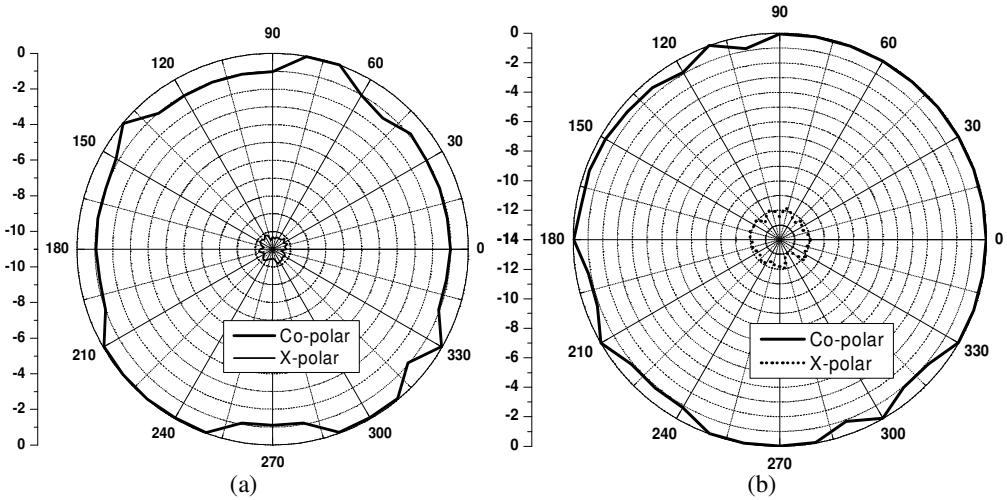



Figure 5. Measured radiation patterns. a) PA 1 and b) PA 2

# IV. CONCLUSION

The study has demonstrated that, the designed antennas having air filled substrate, patch with stubs achieved compactness of about 11 % and 15 % with 210 MHz and 250 MHz impedance bandwidth. It is also found that the designed microstrip patch antennas (PA 1 and PA 2) attained a gain of 2.75 dB and 3.60 dB at resonating frequencies with omni directional radiation patterns that can be suitably used for WiMax services, as it utilizes the 3.3 – 3.5 GHz band and also it can be used for applications like fixed satellite services, maritime mobile services etc covering 2 - 4 GHz for S-band frequency.

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# REDUCING TO FAULT ERRORS IN COMMUNICATION CHANNELS SYSTEMS

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***ABSTRACT***
*In this paper we introduce error-control techniques for improving the error-rate performance that is delivered to an application in situations where the inherent error rate of a digital transmission system is unacceptable. The acceptability of a given level of bit error rate depends on the particular application. For examples, certain types of digital speech transmission are tolerant to fairly high bit error rates. Other types of applications such as electronic funds transfer require essentially error-free transmission. For example, FEC is used in the satellite and deep-space communications. A recent application is in audio CD recordings where FEC is used to provide tremendous robustness to errors so that clear sound reproduction is possible even in the presence of smudges and scratches on the disk surface.*

***KEYWORDS****: ARQ, FEC, Detection System, Parity check code.*

## I. INTRODUCTION

In most of the communication channels a certain level of noise and interface is unavoidable. With the advent of digital systems, transmission has been optimized. However, bit errors in transmission will occur with some small but nonzero probability. For example, typical bit error rates for systems that use copper wires are in the order of $10^{-6}$ i.e. one in a million. Modern optical fiber systems have bit error rates of $10^{-9}$ or less. In contrast, [3] wireless transmission systems can experience error rate as high as $10^{-3}$ or worse. There are two basic approaches to error control. The first approach involves the detection of errors and an automatic retransmission request (ARQ) when errors are detected. This approach presupposes the availability of a return channel over which the retransmission request can be made. For example, ARQ is widely used in computer communication systems that use telephones lines. The seconds approach, forward error correction (FEC)[1][5], involves the detection of errors followed by processing that attempts to correct the errors. FEC is appropriate when a return channel is not available, retransmission requests are not easily accommodated, or a large amount of data is sent and retransmission to correct a few errors is very inefficient. Error detection is the first step in both ARQ and FEC. The difference between ARQ and FEC is that ARQ wastes the bandwidth by using retransmission, whereas FEC requires additional redundancy in the transmitted information and incurs significant processing complexity in performing the error correction.

## II. DETECTION SYSTEM TECHNIQUES

Here, the idea of error detection has been discussed by using the single parity check code as an example throughout the discussion. As illustrated in Figure 1.1, the basic idea in performing error detection is very simple. The information produced by an application is encoded so that the stream that is input the communication channel satisfies a specific pattern or condition [2][7]. The receiver checks the stream coming out of communication channel to see whether the pattern is satisfied or not. If it is not, the receiver can be certain that an error has occurred and therefore sets an alarm to alert the user. This certainty stems from the fact that no such pattern would have been transmitted by the encoder.

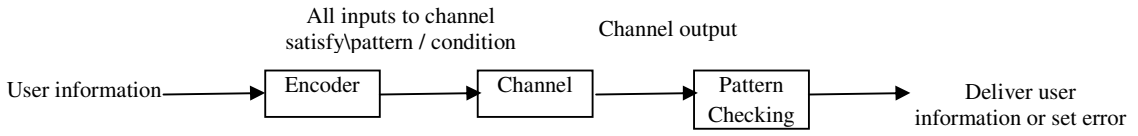



Figure 1.1 General error-detection systems

The simplest code is the single party check code that takes k information bits and appends a single check bit to form a codeword. The parity check ensures that total number of 1's in the codeword is even; that is, the codeword has even party. The check bit in this case is called a parity bit. This error detection is used in ASCII where characters are represented by seven bits and the eighth bit consists of a parity bit. This code is an example of the so-called linear codes because the parity bit is calculated as the modulo 2 sum of the information bits:

$$b_{k+1} = b_1 + b_2 + \cdots + b_k \qquad modulo\ 1$$

Where $b_1, b_2, \ldots, b_k$ are the information bits.

Recall that in modulo 1 arithmetic $0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1$ and $1 + 1 = 0$. Thus, if the information bits contain an even number of 1s, then the parity bit will be 0; and if they contain an old number, then the parity bit will be 1. Consequently, the above rule will assign the parity bit a value that will produce a codeword that always contains an even number of 1s.

## 2.1 Single Parity Check Code

This pattern defines the single parity check code. If a codeword undergoes a single error during transmission, then the corresponding binary block at the output of the channel will contain an odd number of 1s and the error will be detected. More generally, if the codeword undergoes an odd number of errors, the corresponding output block will also contain an odd number of 1s. Therefore, the single parity bit allows us to detect all error patterns that introduce an odd number of errors. On the other hand, the single parity bit will fail to detect any error patterns that introduce an even number of errors, since the resulting binary vector will have even parity. Nonetheless, the single parity bit provides a remarkable amount of error-detection capability, since the addition of a single check bit results in making half of all possible error patterns detectable, regardless of the value of k. Figure 1.2 shows an alternative way of looking at the operation of this example. [6][4] At the transmitter a checksum is calculated from the information bits and transmitted along with the information. At the receiver, the checksum is recalculated, based on the received information. The received and recalculated checksums are compared, and the error alarm is set if they disagree.

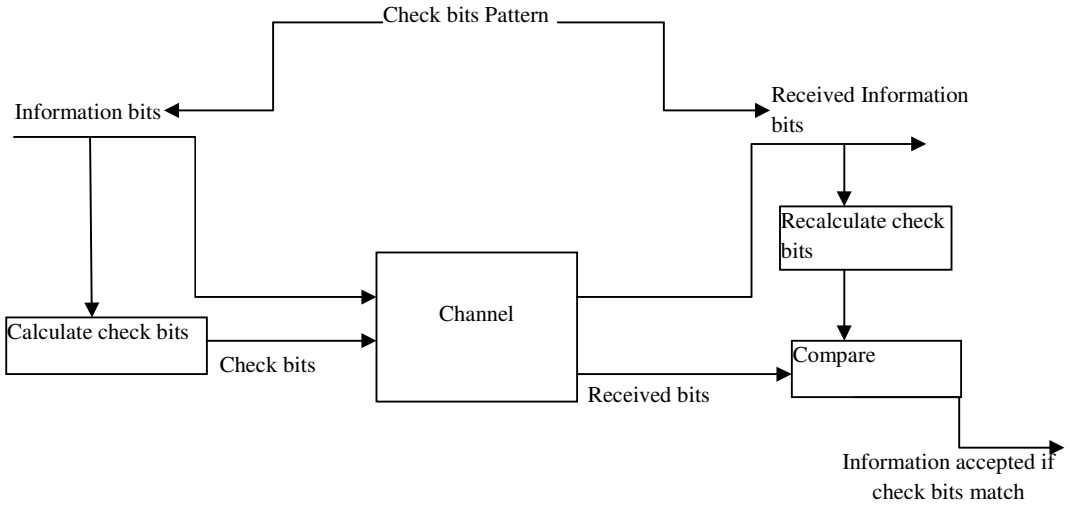
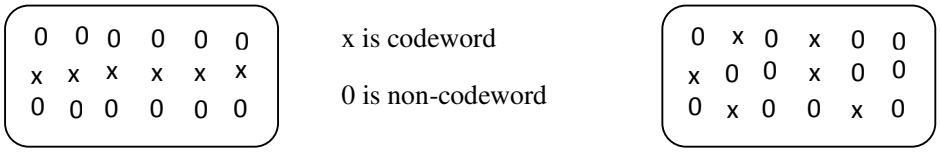



Figure 1.2 Error-detection system using check bits

This simple example can be used to present two fundamental observations about error detection. The first observation is that error detection requires redundancy in that the amount of information that is transmitted is over and above the required minimum. For a single parity check code of length $k+1$, $k$ bits are information bits, and one bit is the parity bit. Therefore, the fraction $1/(k+1)$ of the transmitted bits is redundant.

The second fundamental observation is that every error-detection technique will fail to detect some errors. In particular, an error-detection technique will always fail to detect transmission errors that convert a valid codeword into another valid codeword. For the single parity check code, an even number of transmission errors will always convert a valid codeword to another valid codeword.

The objective in selecting an error-detection code is to select the codeword that reduce the likelihood of the transmission channel converting one valid codeword into another [8]. To visualize how this is done, suppose we depict the set of all possible binary block as the space shown in Figure 1.3, with code words shown by $xs$ in the space and noncodewords by $os$. To minimize the probability of error-detection failure, we want the code words to be selected so that they are spaced as far away from each other as possible. Thus the code in Figure 1.3a is a poor code because the code words are close to each other. On the hand, the code in Figure 1.3b is good because the distance between code words is maximized. The effectiveness of a code clearly depends on the types of error that are introduced by the channel. We next consider how the effectiveness is evaluated for the example of the single parity check code.




(a). A code with poor distance properties (b). A code with good distance properties

Figure 1.3 Distance properties of codes

## 2.2 Effectiveness of Error-Detection Codes

The effectiveness of an error-detection code is measured by the probability that the system fails to detect an error. To calculate this probability of error-detection failure, we need to know the probabilities with which various errors occur. These probabilities depends on the particular properties of the given communication channel. We will consider three models of error channels [18]; the random error vector model, the random bit error model, and burst errors.

Suppose us transmission a codeword that has n bits. Defines the error vector $\vec{e} = (e_1, e_2, \ldots, e_n)$ where $e_i = 1$ if an error occurs in the $i$th transmitted bit and $e_i = 0$ otherwise. In one extreme case, the random error vector model, all $2^n$ possible error vectors are equally likely to occur. In this channel model the probability of $\vec{e}$ does not depend on the number of errors it contains. Thus the error vector (1, 0, …, 0) has the same probability of occurrence as the error vector (1, 1, … , 1). The single parity check code will fail when the error vector has an even number of 1s. Thus for the random error vector channel model, the probability of error detection failure is 1/2.

Now consider the random bit error model where the bit errors occur independently of each other. Satellite communication provides an example of this type of channel [9][10]. Let p be the probability of an error in a single-bit transmission. The probability of an error vector that has $j$ errors is $p^j(1-p)^{n-j}$, since each of the $j$ errors occurs with probability $p$ and each of the $n-j$ correct transmissions occurs with probability$1-p$. By rewriting this probability we obtain:

$$p[\vec{e}] = (1-p)^{n-w(\vec{e})}p^{w(\vec{e})} = (1-p)^n\left(\frac{p}{1-p}\right)^{w(g)} \quad (1)$$

Where the weight $w(\overrightarrow{e})$ is defined as the number of 1s in $\overrightarrow{e}$ . For any useful communication channel. The probability of bit error is much smaller than 1, and so $p < \frac{1}{2}$ $and$ $\left(\frac{p}{1-p}\right) < 1$. This implies that

for the random bit error channel the probability of $\vec{e}$ decreases as the number of errors (1s) increases; that is, an error pattern with a given number of bit errors is more likely than an error pattern with a large number of bit errors. Therefore this channel tends to map a transmitted codeword into binary blocks that are clustered around the codeword.

The single parity check code will fail if the error pattern has an even number of 1s. therefore, in the random bit error model:

$$p[error\ detection\ failure] = p[undetectable\ error\ pattern]$$

$$= p[error\ patterns\ with\ even\ number\ of\ 1s] \quad (2)$$

$$= \binom{n}{2}p^2(1-p)^{n-2} + \binom{n}{4}p^4(1-p)^{n-4} + \ \ldots$$

where the number of terms in the sum extends up to the maximum possible even number of errors. In the preceding equation we have used the fact that the number of distinct binary $n-tuples$ with $j$ ones and $n-j$ zeros is given by

$$\binom{n}{j} = \frac{n!}{j!\,(n-j!)}$$

In any useful communication system, the probability of a single-bit error p is much smaller than 1. We can then use the following approximation:

$$p^i(1-p)^i \approx p^i(1-pj) \approx p^i.$$

For example, if $p = 10^{-3}$ then $p^2(1-p)^{n-2} \approx 10^{-6}\ and\ p^4(1-p)^{n-4} \approx 10^{-12}$. Thus the probability of detection failure is determined by the first term in equation 4. For example, suppose $n = 32\ and\ p = 10^{-4}$. Then the probability of error detection failure is $5 \times 10^{-6}$ a reduction of nearly two orders of magnitude.

We have observed that a wide gap exists in the performance achieved by the two preceding channel models. Many communication channels combine aspects of these two channels in that errors occur in bursts. Period of low error rate transmission are interspersed with periods in which clusters of error occur. The periods of low error rate are similar to the random bit error model, and the periods of error burst are similar to the random error vector model, the probability of error-detection failure for the single parity check code will be between those of the two channel models. In general, measurement studies are required to characterize the statistics of the burst occurrence in specific channels.

## III. TWO-DIMENSIONAL PARITY CHECKS

A simple method to improve the error-detection capability of a single parity check code is to arrange the information bits in columns of *k* bits, as shown in Figure1.4. The last bit in each column is the check bit for the information bits in the column. [11][13] Note that in effect the last column is a "check codeword" over the previous *m* columns. The right-most bit in each row is the check bit of the other bits in the row. The resulting encoded matrix of bits satisfies the pattern that all rows have even parity and all columns have even parity. If one, two, or three errors occur anywhere in the matrix of bits during transmission, then at least one row or parity check will fail, as shown in Figure 1.5. However, some patterns with four errors are not detectable, as shown in figure. The two-dimensional parity check code is another example of a liner code. It has the property that error-detecting capabilities can be identified visually, but it does not have particularly good performance.

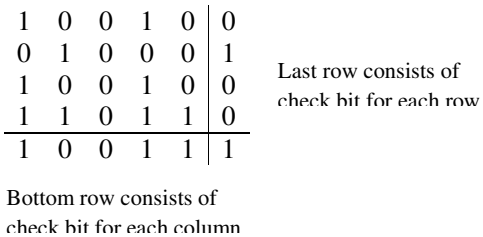



Figure 1.4 Two –dimensional parity check code

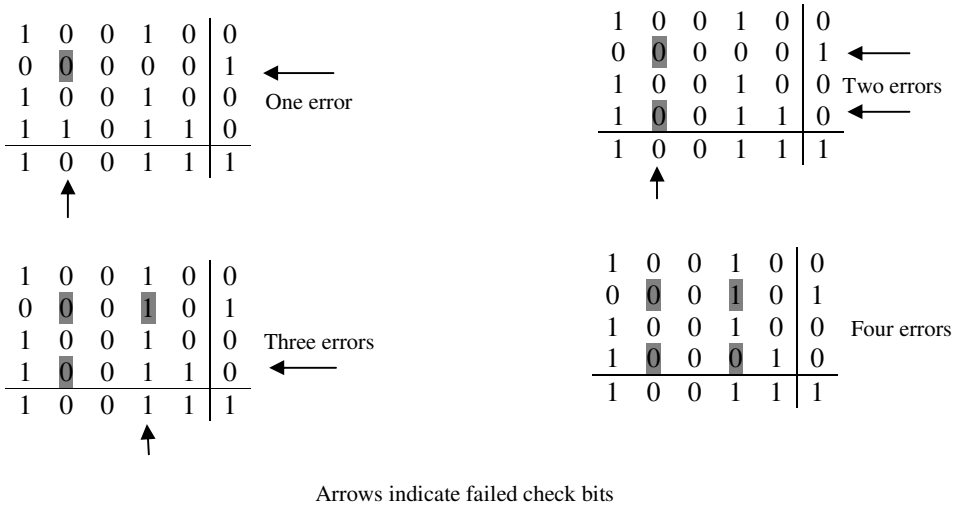



Figure 1.5 Detectable and undetectable error patterns for two-dimensional code

## IV. PERFORMANCE OF LINEAR CODES

In figure 1.3 we showed qualitatively that we can minimize the probability of error detection failure by spacing code words apart in the sense that it is unlikely for errors to convert one codeword into another. In this paper we show that the error-detection performance of a code is determine by the distances between code-words. The Hamming distance $d(\underline{b_1}, \underline{b_2})$ between the binary vectors $\underline{b_1}$ and $\underline{b_2}$ is defined as the number of components in which they differ. Thus the Hamming distance between two vectors increases as the number of bits in which they differ increases. Consider the modulo 2 sum of two binary $n-tuples$ $\underline{b_1} + \underline{b_2}$. The components of this sum will equal one when the corresponding components in $\underline{b_1}$ and $\underline{b_2}$ differ, and they will be zero otherwise [14],[15]. Clearly this result is equal to the number of 1s in $\underline{b_1} + \underline{b_2}$, so

$$d\left(\underline{b_1}, \underline{b_2}\right) = w(\underline{b_1} + \underline{b_2}) \qquad (3)$$

where w is the weight function introduced earlier. The extent to which error vectors with few errors are more likely than error vectors with many errors suggests that we should design linear codes that have code words that are far apart in the sense of Hamming distance.

Define the minimum distance $d_{mn}$ of a code as follows

$$d_{mn} = distance\ between\ two\ closest\ distinct\ codewords$$

For any given linear code [16], [17], the pair of closest codewords is the most vulnerable to transmission error, so $d_{mn}$ can be used as a worst-case type of measure. Form equation 9 we have that if $\underline{b_1}$ and $\underline{b_2}$

Is also a codeword. To find $d_{mn}$, we need to find the pair of distance codewords $\underline{b_1}$ and $\underline{b_2}$ that minimize$d(\underline{b_1}, \underline{b_2})$. By equation 10, this is equivalent to finding the nonzero codeword with the smallest weight. Thus

$$d_{mn} = weight\ fo\ the\ nonzero\ codeword\ with\ the\ smallest\ number\ of\ 1s$$

From Table 1.1, we see the Hamming (7,4) code has $d_{mn} = 3$.

| Information | | | | Codeword | | | | | | | weight |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | $w(\underline{b})$ |
| **0** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **0** | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 4 |
| **0** | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 3 |
| **0** | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 3 |
| **0** | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 3 |
| **0** | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 3 |
| **0** | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 4 |
| **0** | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 4 |
| **1** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 3 |
| **1** | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 3 |
| **1** | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 4 |
| **1** | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 4 |
| **1** | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 4 |
| **1** | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 4 |
| **1** | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 3 |
| **1** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7 |

Table 1.1 Hamming (7, 4) code

If we start changing, the bits in a codeword one at a time until another codeword is obtained, then we will need to change at least $d_{mn}$ bits before we obtain another codeword. This situation implies that all error vectors with $d_{min} - 1$ or fewer errors are detectable. We say that a code is $t - error$ detecting if

$$d_{min} \geq t + 1.$$

Finally, let us consider the probability of error-detecting failure for general linear code. In the case of the random error vector channel model, all $2^n$ possible error patterns are equally probable. A linear $(n, k)$ code fails to datect only the $2^k - 1$ error vectors that correspond to nonzero codewords. We can state then that the probability of error-detection failure for the random error vector channle model is

$\frac{2^k-1}{2^n} \approx 1/2^{n-k}$. [6][12] Furthermore, we can decrease the probability of detection failure by increasing the number of parity bits $n - k$. Consider now the random bit error channel model. The probability of detection failure is given by

$$p[detection\ failure] = p[\underline{e}\ is\ a\ nonzero\ codeword]$$

$$= \sum_{nonzero\ codewords\ \underline{b}} (1-p)^{n-w(\underline{b})} p^{w(\underline{b})}$$

$$= \sum_{w=d_{min}}^{d_{max}} N_w (1-p)^{n-w} p^w$$

$$\approx N_{d_{min}} p^{d_{min}} \; for \; p \ll 1$$

The second summation adds the probability of all nonzero code words. The third summation combines all code words of the same weight. So $N_w$ is the total number of codewords that have weight $w$. The approximation results from the fact that the summation is dominated by the leading term when $p$ is very small. Consider the $(7,4)$ Hamming code as an example once again. For the random error vector model, the probability of error-detection failure is $\frac{1}{2^3} = \frac{1}{8}$. On the other hand, for the random bit error channel the probabiltity of error-detection failure is approximation $7p^3$, since $d_{min} = 3$ and seven codewords have this weight. If $p = 10^{-4}$, then the probabiltiy of error detection failure is $7 \times 10^{-12}$. Compared to the single parity check code, the Hamming code yields a tremendous improvement in error-detection capability.

## V. RESULTS AND DISCUSSION

This paper has proposed coding techniques that are applicable in error control for improving the error-rate performance. The effectiveness of an error-detection code observed that a wide gap in terms of errors occur in bursts by the two preceding channel models. Then performance of linear codes are extent to which error vectors with few errors are more likely than error vectors with many errors that should design linear codes that apart in the sense of Hamming distance.

## VI. CONCLUSION

Result shows that a wide gap exists in the performance achieved by the two preceding channel models. Many communication channels combine aspects of these two channels in that errors occur in bursts. Period of low error rate transmission are interspersed with periods in which clusters of error occur. The effectiveness of an error-detection code is measured by the probability that the system fails to detect an error. To calculate this probability of error-detection failure, one needs to know the probabilities with which various errors occur. These probabilities depends on the particular properties of the given communication channel.

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# SPACE VECTOR BASED VARIABLE DELAY RANDOM PWM ALGORITHM FOR DIRECT TORQUE CONTROL OF INDUCTION MOTOR DRIVE FOR HARMONIC REDUCTION

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***ABSTRACT***

*The conventional SVPWM algorithm gives good performance for control of induction motor drive, but it produces more acoustical noise resulting in increased total harmonics distortion. The random pulse width modulation (RPWM) techniques has become an established means for mitigation of undesirable side effects in PWM converters, the use of voltage source inverters in adjustable speed ac drives in particular. Hence, to minimize these anomalies of the drive, this paper presents a novel variable delay random pulse width modulation (VDRPWM) algorithm with constant switching frequency for direct torque controlled induction motor drive. The Simplicity of this technique is its easy implementation and requires only low-end processors. The conventional VDRPWM preserves both the quality switching of the conventional space-vector PWM (SVPWM) method and minimized harmonic mitigation of the variable switching frequency PWM technique. To validate the proposed conventional VDRPWM algorithm for the considered drive, simulation studies have been carried out and results are presented. The simulation results confirmed the feasibility of proposed VDRPWM algorithm strategy in terms of acoustical noise and harmonic distortion as compared with conventional DTC and SVPWM based induction motor drive.*

***KEYWORDS:*** *Total Harmonic Distortion, sampling period, acoustic noise, SVPWM, constant switching times, Variable Delay Random Pulse Width Modulation (VDRPWM).*

## I. INTRODUCTION

Variable frequency AC drives are increasingly used for various industrial applications. The direct torque control (DTC) technique has been recognized as the viable solution to achieve the requirements of various industrial drives. Despite being simple, DTC is able to produce very fast torque and flux control and also robust with respect to drive parameters [1]-[2]. However, during steady state operation, a notable torque, flux and current pulsations will occur which are reflected in speed estimation and in increased acoustical noise. To overcome these anomalies and also for full utilization of dc bus, Space Vector PWM technique has been introduced [3]-[4]. Due to the improvement of fast-switching power semiconductor devices, voltage source inverters with pulse width- modulated (PWM) control growing interest which increases the performance of DTC drive Systems [5]-[6] . In recent years, the space vector PWM (SVPWM) algorithm is gaining importance by many researchers. In the SVPWM algorithm, the reference is given as a voltage space vector, which is sampled in every sub-cycle and an average voltage vector equal to the sampled reference is generated by different voltage vectors produced by the inverter. The SVPWM based PWM technique for inverter operated induction motor drive has major advantages compared to other techniques. It has lower current harmonics, a possible higher modulation index compared with sinusoidal modulation technique and ease of implementation. Though, the SVPWM algorithm has good performance, it produces acoustical noise and harmonic distortion due to its nature of pulse durations. To overcome the anomalies CSVPWM, the PWM controlled inverter is used which is operated at a constant

switching frequency. When the carrier frequency increases, the current harmonics shift to higher frequencies. As the PWM switching done at high frequencies higher harmonic distortion and switching noise will results. Among various PWM techniques, the random pulse width modulation (RPWM) techniques are attracted by many researchers for application to various drive systems. The principle of RPWM is that, either the position of the pulse or the switching frequency is varied randomly then the power spectrum of the output voltage acquires a continuous part, while the harmonic part is significantly reduced. The detailed review of the RPWM approach is given in [7]-[9]. However, a novel algorithm known as variable delay RPWM (VDRPWM) which is characterized by a constant switching frequency and a varying switching period (Ts) is gaining importance recently [10]-[11]. This paper presents a novel variable delay random PWM based direct torque controlled induction motor drive to reduce acoustical noise and harmonic distortion. The results of this drive are compared with that of the conventional DTC and SVPWM based induction motor drive.

## II. SPACE VECTOR PWM ALGORITHM

The three-phase, two-level voltage source inverter (VSI) has a quite simple design and generates a low-frequency output voltage with controlled amplitude and frequency by programming gating pulses at high-frequency. For a 3-phase, two-level VSI, there are eight possible voltage vectors, which can be represented in the space as shown in Fig. 1.

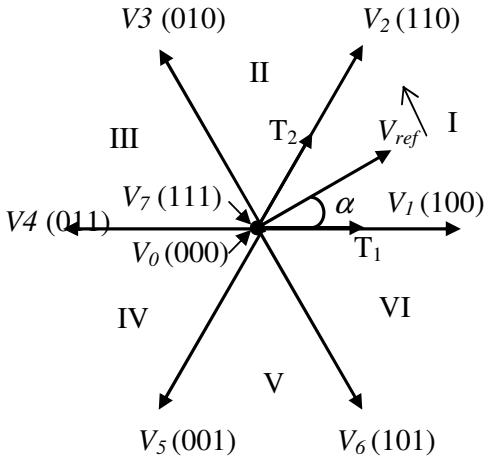


Fig 1 Possible voltage space vectors and sector definition

The voltage vectors $V_1$ and $V_7$ are known as zero voltage vectors or null vectors and the remaining voltage vectors $V_1$ to $V_6$ vectors are known as active voltage vectors or active states. The reference voltage space vector or sample as shown in Fig.1 represents the corresponding required value of the fundamental components for the output voltages. In the space vector algorithm this is constructed in an average sense. $V_{ref}$ is sampled at equal intervals of time, $T_s$ . Different voltage vectors that are produced will be applied over different time durations with in a sampling time period such that the average vector produced over the sampling time period is equal to the sampled value of the $V_{ref}$, both in terms of magnitude and angle. Any two active voltage vectors and one zero voltage vectors forming the boundary of the sector in which the sample lies be considered to generate reference sample vector. For the required reference voltage vector, the active and zero voltage vectors times are calculated as given in (1)-(3).

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i \sin(60^o - \alpha) T_s \quad (1)$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i \sin(\alpha) T_s \quad (2)$$

$$T_z = T_s - T_1 - T_2 \quad (3)$$

where $M_i$ is the modulation index and defined as $M_i = \pi V_{ref} / 2V_{dc}$ .

## III. PROPOSED VDRPWM ALGORITHM

A fixed sampling technique allows optimal use of the processor computational capability. Several papers by various researchers have investigated different methods for maintaining fixed sampling rate while introducing RPWM techniques [12]–[13]. In [13], three different fixed sampling rate techniques are illustrated, which maintains synchronous sample and PWM period but it suffers some form of limitation. Random zero vector and random centre displacement (RCD) has less effectiveness at high-modulation indexes. The Random lead–lag (RLL) does not offer a very good performance with respect to the reduction of acoustical noise and suffers in increased current ripple. In addition, RLL and RCD introduce an error in the fundamental component due to average value of the switching ripple. For the listed reasons, the variable-delay random pulse width modulation (VDRPWM) method was selected for this application.

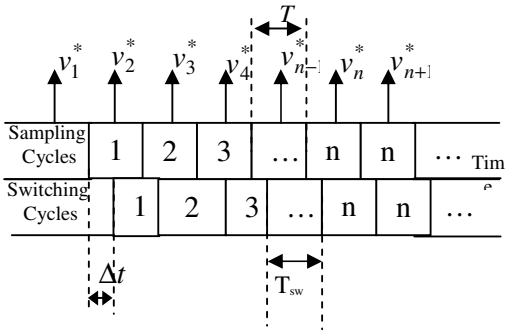


Fig 2 sampling and switching cycles in the proposed VDRPWM algorithm

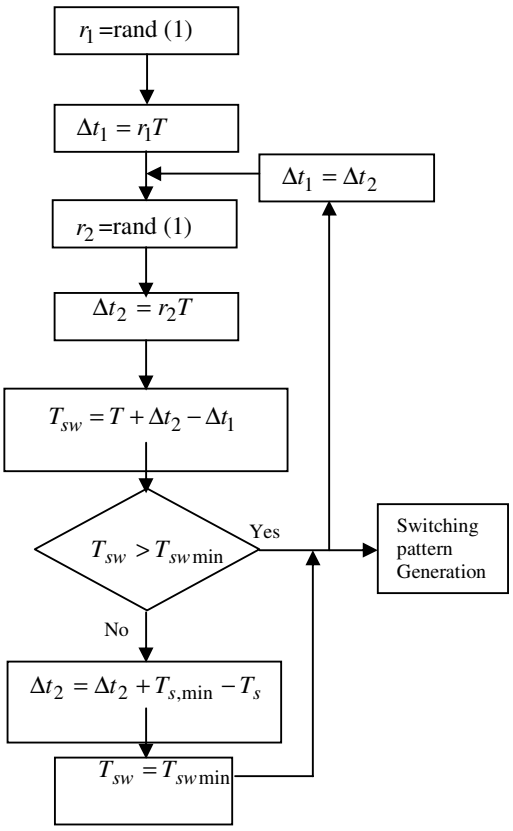


Fig 3 flowchart of proposed variable delay random PWM algorithm

The novel approach to dithering the switching periods, referred to as a variable-delay random pulse width modulation (VDRPWM) technique, is characterized by a constant sampling frequency. The Sampling and switching cycles in the VDRPWM technique is shown in figure 2. As described in the above figure, the individual switching periods are varied in a random manner by randomizing the switching cycle delays with respect to their corresponding sampling cycles. The random delay, $\Delta t$, can be varied with uniform distribution between zero and the sampling period, $\tau$[14]-[16]. The resulting switching period will turn out to be too short if a long delay in one sampling cycle is followed by a short delay in the next subsequent cycle, that is, shorter than its minimum allowable value $T_{sw}$ minimum. In such case, the switching period is set to that value which results the length of the switching cycle varies between $T_{sw}$ minimum and $2\tau$. A flow chart of the VDRPWM technique for control of induction motor drive is shown in Fig. 3 from which it is clear that, the number of switching cycles is same as that of sampling cycles, that is, the average switching frequency equals the fixed sampling frequency.

## IV. PROPOSED VDRPWM BASED DTC-IM DRIVE

The block diagram of the proposed VDRPWM algorithm based DTC is as shown in Fig. 4, from which it can be observed that this scheme retains all the advantages of the conventional direct torque control, such as no co-ordinate transformation and robust motor parameters.

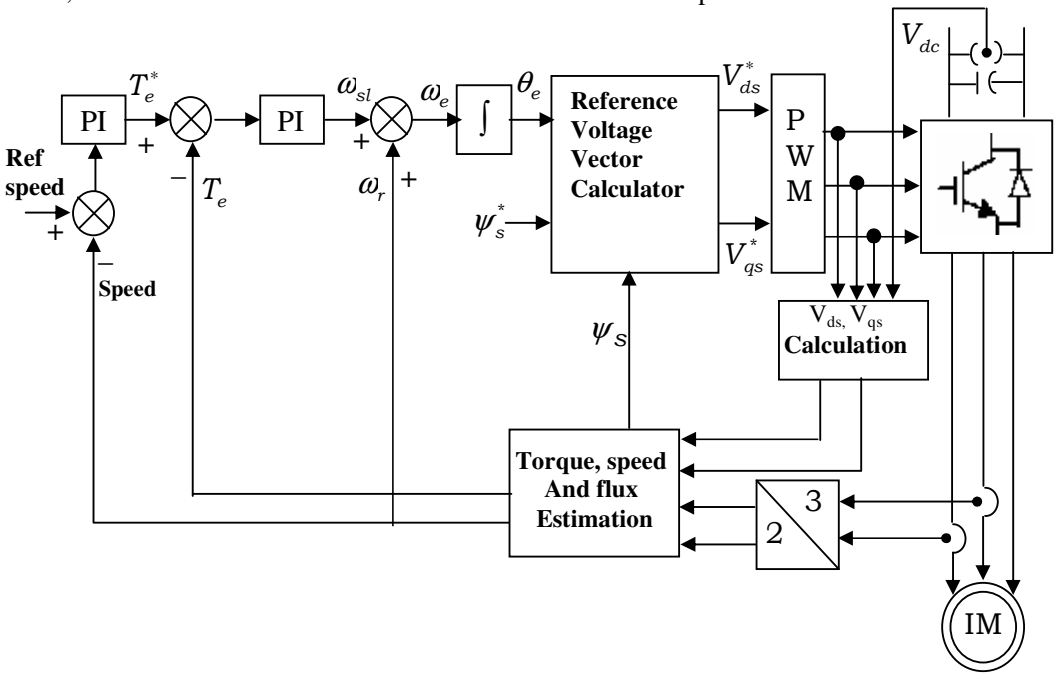


Fig 4 Block diagram of proposed VDRPWM based Direct Torque Control

However a PWM modulator is used to generate the pulses for the inverter control, therefore the complexity is increased in comparison with the CDTC method. In the proposed method, by adding the slip speed and actual rotor speed of the drive the position of the reference stator flux vector $\bar{\psi}_s^*$ is obtained and by using the flux estimator the actual synchronous speed of the stator flux vector $\bar{\psi}_s$ is evaluated. After each sampling interval, actual stator flux vector $\bar{\psi}_s$ is corrected by the error signal and it tries to reach the reference flux space vector $\bar{\psi}_s^*$. Thus the flux error is reduced in each sampling interval. The reference values of the d-axis and q-axis stator fluxes and actual values of the d-axis and q-axis stator fluxes are compared in the reference voltage vector calculator block and then the errors in the d-axis and q-axis stator flux vectors are obtained as in (4)-(5).

$$\Delta\psi_{ds} = \psi_{ds}^* - \psi_{ds} \tag{4}$$

$$\Delta\psi_{qs} = \psi_{qs}^* - \psi_{qs} \tag{5}$$

The knowledge of flux error is then can be used to get the appropriate reference voltages as in (6)–(7).

$$V_{ds}^{*} = R_s i_{ds} + \frac{\Delta \psi_{ds}}{T_s} \tag{6}$$

$$V_{qs}^{*} = R_s i_{qs} + \frac{\Delta \psi_{qs}}{T_s} \tag{7}$$

These derived d-q components of the reference voltage vectors are passed to the PWM block. In PWM block, these two-phase voltages are then converted into three-phase voltages. Later, the switching times are calculated as explained in the earlier sections for VDRPWM control.

## V. SIMULATION RESULTS AND DISCUSSION

To verify the proposed conventional VDRPWM based drive, simulation studies have been carried out on direct torque controlled induction motor drive by using MATLAB/SIMULINK. For the simulation analysis, the reference flux is considered as 1wb and starting torque is limited to 15 N-m. The induction motor used in this case study is a 3-phase, 4-pole, 1.5 kW, 1440 rpm and having the parameters as $R_s$ = 7.83Ω, $R_r$ = 7.55 Ω, $L_s$ = 0.4751H, $L_r$ = 0.4751H, $L_m$ = 0.4535 H and J = 0.06 Kg.m$^2$. The steady state results of conventional DTC and SVPWM algorithm based DTC are shown in Fig.5-Fig.10. From the results it is clear that SVPWM algorithm based drive gives superior performance and reduced harmonic distortion when compared with conventional DTC, but it gives considerable acoustical noise. Hence, to minimize the acoustical noise and THD of the drive, this paper presents conventional VDRPWM algorithm based control. The simulation results of VDRPWM algorithm based induction motor drive are shown in Fig. 11- Fig.16. From the simulation results, it is clear that the proposed VDRPWM algorithm gives reduced THD and less acoustical noise when compared with the SVPWM algorithm based drive.

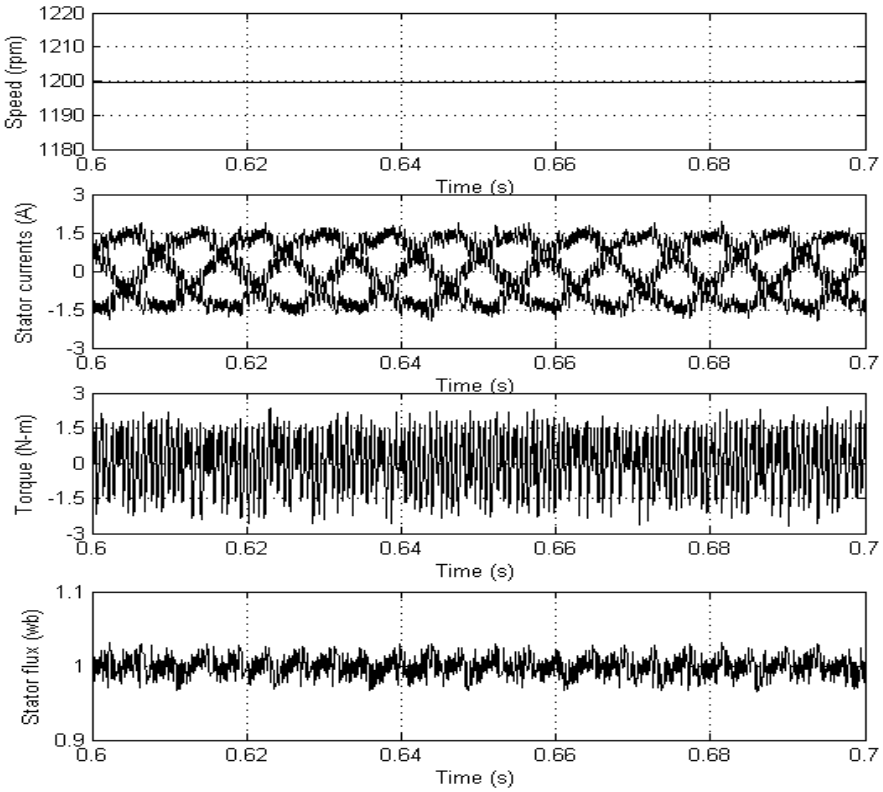


Fig 5 steady state plots of conventional DTC

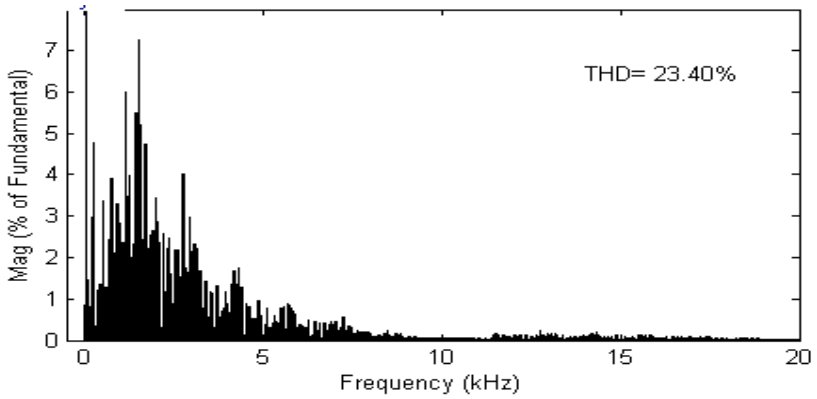


Fig 6 Harmonic spectra of line current in conventional DTC

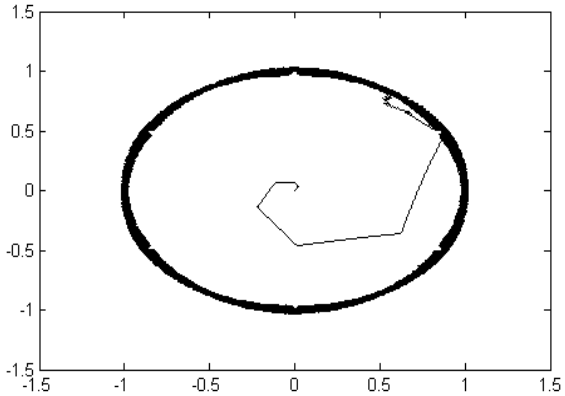

Fig 7 Locus of stator flux in conventional DTC drive

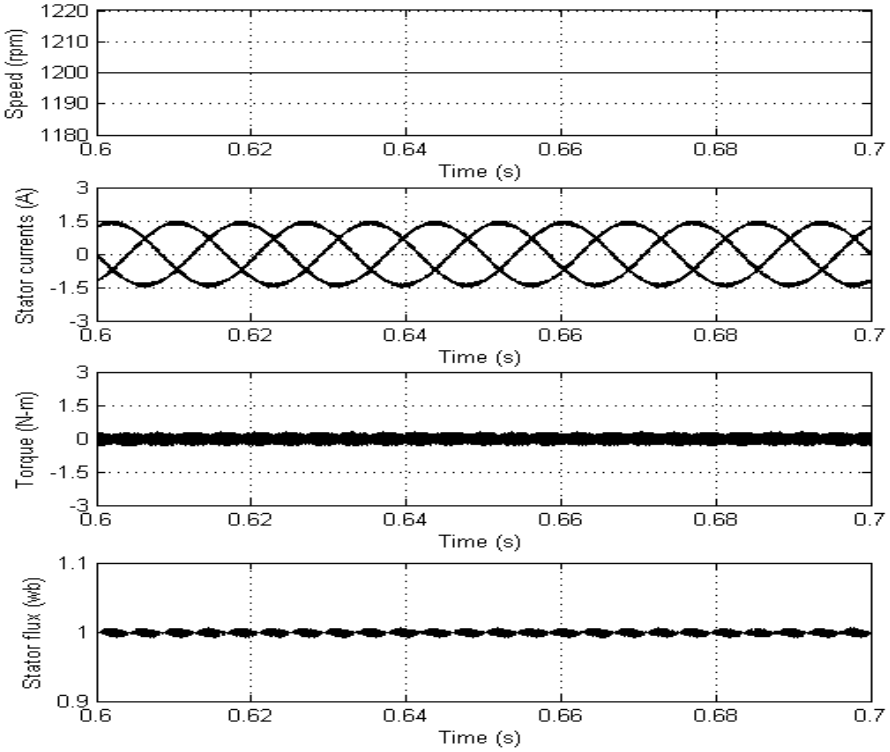


Fig 8 steady state plots of SVPWM algorithm based DTC

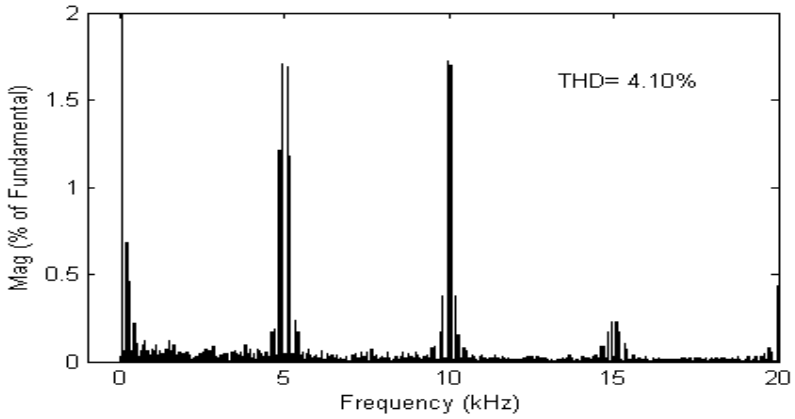


Fig 9 Harmonic spectra of line current in SVPWM based DTC drive

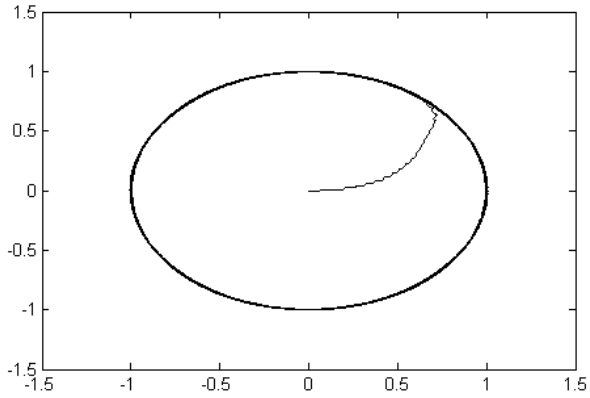

Fig 10 Locus of stator flux in SVPWM based DTC drive

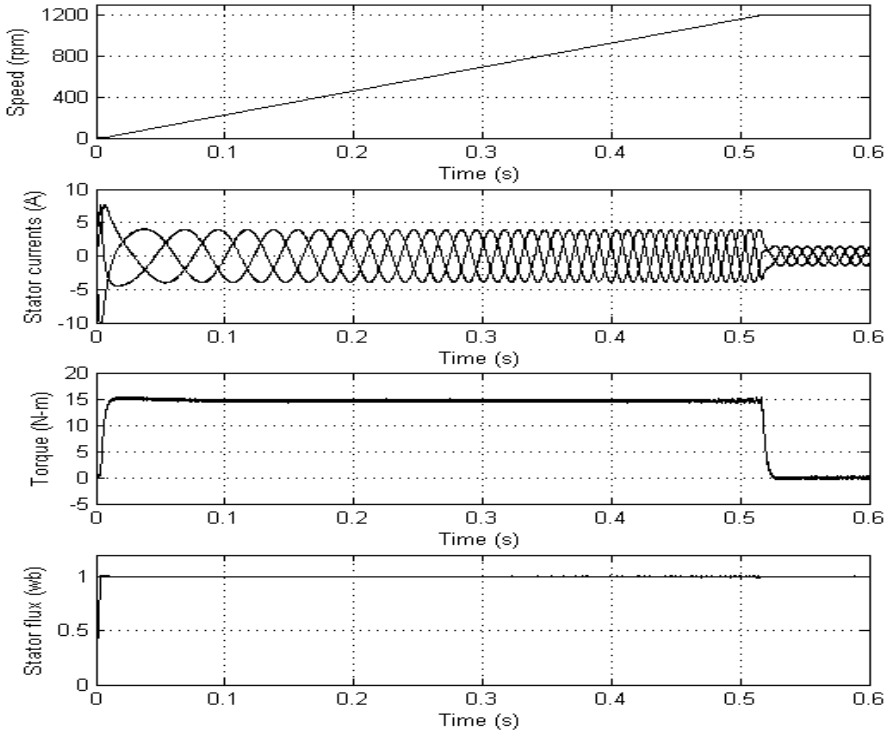


Fig 11 starting transients of proposed VDRPWM based DTC drive

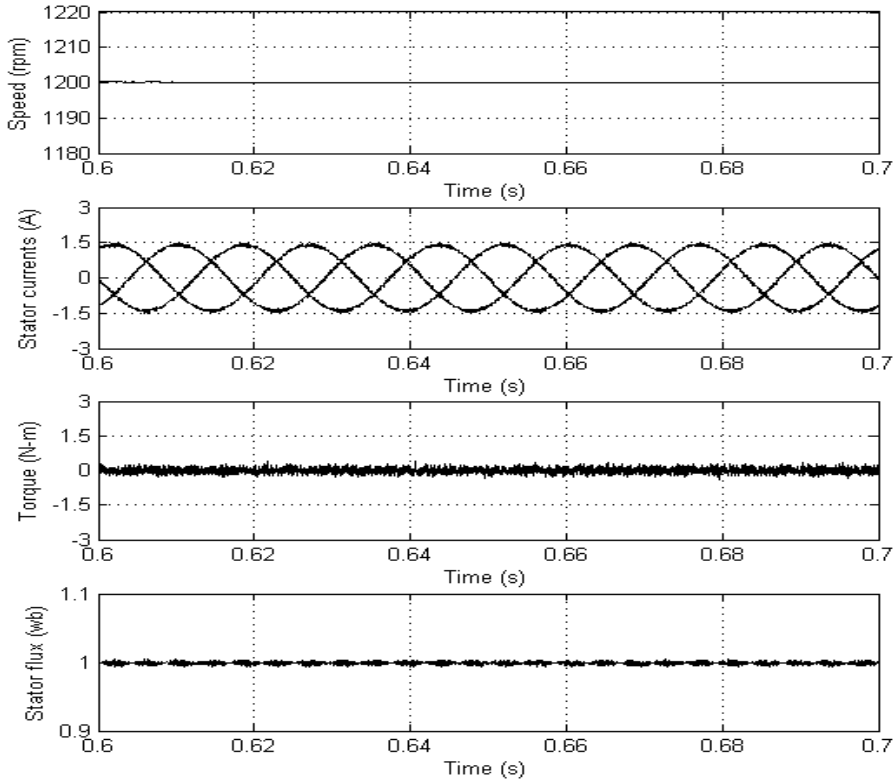


Fig 12 Steady state plots of proposed VDRPWM based DTC drive

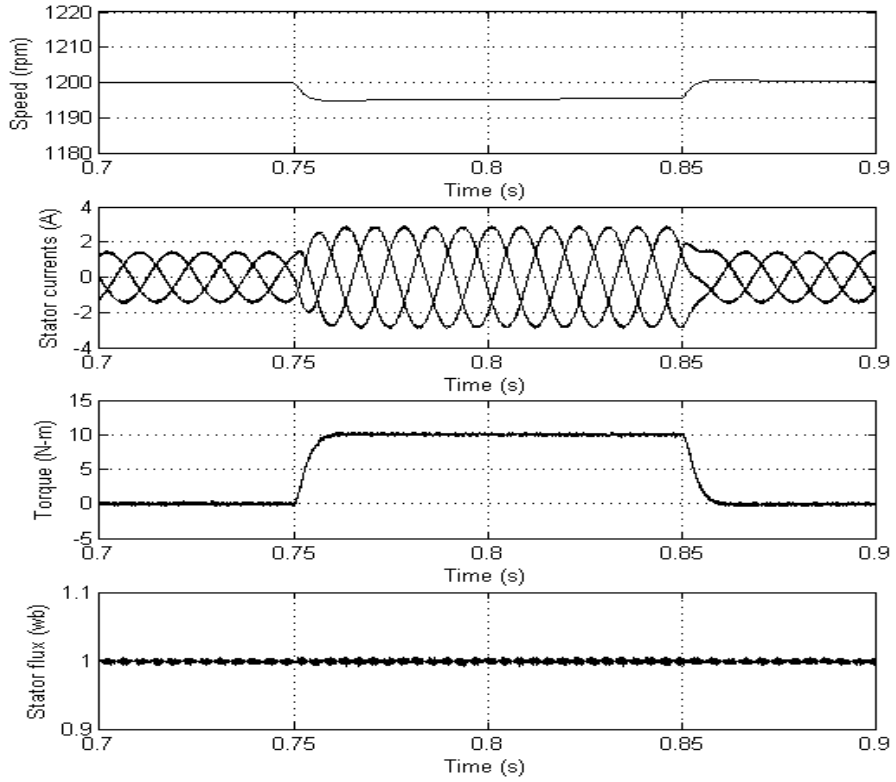


Fig 13 Transients during step change in load for proposed VDRPWM algorithm based DTC drive (a load torque of 10 N-m is applied at 0.75 s and removed at 0.85s)

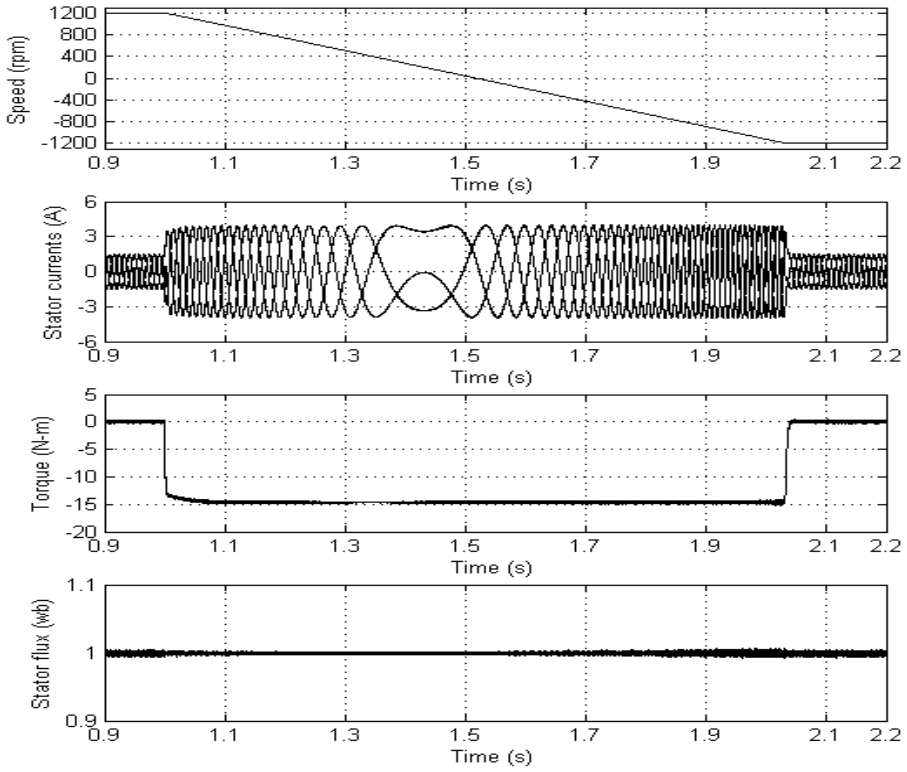


Fig. 14 Transients during speed reversal condition for proposed VDRPWM algorithm based DTC drive (speed changed from +1200 rpm to -1200 rpm)

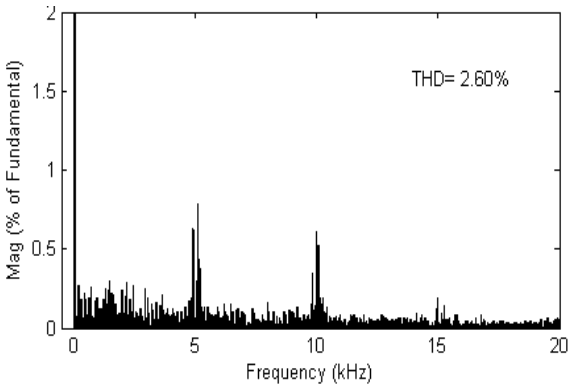


Fig 15 Harmonic spectra of line current in proposed VDRPWM based DTC drive

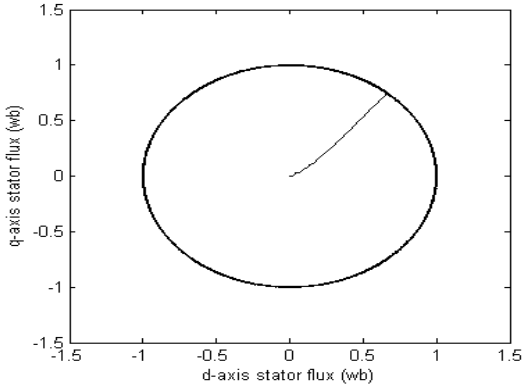


Fig 16 Locus of stator flux in proposed VDRPWM based DTC drive

## VI. CONCLUSION

To overcome the drawbacks of conventional DTC and SVPWM algorithm based drive, a novel VDRPWM algorithm is presented in this paper for direct torque control of induction motor. From the simulation results, it can be observed that the proposed VDRPWM algorithm gives reduced harmonic distortion. Hence, the proposed VDRPWM algorithm gives distributed spectra and gives reduced amplitude of harmonics when compared with the SVPWM algorithm. The simulation results confirm the superiority of proposed VDRPWM algorithm when compared with the SVPWM algorithm based DTC drive.

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His research areas include Gas Insulated Substations, High Voltage Engineering, Power Systems and Electrical Drives.

# SOFTWARE AGENT'S DECISION MAKING APPROACH BASED ON GAME THEORY

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***ABSTRACT***

*This paper highlights the use of software agent which is capable of perceiving its environment and performs its own operations without any other explicit instruction. The main objective of this paper is to investigate the possibility how to make the decision making capability of an Expert system more accurate and successful goal-oriented. This is done with the use of a utility measurement which is explained in a given example. It helps the agent to take a decision quicker so goal will be achieved.*

***KEYWORDS:*** *Software Agents, Game Theory, Expert System, Decision Making, Utility Value.*

## I. INTRODUCTION OF SOFTWARE AGENT

Software agents are autonomous pieces of software that conduct several tasks delegated to them. In the era of endless information flows, benefits can be achieved by authorizing certain kind of tasks to be done automatically by small independent software programs. Software agents are continuously running, personalized and semi-autonomous, and this makes them useful for a wide variety of information and process management tasks.

Numerous definitions exist for software agent and there is no single commonly accepted one. Some of them are: Software agent is a software entity that functions continuously and autonomously in a particular environment, which may contain another agents and processes. Intelligent agents continuously perform three functions as:

- Perception of dynamic conditions in the environment;
- Action to affect conditions in the environment; and
- Reasoning to interpret perceptions, solve problems, draw inferences, and determine actions

## II. SOFTWARE AGENT AND ENVIRONMENT

On the basis of definitions, it is noticed that a software agent is a piece of software that is able to act autonomously in particular environment. Figure1 from Wooldridge [3] illustrates how agent interacts with its environment. However, there is no commonly accepted definition by many researchers. Generally, it is stated that an agent is a software entity that is able to conduct information-related tasks without human supervision [1], which can be viewed as an autonomic property of an agent which shows that software agent have decision making capability before taking any action[2] as shown below in the figure 1:

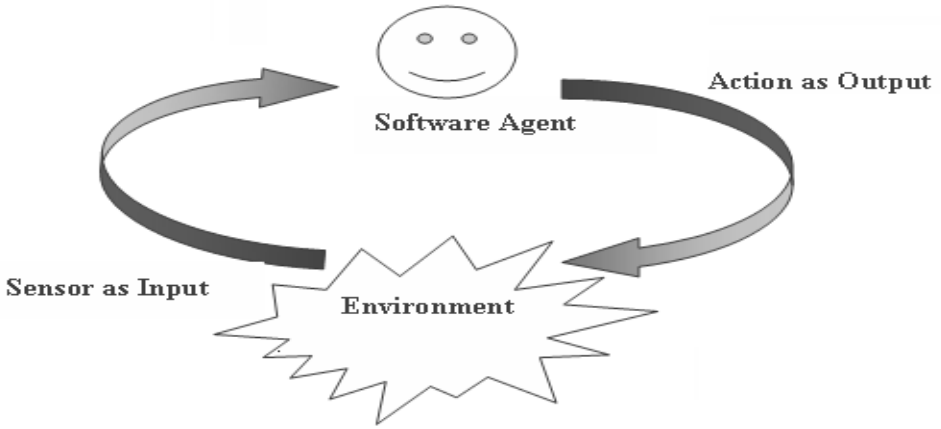


Figure 1: Software Agents and its Environment

## III. MAIN FEATURES OF SOFTWARE AGENTS

- **Reactivity** Agent should be able to perceive its environment and respond to changes that occur in it. It shows its reactive behavior based on some changes in input.
- **Proactivity** An agent should also have the ability to take the initiative and not only react to external signals. This helps agent to pursue its individual goals (goal-directed behavior).
- **Cooperation** An agent should be able to interact with other agents. This can be arranged via agent-communication language.
- **Learning** shows that agents have to learn new things when they interact with external environment. It increases the performance of the agents with the collection of new knowledge gained.

## IV. DIFFERENT TYPES OF SOFTWARE AGENTS

There are various types of software agents which are noticed by many researchers and all have their own role to play. Some of them are shown in figure 2 which are as:

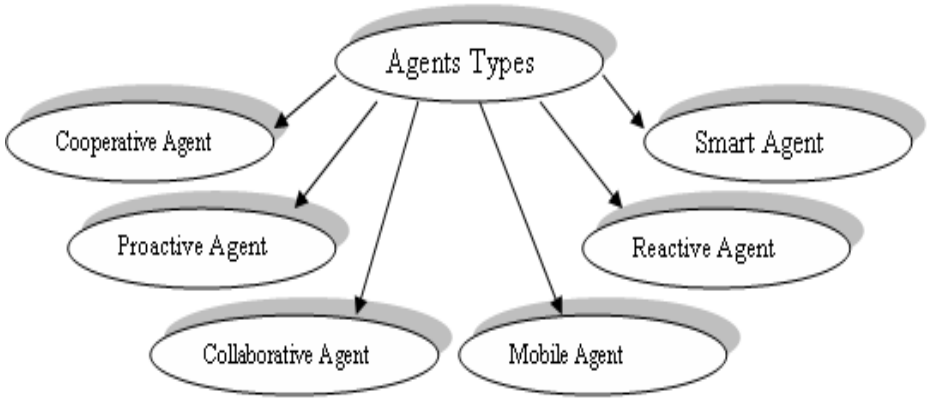


Figure 2: Types of Software Agents

**4.1 Cooperative Agents** communicate with other agents and give their next response based on that communication.

**4.2 Proactive Agents** initiate actions without user prompting.

**4.3 Collaborative Agents** are proactive and cooperative with other agents. They share their information with others within the same environment or group.

**4.4 Mobile Agents** are those who are able to migrate from host to host to work in a heterogeneous network environment.

**4.5 Reactive Agents** are reactive in nature, senses input and take decision for the specific tasks for which these are responsible.

**4.6 Smart Agents** are autonomous, cooperative and learner in nature so able to perform its tasks efficiently and smartly.

**Multi-Agent System (MAS)**

Multi-Agent Systems (MAS) are systems composed of multiple agents and these multiple agents work together to achieve the main objective.

## V. SOFTWARE AGENT: HOW TO TAKE DECISIONS

To become a responsive and proactive agent there is requirement of decision making capability. For example, a responsive agent responds to the environment inputs it senses. But to do so, the agent must decide how to respond as well as the most appropriate time to respond, whether it does so immediately or has time to analyze the situation. Furthermore, a proactive agent is able to take action without being specifically prompted to, if it senses an opportune scenario. Clearly this capability requires an agent be able to decide both when to take action as well as what action to take.

Furthermore, beyond simply making a decision, not all decisions are good decisions. Consequently decision making protocols are often analyzed and compared by parameters such as: negotiation time, simplicity, stability, social welfare, pareto efficiency, individual rationality, computational efficiency, and distribution and communication efficiency. In terms of negotiation time, it is clearly not useful for an agent to take exceedingly long periods of time to make a decision such that the decision making mechanism cannot be used in practical situations.

An unstable design mechanism does not repeatedly arrive at the same conclusion in identical scenarios. Consequently, with unpredictable choices, an unstable design mechanism cannot be trusted to represent the user of the software agent. Social Welfare is a measure of the overall value of all agents as a sum of each agent's payoff.

Pareto efficiency also views the overall global perspective in which no alternate solution benefits any individual agent. Individual rationality on the other hand pertains to each agent individually rather than collectively. For an agent to be individually rational, the resulting payoff from a decision must be no less than the payoff an agent receives by not participating in whatever the decision at hand may be. If an agent is not computationally efficient, it cannot be implemented in a realistic setting and is effectively useless. Similarly, if communication between agents and the distribution of processing between multi-agent systems is not efficient then the system will be subject to computational limitations and may not necessarily be a useful decision making mechanism [7].

One type of decision making theory is Subjective Expected Utility (SEU), which is a mathematical technique of economics that specifies conditions for ideal utility maximization. However SEU deals only with decision making and does not describe how to model problems, order preferences, or create new alternatives. Furthermore, SEU theory requires strong assumptions such as the consequences of all alternatives are attainable, and as a result it cannot be applied to complex real problems [8].

Rational Choice is an economic theory based upon a hypothetical `economic man' who is cognizant of his environment and uses that knowledge to arrange the desired order of possible actions. However, much like SEU, rational choice theory falls short as a complete decision making model because it does not specify how to perform the calculations necessary to order choices [10].

Welfare economics analyzes the effect of resource distribution amongst members of the society as a whole. The aforementioned social welfare is a measure of welfare economics which seeks to maximize the average utility of each member in the society. A similar concept is egalitarian social welfare which seeks to maximize the value of the worst member of the society. However, there are limitations which restrict the satisfiability of the members. Fundamental desirable properties of a social choice rule are:

- Existence of a preference ordering for all possible choices which is defined for all outcome pairs,
- An asymmetric and transitive ordering,
- Pareto efficient outcome,
- Independence of irrelevant alternatives, and
- No single agent dictator dominating the preferences of others.

# VI. WHAT IS GAME THEORY?

Game theory is a branch of mathematics that aims to lay out in some way the outcomes of strategic situations. It has applications in politics, inter-personal relationships, biology, philosophy, artificial intelligence, economics, and other disciplines. John von Neumann is looked at as the father of modern game theory, largely for the work he laid out in his seminal 1944 book, Theory of Games and Economic Behavior, but many other theorists, such as John Nash and John Maynard Smith, have advanced the discipline which is applied in many applications because its scope has greatly increased recently.

# VII. DEFINITION OF GAME THEORY

In the form of economics, it is a theory of competition stated in terms of gains and losses among opposing players. As defined by Parsons and Woolridge game theory as “studies interactions between self-interested agents”. In particular it studies the problems of how interaction strategies can be designed that will maximize the welfare of an agent in a multi-agent encounter, and how protocols or mechanisms can be designed that have certain desirable properties"[9]. Game theory is also described as a collection of techniques to analyze the interaction between decision- makers using mathematics to formally represent ideas. Thus, game theory serves as a technique which attempts to compute an optimal choice amongst several in a strategic interaction. One of the driving tenants of game theory is that in a game of a two players, opponents must seek to minimize their potential for loss while maximizing their potential for benefit [9].

# VIII. LIMITATIONS OF GAME THEORY

The most limiting constraint of game theory's applicability to general multi-agent decision making is the computational efficiency evaluation criteria of decision making mechanisms. To function as a generalized decision mechanism, a game theoretic agent would have to be able to adapt to varying input requirements, opposing players, different rule sets, and unique preference relations for each game and set of players. While game theory defines various solution techniques, some of which are optimal, the solution concept varies among games and there does not exist a single solution approach applicable on all the games.

Furthermore, game theory focuses upon the existence of solution concepts but does not specify the algorithmic techniques necessary to compute the solutions. Consequently, many game theoretic techniques assume unlimited computational resources and are often NP-Hard problems [9]. And thus, neither the computational efficiency nor the negotiation time constraints are necessarily satisfied by a game theoretic decision making mechanism.

# IX. MAKING SOFTWARE AGENTS AS AN EXPERT SYSTEM

## 9.1 What is an Expert System?

Expert Systems are computer programs which play the role of an expert related to their domain. The main goal is to understand the situation and take intelligent decisions like human beings. The

fundamental principle underlying an expert system is to embed domain specific knowledge regarding how to solve a particular problem within a production system such that it may reason and attempt to devise a solution with a quantifiable confidence in that decision. Additionally, an expert system also embodies the ability to explain its reasoning by responding to `how' and `why' queries by the user. The knowledge base and explanation subsystem illustrated in **Figure 3** supply the extensive domain knowledge and provide the justification of the systems reasoning respectively. The inference engine performs the reasoning for the expert system just as the control structure of a production system selects among the applicable production rules.

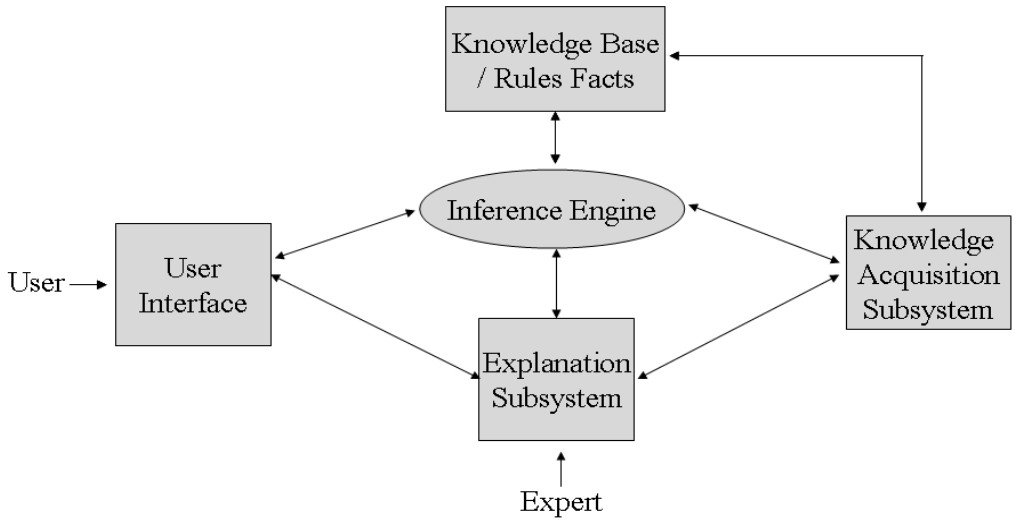


Figure 3: Expert System Architecture

### 9.2 Expert System as a Smart Agent in Making Decisions

It is noticed that Expert System has characteristics like software agents. Kay and McCarthy's notion of a software agent carrying out a goal and asking for advice if necessary is fundamental to the function of an expert system. As already described, an expert system is designed to try and solve a particular problem, and furthermore does so without additional interaction unless the user must be queried to obtain information necessary to make a decision.

The characteristic of being situated is satisfied by the general software agent capability of perceiving the environment in the form of askable information and acting upon the environment by the selected decision signal. The askable information may be obtained from either another agent capable of answering queries or a human user and thus an expert system is also social.

Once an expert system has been programmed with the knowledge of a subject matter expert, and obtained all of the necessary information from the environment to guide its decision making process the resulting decision is obtained autonomously without further intervention. To be flexible, an expert system would need to be responsive and proactive. Although an expert system may respond to the signals it receives and requires to make informed decisions, it cannot proactively analyze the environment and decide when to take action. Effectively, although an expert system does not meet all of the generally agreed upon guidelines which describe an intelligent software agent, the majority of the criteria are met and therefore an expert system may be regarded as a rudimentary intelligent agent.

### 9.3 How to Enhance the Decision Making Approach

The efficiency of the system performance is dependent upon the inference engine's search algorithm so a good searching algorithm should be applied. Main of them are as:

- **Rule-based expert system** performs a goal-driven state space search and
- **Case-based expert system** search for the most similar case to the current scenario.

When searching among possible options there are various techniques such as a depth-first or breadth-first search.

- A **breadth-first search** examines all of the possible options at the current state of the system. A breadth first search implements goal-driven state space search, and consequently it is most efficient if the first line of reasoning traversed leads to a solution so the system does not have to backtrack and try another possible sequence of actions.
- A **depth-first search** on the other hand traverses the state space graph along a single line of reasoning until a terminal node is met either corresponding to a successful conclusion, otherwise if the line of reasoning is unsuccessful it then backtracks to consider the next line of reasoning.

Alternatively, in this paper we propose game-theoretic concepts of utility measures may be incorporated to enhance the decision making performance of expert systems. Depending upon the implementation, the utility measure is not necessarily tied to a particular payoff, but rather is a preference ordering by which the possible actions are arranged in order of desired outcome. The particular utility values assigned to the knowledge set are implementation dependent.

### 9.4 Example: Basketball Game Expert Coach

We have created a rudimentary basketball coach system termed Coach Rule-base Expert System (CRES), which calls an offensive play according to specific game situations and player capabilities. Game of basketball serves as a beneficial example because it embodies several meaningful criteria such as diametrically opposed players, a complex decision domain, and a two level decision hierarchy by which first the defense selects a play and then the offense calls a play. Here we have four situations where a smart agent takes the decisions autonomously which are as:

1. **Last minute game situation** is defined as when there is less than a minute left in the game and the offensive team is down by two points or less. The coach would also know the capabilities of his own players, and so if he has good jump shooters he will go for the win and attempt a three point shot. Otherwise, rather than hoping for a lucky bounce, if the coach does not have exceptional three point shooters he will instead call a play looking for a two point basket tying the game so that they may go for the win in overtime.
2. **A man-to-man defense** is defined as one in which a single defender is guarding each player regardless of where they move on the court, and that there are not multiple defenders guarding any single player. Depending upon the skills of the offensive players on the floor there are two possible plays:
   - If there are good jump shooters on the offense, then the coach calls for the offense to set a screen opening up a jump shot for one of the players. Due to the fact that each defender is focusing on an assigned offensive player, they are most likely guarding the good offensive player tightly, so by setting a screen for a teammate, an offensive player may be freed for a high percentage jump shot.
   - If the offensive team does not have good jump shooters playing at the particular point in the game but the defense is guarding them in a man-to-man defense, the coach calls for a pick and roll in which the offensive players work together to move closer to the basket for a better percentage shot.
3. **A zone defense** approach in which a player guards a particular region of the floor rather than a particular player. Here, the coach recognizes a zone defense by the fact that the same defender is not following offensive players across the floor and there are not multiple defenders guarding a single offensive player. Once again depending upon the individual capabilities of the offensive players there are two basic plays the coach may call:
   - If the offensive team has good outside shooters, then it is recommended to attack the zone defense by shooting long distance jumpers that the zone is not adequately guarding against. The spacing of the defenders in a zone defense to cover the floor opens up the inside for a dominant low post player to post up.

- If the offense does not have exception jump shooters, they should pass the ball in for a post player to get a closer higher percentage shot.

4. **Double Team** is applied when the offensive team has a star player the defense may double team the individual player. A double team is easily recognized by the coach, in which there is not a single defender, but rather multiple players simultaneously guarding the star player. Here, another player on the offensive team is not being guarded, and the coach advises the team to pass the ball to the open player who is not being guarded and effectively the highest percentage shot.
   This expert coach system is designed to vary its performance in accordance to the abilities of the players it is emulating such as whether the team consists of skilled jump shooters or post players. This example is based upon the perspective that the offensive team has excellent jump shooters. The utility measure decision making enhancement is incorporated by strategically ordering the rules based upon average utility.

The Utility Preference shows utility ordering assigned for each possible defense based on their chances to win the game with their possible situations and their possible winning directions which are shown in the Table 1 below:

Table 1: Utility Preference

| Offense/ Defense | Last Minute | Man Def. | Zone Def. | Double Team | Sum | Average | Utility |
|---|---|---|---|---|---|---|---|
| Win_on_3 | 7 | 4 | 4 | 5 | 20 | 5 | 5 |
| Tie overtime | 6 | 3 | 2 | 3 | 14 | 3.5 | 3 |
| Screen shot | 5 | 6 | 5 | 1 | 17 | 4.25 | 4 |
| Free_player | 4 | 7 | 7 | 7 | 25 | 6.25 | 7 |
| Shoot Jumper | 3 | 5 | 6 | 6 | 20 | 5 | 6 |
| Pick Roll | 2 | 2 | 3 | 2 | 9 | 2.25 | 2 |
| Post Up | 1 | 1 | 1 | 4 | 7 | 1.75 | 1 |

It is noticed that if utility value is used then it saves time and move in the right goal-based direction where the possibility of achieving the goal is maximum. So as shown in figure 4 goal is more closer and team is in good state as actions taken by the Coach as an expert system based on decisions which are made on the basis of utility value. The utility enhanced ruled ordering approach arrived at a solution in only its second line of reasoning.

When decisions are not based on their utility value then decisions would be taken randomly as shown in figure 5 where goal is achieved after taking many steps not goal-directed conformation is here. This random order decision making approach arrived at a solution in its fifth line of reasoning.

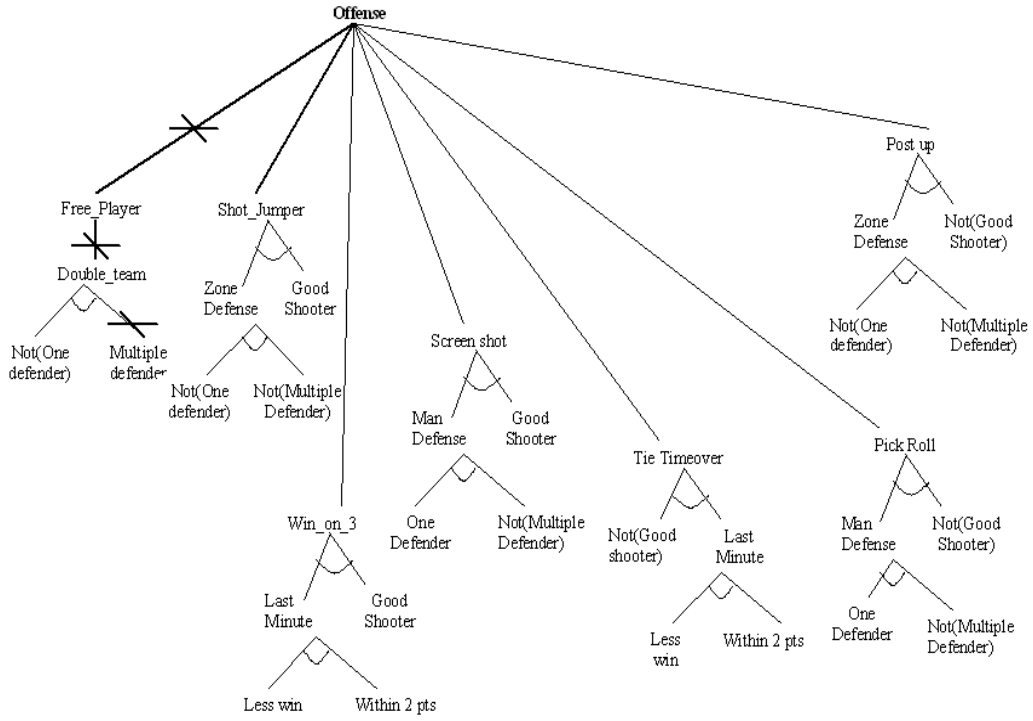


Figure 4: Utility Enhanced Decision Making

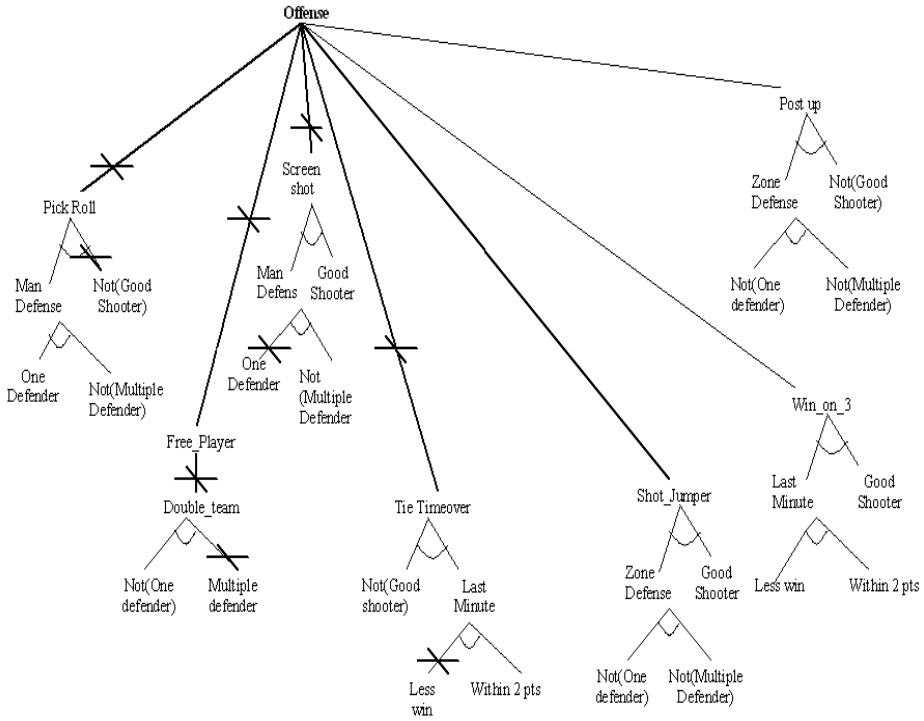


Figure 5: Random Ordered Decision Making

Note: The bold lines mark the lines of reasoning attempted moving left to right, with X's denoting eliminated options.

## X. CONCLUSION

Making an intelligent and good decision is not an easy task. A smart agent achieves the given goal with minimum instructions from others and has the capability to reason and make decisions related to that domain. Here game theoretic utility notions are used to enhance the decision making mechanism of an expert system. Doing so provides a more strategic means of improving expert system performance rather than relying upon inconsistent heuristic approaches. Thus, making decisions is no easy task but doing so in a more strategic rational manner has greater value than making random choices.

## XI. FUTURE WORK

Here a relatively simple rule based system approach is used so it can be expanded with a larger rule based system to incorporate more specific games and a defensive expert system could be coupled to oppose the offensive expert system in which case analysis can be performed on the possible result by the opposing system. A video game with multiple graphical effects and an expert system with good artificial intelligence could be applied for good game application.

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# CALCULATION OF POWER CONSUMPTION IN 7 TRANSISTOR SRAM CELL USING CADENCE TOOL

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## *ABSTRACT*

*In this paper a new 7T SRAM is proposed. CMOS SRAM Cell is very less power consuming and have very less read and write time. In proposed SRAM an additional write bit line balancing circuitry is added in 6T SRAM for power reduction. A seven Transistor (7T) cell at 45 nm Technology is proposed to accomplish improvement in stability, power dissipation and performance compared with previous designs. Simulation result of proposed design using CADENCE TOOL shows the reduction in total average power consumption.*

***KEYWORDS***:- Conventional SRAM, Low Power, Power Consumption.

## I. INTRODUCTION

Advances in CMOS technology have made it possible to design chips for high integration density, fast performance, and low power consumption. To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to very small features and dimensions [1]. Over the last few years, devices at 180nm have been manufactured; the deep sub-micron/nano range of 45nm is foreseen to be reached in the very near future.

Technology scaling results in a significant increase in leakage current of CMOS devices. As the integration density of transistors increases, leakage power has become a major concern in today's processors and SoC designs. Considerable attention has been paid to the design of low power and high-performance SRAMs as they are critical components in both handheld devices and high performance processors. Different design remedies can be undertaken; a decrease in supply voltage reduces quadratically the dynamic power consumption. However, with an aggressive scaling in technology as predicted by the Technology Roadmap, substantial problems have already been encountered when the conventional six transistors (6T) SRAM cell configuration is utilized at an ultra-low power supply; this cell shows poor stability at very small feature sizes[2]. A seven transistors (7T) SRAM cell configuration is proposed in this paper, which is amenable to small feature sizes encountered in the deep sub-micron/nano CMOS ranges. The schematic and Layout of proposed 7T SRAM Cell is shown in Figure 1.1 and figure 1.2 respectively.

The objective of this paper is to investigate the transistor sizing of the 7T SRAM cell for optimum power. An innovative precharging and bitline balancing scheme for writing operation of the 7T SRAM cell is also proposed for maximum standby power savings in an SRAM array[3]. CADENCE simulation results confirm that the proposed scheme achieves 45% of power savings compared to the conventional SRAM cell array based on the 6T configuration. The paper starts with introducing the proposed 7T cell and the design method used to find the optimal transistor sizing for the proposed SRAM cell[4]. Finally, the impact of process variation on the cell's stability and power consumption is analyzed to show that the 7T SRAM cell has a very good tolerance in the presence of process variations [5].

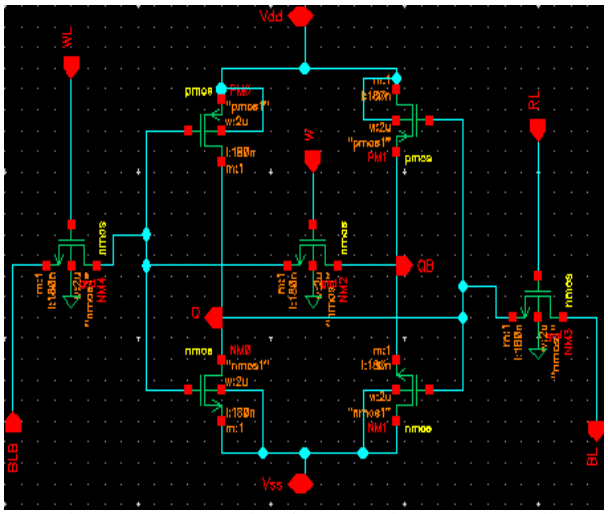


Figure 1.1 Schematic of Proposed 7T SRAM Cell

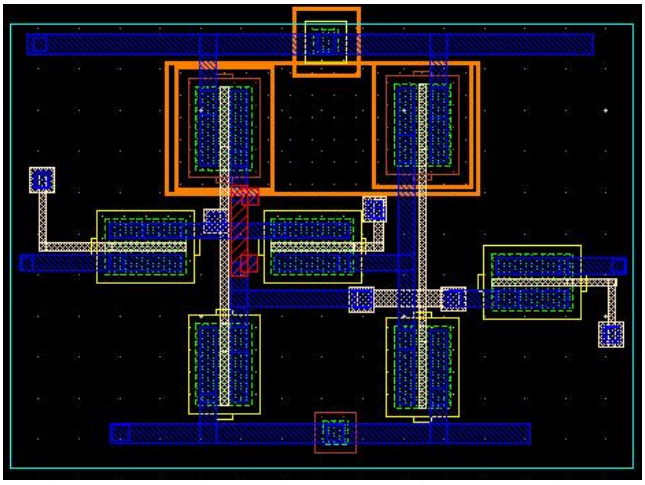

Figure 1.2 The physical layout view of the proposed 7T cell

## II. LEAKAGE CURRENT OF 7T SRAM CELL

Gate length scaling increases device leakage exponentially across technology generations. Leakage current is the main source of standby power for a SRAM cell. In nano-scale CMOS devices, the major components of leakage current are the sub-threshold leakage, the gate direct tunneling leakage, and the reverse biased band-to- band tunneling junction leakage. The sub-threshold leakage, which is defined as a weak inversion conduction current of the CMOS transistor when $V_{gs} < V_{th}$, represents a significant leakage current component in the off-state.
The equation for the sub-threshold leakage current is given by (1)

$$Isub = I_o e^{(Vgs-Vth)/\eta kT/q} (1-e^{(-Vds)/kT/q}) \quad - (1)$$

Where,

$$Io = \mu_o C_o x (W/L)(kT/q)^2 (1-e^{1.8}) \quad - (2)$$

*W* and L are the transistor's channel width and length, μ0 is the low field mobility, *Cox* is the gate oxide capacitance, *k* is Boltzmann's constant, and *q* is the electronic charge.

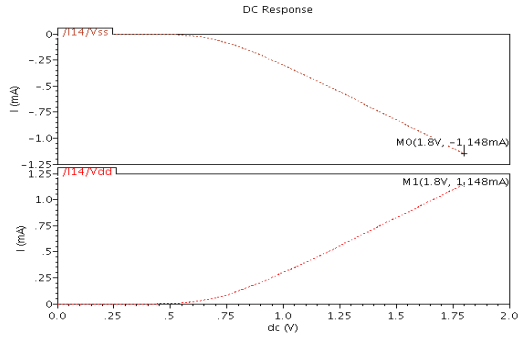


Figure 2 Leakage current of Proposed 7T SRAM

## III. WRITE BITLINE BALANCING CIRCUITRY FOR POWER REDUCTION

The proposed write concept depends on cutting off the feedback connection between the two inverters, invl and inv2, before the write operation. The feedback connection and disconnection are performed through an extra NMOS transistor N5, as shown in Figure 1, and the cell only depends on BL_bar to perform a write operation [6]. The write operation starts by turning N5 off to cut off the feedback connection. BL_bar carries complement of the input data, N3 is turned on, and N4 is kept off. The SRAM cell looks like two cascaded inverters, inv2 followed by invl. BL_bar transfers the complement of input data to Q2 which drives inv2, P2 and N2, to develop Q, cell data, which drives invl and develops Qbar. Both BL and BL_bar are precharged "high" before and after each read/write operation [9]. When writing "0", BL_bar is kept "high" with negligible write power consumption.
To write "1", BL_bar is discharged to "0" with comparable power consumption to a conventional write. The write circuit does not discharge one of the bit lines for every write operation and the activity factor of discharging BL_bar is less than "1".
The proposed write bitline balancing circuitry, output waveform and power consumption graph is shown in the Figure 3.1, Figure 3.2 and Figure 3.3 respectively.

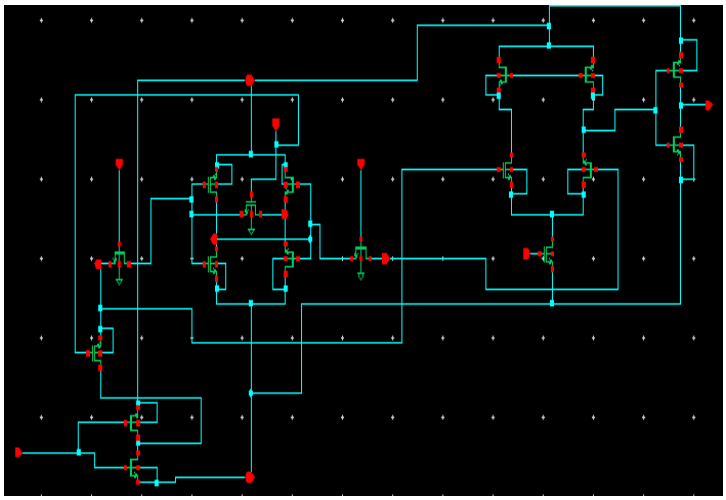

Figure 3.1 Proposed write bit line balancing circuitry

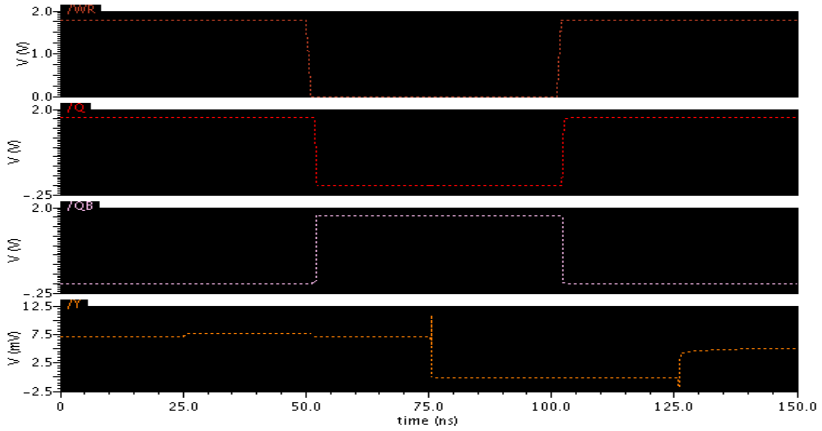


Figure 3.2 Output Waveform of 7T SRAM cell

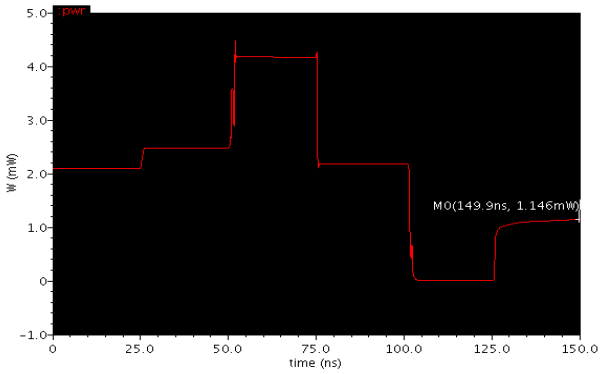


Figure 3.3 Power consumption of Proposed 7T SRAM.

## IV. SIMULATION RESULTS

In this paper, a novel write methodology is proposed which depends on cutting off the feedback connection between the two back-to-back inverters in the SRAM cell and requires a 7T SRAM cell. The proposed technique reduces the number of times to charge and discharge the large bit lines capacitance to reduce the write power consumption. Simulation results show that the write circuitry scheme for the proposed 7T SRAM cell based array achieves a 45% reduction in power consumption at a 1.8V power supply voltage and typical process corner compared with a conventional 6T SRAM cell based array. The Figure 4.1 & Figure 4.2 also shows the waveform of leakage current and power consumption. The Results of leakage current and power consumption using Cadence Tool is given in TABLE I.

Table I: Simulation results of the 7T SRAM cell

| | |
|---|---|
| Process Technology | 45 nm |
| Power Supply Voltage | 1.8 V |
| Precharge Voltage | 1 V |
| Leakage Current | 1.148 mA |
| Power Consumption | 1.146 mW |

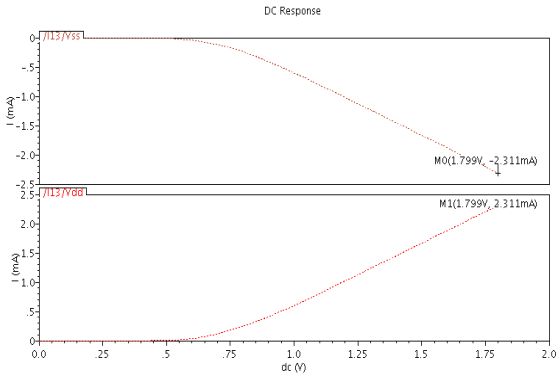


Figure 4.1 Leakage current of 6T SRAM

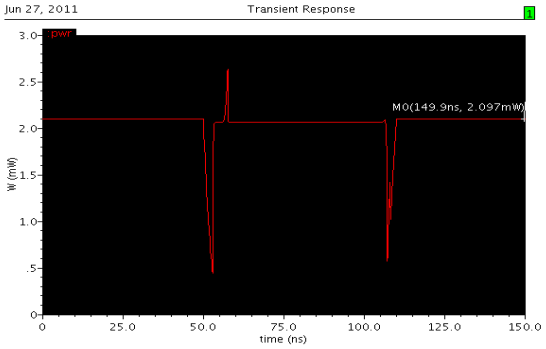


Figure 4.2 Power consumption of Proposed 7T SRAM

# V. CONCLUSION

In this paper, a novel write methodology is proposed which depends on cutting off the feedback connection between the two back-to-back inverters in the SRAM cell and requires a 7T SRAM cell. The proposed technique reduces the number of times to charge and discharge the large bit lines capacitance to reduce the write power consumption. The simulation results using CADENCE TOOL show that much better tolerance to process variation is achieved using the proposed 7T SRAM cell.

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# REFRACTOMETRIC FIBER OPTIC ADULTERATION LEVEL DETECTOR FOR DIESEL

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## *ABSTRACT*

*Adulteration of diesel with kerosene is common malpractice since kerosene is cheaper than diesel. Such adulteration results in increased pollution, reduced lifetime of components, decrease in engine or machine performance etc. This paper presents a simple, extrinsic intensity modulated fiber optic sensor for determining adulteration of diesel by kerosene. The sensing principle is based on variation in reflected light intensity due to change in the refractive index of adulterated diesel. A parallel two fiber sensor probe consisting transmitting fiber and receiving fiber with a reflector is used as a sensor. An adulterated diesel is considered as a medium between sensor probe and reflector. A prototype is fabricated and tested in laboratory for different levels of adulteration of diesel by kerosene.. The sensor is useful due to its simple construction, operation, safety with inflammable fuels and the possibility of making it compact and portable for in-situ measurements. Micro-controller is used for incorporating totally automatic and adding further sophistication in final display so that it is more useful to layman i.e. society. Thus inexpensive and portable adulteration level detector is proposed.*

***KEYWORDS:*** *fiber optic sensor, fuel adulteration, adulteration level detector, refractometeric sensor, fiber optic sensor probe.*

## I. INTRODUCTION

The blending of kerosene with automotive diesel is generally practiced by oil industry worldwide as a means of adjusting the low temperature operability of the fuel [1]. This practice is not harmful or detrimental to tailpipe emissions, provided the resulting fuel continues to meet engine manufacturer's specifications [2]. High level adulteration causes increase in emissions, as kerosene is more difficult to burn than gasoline. Adulterating of diesel with kerosene is common malpractice since kerosene is cheaper than diesel. Such adulteration results in increased pollution, reduced lifetime of components, decrease in engine or machine performance etc. There are number of techniques used to detect adulteration like use of markers, gas chromatography etc. However, for in-situ measurement of level of adulteration these techniques fall short.

Fiber optic sensors (FOS) have received considerable attention in the recent years because of their inherent immunity to electromagnetic interference, safety in hazardous and explosive environment, high sensitivity and long distance remote measurements. The miniature size, low cost, intrinsic safety and ease of installation of FOS makes this system ideal for applications in various engineering areas including numerous in line chemical, food, beverages or medical analysis and monitoring system.

Languease presented an optical fiber refractometer for liquids which eliminates the influence of attenuation due to the liquids [3]. L.S.M. Wiedemann etal proposes a method to detect adulteration by using physico-chemical properties of gasoline samples and performing statistical analysis [4]. Sukhdev Roy proposes a method of changing the refractive index of cladding of fiber for detecting adulteration of fuel which is based on the modulation of intensity of light guided in the fiber due to change in the refractive index of the cladding formed by adulterated fuel and the phenomenon of evanescent wave absorption [5]. L. M. Bali et al has developed an optical sensor for determining the proportional composition of two liquids in a mixture [6]. It is based on changes in the reflected light intensity at the glass-mixture interface brought about by the changes in the proportion of one liquid

over that of the other in the mixture. It uses a simple configuration consisting of the end separated fibers where T-R coupling is decided by medium filled in the gap. This configuration however is difficult to handle because of precision needed for alignment so as to get maximum sensitivity. This paper presents a simple, extrinsic intensity modulated fiber optic sensor probe for determining adulteration of diesel by kerosene. The sensing principle is based on variation in reflected light intensity due to change in the refractive index of adulterated fuel. A sensor probe consists of parallel transmitting fiber and receiving fiber and a reflector is placed at distance from the sensor probe. A gap between sensor probe and reflector is filled with adulterated fuel. The paper discuses and proposes parallel two fiber sensor probe and a reflector with liquid media whose refractive index in to be detected. An extrinsic FOS measures refractive index of adulterated diesel based on reflective intensity modulation.

In this paper, principle of operation for detecting adulteration in diesel by using the sensor probe is discussed in detail in section 2. Further section 3 discusses how the probe is designed and how it can be configured for measuring of adulteration in diesel by kerosene. It further discusses how to mount the sensor probe for in-situ measurement of adulteration of diesel in automobiles. Section 4 discusses block diagram of microcontroller based experimental set up for measuring the adulteration level. Flowcharts of the programs are explained in detail for two configurations. Next section 5 discusses results obtained after testing the probe for different values of percentage adulteration in diesel by kerosene. Finally the concluding section gives the important findings of the work.

## II. PRINCIPLE OF OPERATION

The proposed probe is based on the fiber optic sensor reported by Choudhari etal[7,8,9]. The fiber optic probe consists of two fibers: one fiber as transmitting fiber (T) and other is used as receiving fiber(R) .Both the fibers are of same type and same dimension. The fiber optic sensor (FOS) used is extrinsic type. So the light is carried up to the modulating zone by transmitting fiber where the properties of the incident light are modulated by modulator. The modulated light is carried out to the detector by receiving fiber. The modulating zone is between the fiber probe and a reflector kept at distance Z from transmitter.

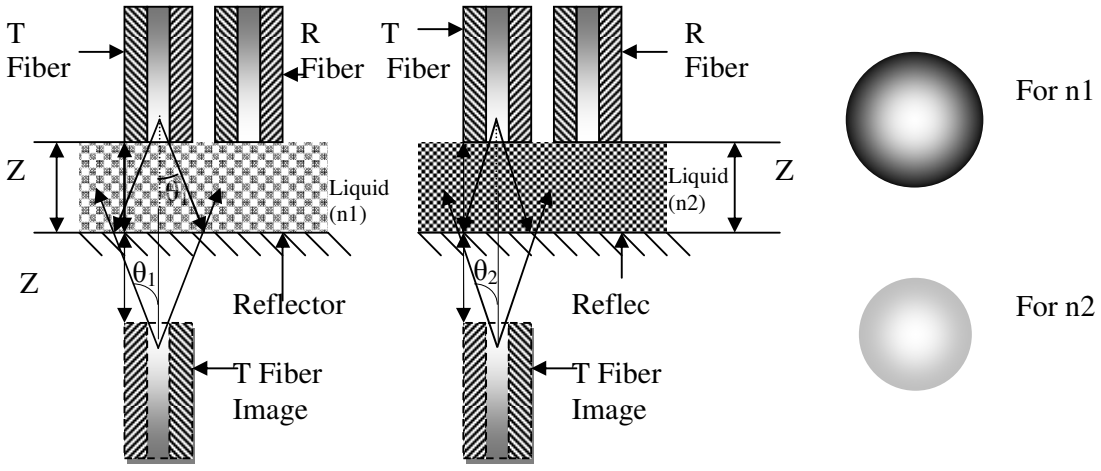


Fig. 1(a) Model of fiber optic Refractive index sensor

Fig. 1(b) Cross sections of Reflected cone for different refractive indices

An adulterated fuel is used as medium. As shown in Figure 1(a) the incident light in the form of cone of emission from transmitting fiber gets reflected back in the form of expanding cone of light towards the receiving fiber. The cone of emission depends upon the refractive index of the medium filled between the fiber probe and reflector. The medium having refractive index n1 is filled between the gap in sensor probe and reflector. The angle of emission is $\theta_1$. It is given by equation

$$\theta_1 = \sin^{-1} (NA/n_1) \quad (1)$$

where NA is numerical aperture of transmitting fiber and $n_1$ is refractive index of liquid filled between sensor probe and reflector. The output power is determined by the amount of light reflected by reflector. It is calculated by considering overlap area between the receiving fiber cone and reflected cone emitted by image of transmitting fiber. The receiver collects the optical power that falls in its cone of acceptance and guides it up to the detector.

Consider the gap is filled with liquid having refractive index $n_2$ as shown in Figure 1. Since $n_2 > n_1$ the cone of emission is $\theta_2 < \theta_1$. , $\theta_2$ is given by

$$\theta_2 = \sin^{-1} (NA/n_2) \quad (2)$$

where NA is numerical aperture of transmitting fiber and $n_2$ is refractive index of liquid filled between sensor probe and reflector. The light rays are concentrated in smaller cone thus concentrating more intensity in the receiving fiber. Hence received output power increases. Figure 1(b) shows light received by the receiving fiber for refractive indices $n_1$ and $n_2$ respectively. Keeping Z fixed, the output thus depends on the variation in adulteration level of diesel by kerosene i.e. refractive index of liquid filled between sensor probe and reflector.

# III. FOS PROBE FOR ADULTERATION DETECTION:

Fiber optic sensor probe consists of light source, detector, and chemical cell with holes and a reflector as shown. The light from source is launched in to optical fiber and guided to a region between sensor probe and reflector. Light is reflected from reflector through sample solution. It is then collected by the receiving fiber. The other end of this fiber probe is connected to a detection and measuring system. The fiber used for the experimentation is a plastic fiber of 488 μm core diameter with numerical aperture of 0.47. Cladding thickness (cl) = 0.612mm. T-R separation with jacket(s) = 0.0mm, angle between T-R fibers = $0^0$. The length of the fiber = 85mm. Both transmitting and receiving fibers are of same type. A round cut transparent glass is press fitted to the sensing tip end of the fibers in order to avoid damage of polished tip due to the interaction with any chemical/fuel under test. Fiber sensor probe consists of a RED bright LED and photodiode (L14G3) enclosed in a brass assembly as shown in Figure 2(a). A chemical cell is fabricated having holes on the side walls and reflector is press fitted at the bottom. Mirror is used as a reflector. This chemical cell is fitted to the fiber sensor tip assembly. The sensing distance between the senor probe and reflector in chemical cell is adjusted so as to sense the variation in refractive index of adulterated fuel.

### 3.1 Configuration Description:

Fig 2. (a) shows configuration for detecting in situ measurement of adulteration level of diesel by kerosene. It has three indicator LEDs showing different adulteration levels such as no adulteration, adulteration within limits and over adulteration. This probe consists of transmitting and receiving fiber (sensor probe) and a reflector. A light is launched in the transmitting fiber and receiving fiber received the light reflected from reflector which is further detected by photo-detector. A reflector is fitted at the base of chemical cell with holes as shown in Figure 2(a). If the probe is immersed in the fuel (diesel) then depending upon the adulteration of diesel by kerosene RED, Yellow or Green LED

glows. Green LED indicates that there is no adulteration of diesel by kerosene (0%). Yellow LED indicates that there is adulteration of diesel by kerosene but it is within the tolerance limits (up to 30%).

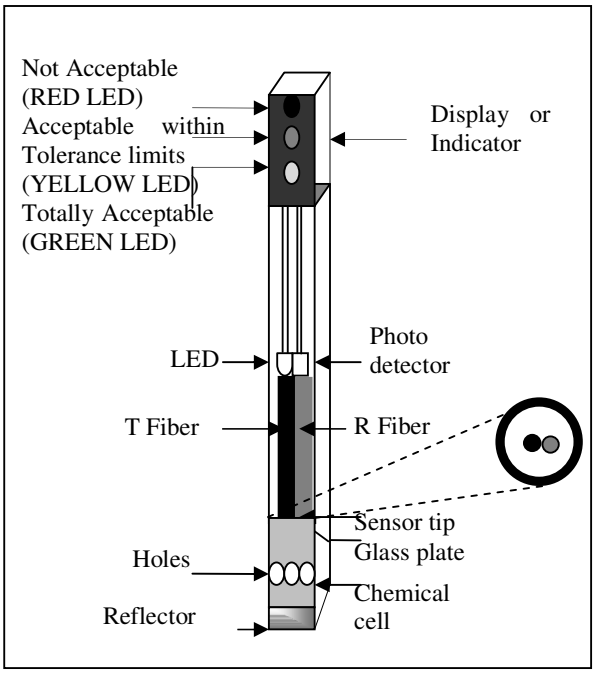


Fig.2 (a) Configuration indicating level of adulteration

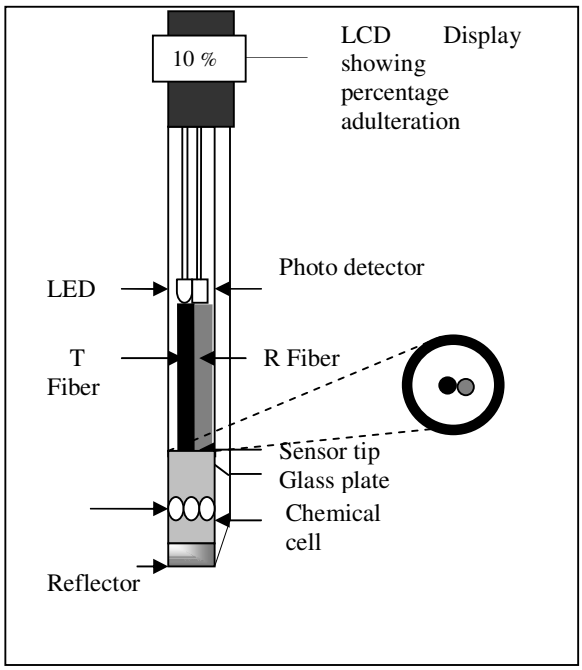


Fig.2 (b) Configuration showing level of adulteration numerically

If Red LED glows then diesel is highly adulterated by kerosene i.e. not acceptable (>30%). Such a probe is very much useful for in situ measurements. This probe can be fitted directly to the diesel tank of the vehicle. Fig 2(b) shows configuration used for detecting percentage adulteration in laboratory. In this configuration instead of indicating the adulteration level, its numerical value is actually displayed on the LCD display.

### 3.2 Probe Mounting:

A cup is designed with perforated upper part on side wall and opaque lower part and fitted at the mouth of the fuel tank as shown in Figure 3(a). Initially small quantity of diesel is to be filled and then depending upon the level of adulteration RED, GREEN or YELLOW LED will glow. Figure 3(a) , Figure 3(b) and Figure 3(c) shows how the sensor actually works for detecting adulteration in diesel by kerosene. . If RED indicator glows showing adulteration then diesel should not be filled in the vehicle. If GREEN or YELLOW indicator glows this indicates no adulteration or adulteration within limits. Then diesel should be filled in vehicle.

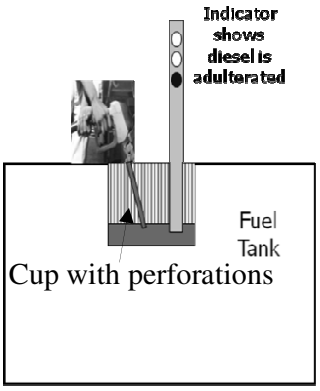


Figure 3(a) Indicator showing Adulteration

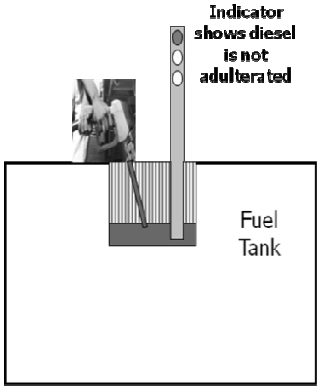


Figure 3(b) Indicator showing no adulteration

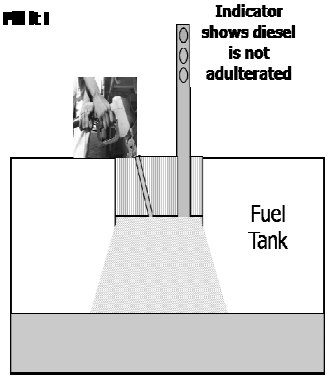


Figure 3(c) No adulteration results in filling the tank

## IV. EXPERIMENTATION:

Adulteration level detector consists of a sensor probe and electronic components, ADC, Micro-controller and LCD display or LEDs. Fig 4 shows block diagram of instrument along with sensor probe.

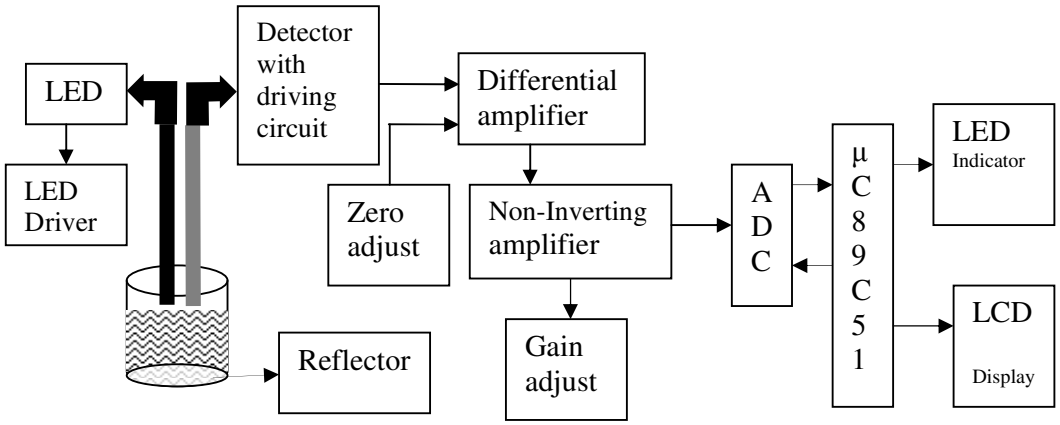


Fig 4. Block diagram of adulteration detector instrument

It consists of light source and its driving circuit, photo- detector and its driving circuit, sensor probe and chemical cell. The experiment was carried out for fixed distance between probe and reflector. The sensor probe consists of two multimode plastic fibers each of diameter 488 micrometer. Photo detector is a phototransistor and its driving circuit which consists of buffer. Differential amplifier is used to amplify difference between detector output and the reference voltage. This reference voltage is meant for zero-adjust of instrument for no adulteration. Non-inverting amplifier is used to further amplify the difference with adjustable gain (span adjustment). Output of amplifier is applied to ADC (AD 0809) which gives binary equivalent of the input analog voltage. Micro-controller is used to calculate the adulteration level and depending upon the binary input it will turn ON respective LEDs which are connected to the port pins. For LCD display the calculated adulteration level is first converted to ASCII code and then displayed on the LCD.

Chemical cell with holes at the side walls is used to test adulterated fuel. The chemical cell is cylindrical in shape with a mirror fitted at a centre of bottom. The mirror is used as a reflector. The experiment was carried out for 0% adulteration (pure diesel) up to 100% adulteration in pure diesel in interval 10% adulteration level. Sensor probe is dipped into sample of fuel under test. The amount of reflected light received by receiving fiber depends on the refractive index of the fuel and distance between sensor probe and reflector. Keeping the distance constant, we get output proportional to refractive index of fuel depending upon its adulteration level by kerosene. The experimental measurements were carried out with variation in adulteration level of diesel by kerosene. Different quantities of kerosene such as 0%(10ml pure diesel), 10%(9ml diesel+1ml kerosene),20%(8 ml diesel + 2 ml kerosene) up to 100%(pure kerosene) are added in diesel to create different adulteration levels. The ZERO adjust potentiometer is adjusted for pure diesel thus making the output voltage zero, indicating 0% adulteration. The span adjustment is done for 100% adulteration i.e only kerosene.

Purpose of using micro-controller is to collect and store the data from different fuel pumping stations and compare them with the standard values. Analytical methods are very tedious and may take hours to conduct different tests in the laboratories for detecting adulteration levels and also these methods are not in-situ. Hence such adulteration detector is not only useful for keeping health of the society but also useful for technical persons which are interested in data analysis.

For configuration indicating level of adulteration, the microcontroller initializes the ADC and output of the sensor is applied to the input channel of ADC. Digital data at the output of ADC is compared with the preset threshold values and accordingly RED, GREEN or YELLOW LED glows indicating over adulteration, no adulteration and adulteration within limits respectively. For configuration showing numerical value of adulteration, the microcontroller initializes ADC and data from the sensor is converted to proper form so that adulteration level is displayed on LCD display unit. Figure 5(a) shows flowchart for LED indicator (configuration 1) and figure 5(b) shows flowchart for LCD display (configuration 2).

## V. RESULTS AND DISCUSSION:

The fiber optic sensor used is extrinsic type. Light is carried up to modulating zone by T (Transmitting) fiber and R(Receiving) fiber which collects it after reflection from reflector fitted at the bottom of the chemical cell at a distance Z from sensor probe. The cone of emission of the T fiber gets reflected back in the form of expanding cone of light towards the R fiber. The cone of emission depends on the refractive index of liquid as given by equation (1) and (2). The output power of R fiber depends upon the overlap area and cross section of reflected cone emitted by image of T fiber. This is given by the cross section of overlap area of reflected cone and the core of receiving fiber. A refractive index increases, angle of emission decrease, but energy density increase. Hence even if overlap area decreases output of the receiving fiber increases which in turn increase the output power. For Z up to 4mm effect of overlap area is dominant on the output power while as refractive index increases effect of energy density within the small cone of emission increase showing increase in output power.

These results show good agreement with those reported by Choudhari et al [9]. Experiment is performed for different adulteration levels such as 0% (pure diesel), 10%, 20% up to 100 %( pure kerosene) at fixed probe reflector separation of 6.22 mm. It is repeated 60 times for same adulteration level. Figure 6 shows histograms for testing the repeatability of the sensor output for adulteration levels. It is observed that for each adulteration level the sensor output shows a spread around mean value. As the observations were made starting from 0% kerosene with adulteration interval of 10%, it is seen that the subsequent peaks are well separated. A statistical T test was used to confirm the non-overlapping of the consecutive distributions. Figure 7 shows mean output voltage variation with increasing adulteration of diesel by kerosene. Though the observations are performed for 0-100% range of kerosene the adulteration of diesel will have significance on lower (approximately upto 30%) kerosene concentration side. It is seen from Figure 7 that the output voltage of the probe almost shows linear variation in this range.

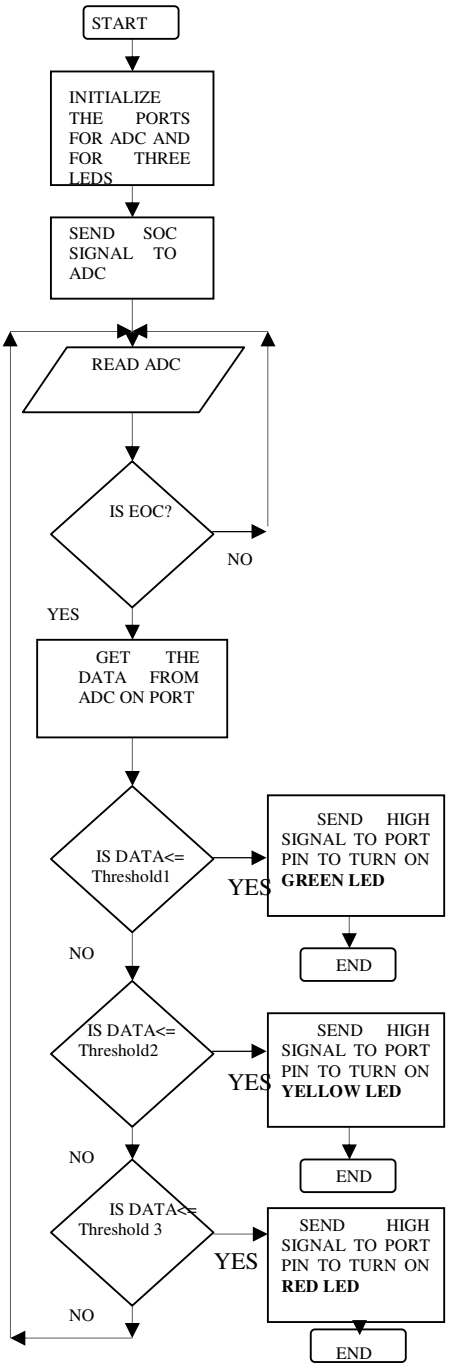


Figure 5(a) Flowchart for configuration 1

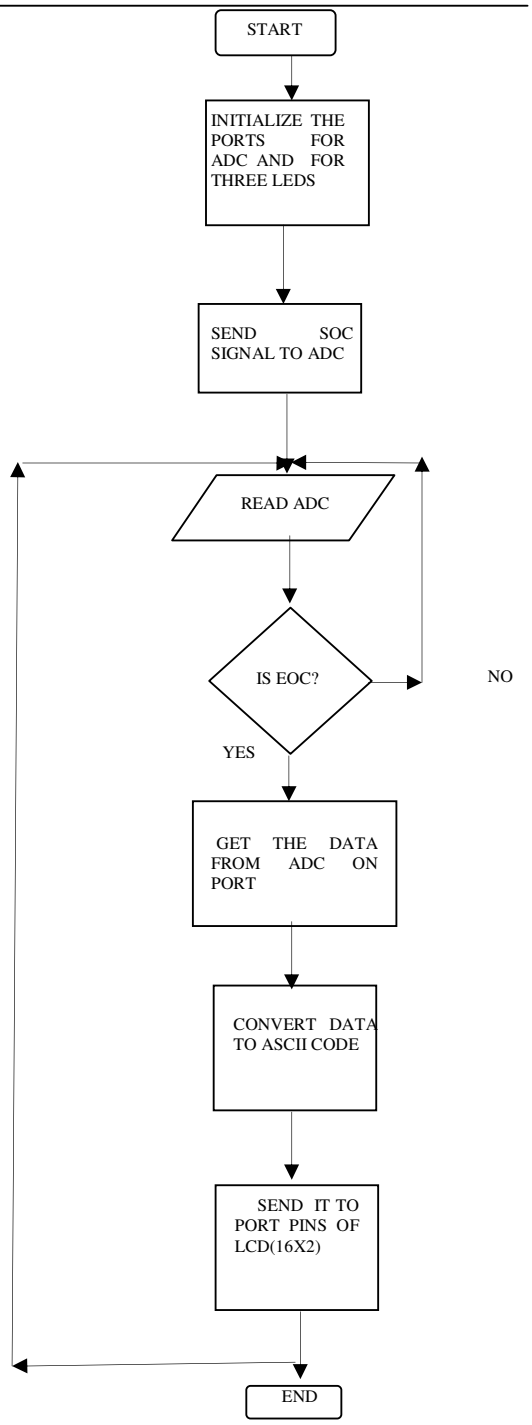


Figure5(b) Flowchart for configuration 2

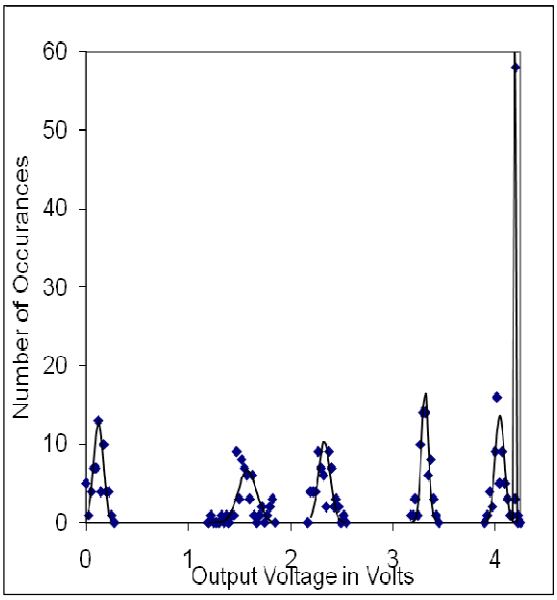


Figure 6 Repeatability of Measurement

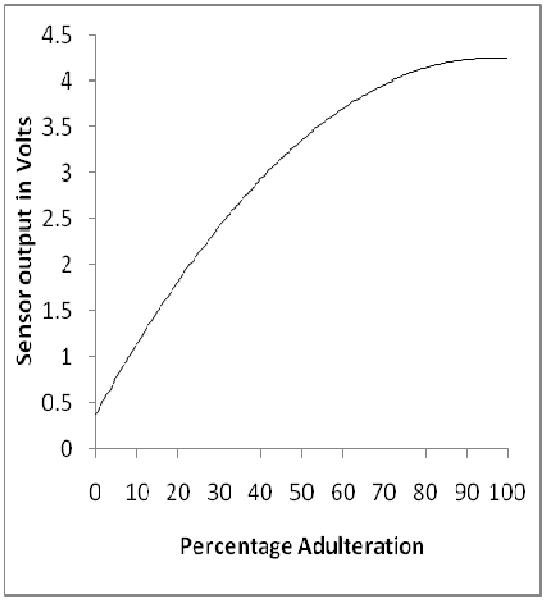


Figure 7 Experimental Results

## VI. CONCLUSION:

Fiber optic sensor probe is designed using multimode fibers which detect adulteration level in diesel by kerosene. This sensor is based on principle of refractive index variation due to variation in adulteration level. It shows significant variation in output voltage for different values of percentage adulteration. It is further tested for repeatability using T-tests. Distinct detection of adulteration levels is observed. This probe is used in two configurations one for in-situ measurement and other for laboratory measurement of adulteration level. For in-situ measurement, RED, YELLOW and GREEN indicators are used for showing no adulteration, adulterated with acceptable level and over adulterated fuel respectively. The configuration 2, designed for laboratory use shows actual value of adulteration percentage on the display unit. Though the observations are performed for 0-100% range of kerosene the adulteration of diesel will have significance on lower (approximately up to 30%) kerosene concentration side. The instrument shows nearly linear behavior in this region. This sensor probe can be used with appropriate modifications for other adulteration detection applications where the adulteration alters the refractive index of the specimen and has definite commercialization potential.

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# SYSTEM FOR DOCUMENT SUMMARIZATION USING GRAPHS IN TEXT MINING

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## *ABSTRACT*

*Summarization of text documents is increasingly important with the amount of data available on the Internet. The large majority of current approaches view documents as linear sequences of words and create query-independent summaries. However, ignoring the structure of the document degrades the quality of summaries. Furthermore, the popularity of web search engines requires query specific summaries. Here one method is used to create query-specific summaries by adding structure to documents by extracting associations between their fragments. This paper has practically implemented graph method for text mining and accordingly documents summary is generated. This system is developed using java programming language and ORACLE. Here text files are stored at particular drive and document graph of each text file is generated by using IR ranking algorithms. When input query is entered it is checked on document graph using summarization algorithm. Summary of matching text files will be displayed as an output. Various results are taken and this system can be implemented in desktop, network environment for accessing files within a short period of time .further new algorithm like top 1 expanding search algorithm can be added to improve the performance of this system.*

***KEYWORDS:*** *Query, Document summarization, Document Graph structure.*

## I. INTRODUCTION

Due to rapid growth of Electronic document there is a need for effective search algorithm.WWW contains so many electronic document and user want to retrieve it within short period of time. Text search and Document summarization are two essential technologies that complement each other. The importance of data/text mining and knowledge discovery is increasing in different areas like: telecommunication, credit card services, sales and marketing etc. Text mining is used to gather meaningful information from text and it includes tasks like Text Categorization, Text Clustering, Text Analysis and Document Summarization. Text Mining examines unstructured textual information in an attempt to discover structure and implicit meanings within the text.

This paper is mainly concentrating on the Document summarization for text mining. Summarization techniques will help us to reduce our access time while we are retrieving data from the internet. The summarization concept is mainly started on the principle of index of books. In books when person want to search particular topic he or she will refer index of book and then that point will be retrieved in the less time. Traditionally Query Summarization is based on the BOW (Bag of Words) approach, in which both the query and sentences are represented with word vectors. [3], this approach suffers from the shortcoming that it merely considers lexical elements (words) in the documents, and ignores semantic relations among sentences. Second way is Natural Language processing where input query is processed by reading each word of the file and then display paragraph which is matching with input query [1]. This is very difficult for the file which has huge amount of data. Text Summarization is the process of identifying the most salient information in a document. [4].In this paper we are referring Document Graph based summarization method for information retrieval and displaying the summary of that text file.

# II. RELATED WORK

## 2.1 Query Summarization Characteristic

**1.** The sentences included in the summary are required to be closely relevant to the query.

**2.** The performance of Query Summarization relies highly on accurate measurement of text similarity.

**3.** In Multi document summarization more than one document are present with huge number of Bag of Words.

**4.** Memory space is the thing where we want to concentrate for multiple documents.

**5.** Multi-document summaries are produced from multiple documents and they have to deal with three major problems:

I. recognizing and coping with redundancy;

II. Identifying important differences among documents;

III. Ensuring summary coherence.

## 2.2 Document Summarization

Due to the limitations in natural language processing technology, abstractive approaches are restricted to specific domains. In contrast, extractive approaches commonly select sentences that contain the most significant concepts in the documents. These approaches tend to be more practical. Recently various effective sentence features have been proposed for extractive summarization, Such as signature word, event and sentence relevance. Although encouraging results have been reported, most of these features are investigated individually. We argue that it is ineffective to identify sentence importance from a single point of view. Each sentence feature has its unique Contribution and combing them would be advantageous. Therefore we investigate combined sentence features for extractive summarization. [2]

Currently, most successful multi-document summarization systems [5] follow the extractive summarization framework. These systems first rank all the sentences in the original document set and then select the most salient sentences to compose summaries for a good coverage of the concepts. For the purpose of creating more concise and fluent summaries, some intensive post-processing approaches are also appended on the extracted sentences.

Two Summary Construction Methods are applied first one is Abstractive method where summaries produce generated text from the important parts of the documents and second is Extractive Method where summaries identify important sections of the text and use them in the summary as they are.

# III. SYSTEM ARCHITECTURE

For implementing graph based document summarization this paper follows following architecture.

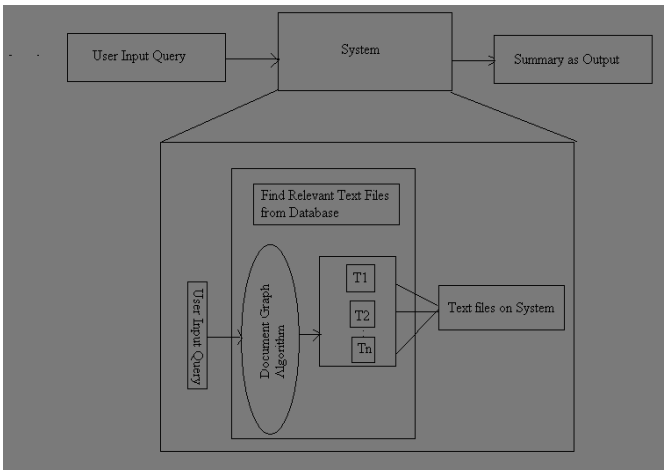


**Fig.1.1 Graph Based System Architecture for Query Specific Summarization**

Document graph is constructed with various phases. Initially all the stop words like (a, an, the, this, that, those, these, is, am, are, were) from all text files will be removed after that document is split into fragments using delimiter paragraph. Every text fragment will be considered as node for the graph. Weighted edge is added between two nodes if they are semantically related. Graph of each document is made. For minimizing the complexity of graph we are considering intermediate nodes with some threshold value. We have taken threshold value as 0.5. With different combination of nodes we are getting various spanning trees. Our work is to consider all combinations of spanning tree and calculate their score. Whichever spanning tree will generate smallest score that will be our summary.

Above fig shows document graph algorithm which is applied on text file i.e. T1, T2, Tn. system will show result as per user input query. To make a document graph and calculating the node weight IR ranking algorithm i.e. okapi [1] is referred which is based on tf-idf principle.

$$\sum_{t \in Q,d} \ln \frac{N - df + 0.5}{df + 0.5} \cdot \frac{(k_1 + 1)tf}{(k_1(1-b) + b\frac{dl}{avdl}) + tf} \cdot \frac{(k_3 + 1)qtf}{k_3 + qtf} \quad \text{……. .(1)}$$

tf: it is a term frequency in document.

qtf is term frequency in user input query.

N is the total number of documents in collection.

df is the number of documents that contains the query term.

dl is document length.

avdl is average document length.

K1 between 1.0-2.0,b is 0.75 and k3 is 0 to 1000. Consider k1, K2, k3 as constants.

Above formula is implemented through programming and nodes from text files are created.

### 3.1 Problem definition

Lets we have n document i.e.d1, d2, to dn. Size of document is total number of words. i.e.size (di).

Term frequency tf(d,w) is no of words present in documents.

Inverse document frequency is i.e.idf(w) Means inverse of documents contain word w in all documents.

Keyword query is set of words. i.e.Q(w1,w2…wn).

The document graph G(V,E) of a document d is defined as follows:

• d is split to a set of non-overlapping text fragments t(v),each corresponding to a node v€V.

• An edge e(u,v) €E is added between nodes u,v€V if there is an association between t(u) and t(v) in d.[1]

### 3.2 System Implementation

For implementation of this system we made various modules by using programming language JAVA. And for storing document graph ORACLE is used. Whole system is divided into various modules.1. Add Remove module 2.Stop Word Elimination Module 3.Document Graph Generation Module 4. Summary Module. This system is executed in the network environment so administrator rights are also considered to monitor the system.

Add Remove module is responsible for adding and removing various text files on the system. Stop word module will remove all the stop word from all the text files as well as from input query which is given to it. Document Graph Generation module will generate the document graph of each text file and that will be stored in ORACLE database. Document graph is generated only once and it is stored in database. If administrator wants to add new files or remove files then he or she want to execute all the modules from starting and make sure that by removing stop word all files nodes are stored inside the database. It means that whenever text files are added or removed from specific drive whole system should be run from the beginning to build a document graph of new files. Summary module will compare input user query with all documents graph and generates the summary.

On text file nodes are created by considering one paragraph as one node likewise all nodes are created for specified file. To make a connection between these nodes i.e. for making edges we are using following formula. [1]

$$EScore(e) = \frac{\sum_{w \in (t(u) \cap t(v))} \left( (tf(t(u), w) + tf(t(v), w)) \cdot idf(w) \right)}{size(t(u)) + size(t(v))} \quad \ldots\ldots\ldots \quad (2)$$

Summary module is referring the concept of spanning tree on the document graph because multiple nodes may have input query so which nodes will be selected? Different combinations from graph are identified and score is generated using following formula. [1]

$$\text{Score}(T) = a \sum_{edge\ e \in T} \frac{1}{EScore\ (e)} + b \frac{1}{\sum_{node\ v \in T} NScore\ (v)} \quad \ldots\ldots\ldots (3)$$

Given the document graph G and a query Q, a summary (sub tree of G) T is assigned a score Score (T) by combining the scores of the nodes v € T and the edges e € T. Where a and b are constants (we use a=1 and b=0.5), EdgeScore(e) is the score of edge e using equation 2, NodeScore(v) is the score of node v using Equation 1.

## IV. PRACTICAL EXAMPLE

Above fig1.1 shows a System for Document Summarization. User will input the query and system will display the summary of text files which are related to user query. We are showing how

summarization process works for text file. Here Fig 1.2 indicates a file which contains n number of paragraphs or sentences.

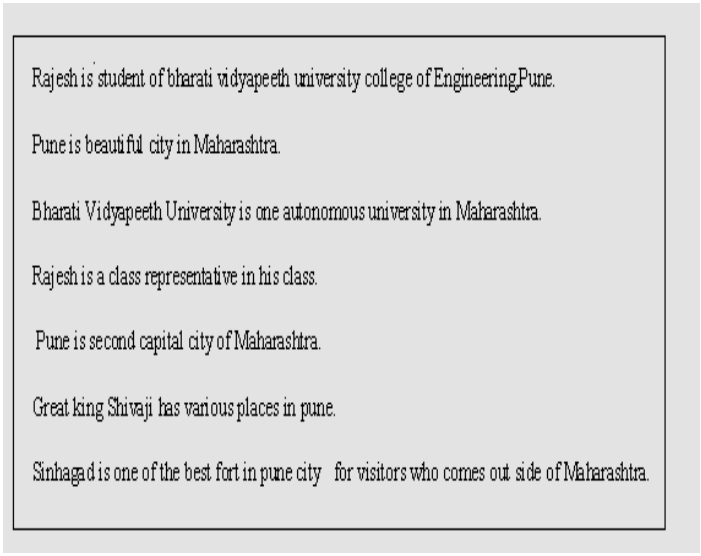


**Fig.1.2 Text File with N Paragraphs**

The Document graph for above file can be created by considering individual line as a single node and then edges can be connected by comparing two lines which have word similarity.Fig.1.3 shows Document Graph for above text file. Information Ranking Techniques are used for giving weights to edges.

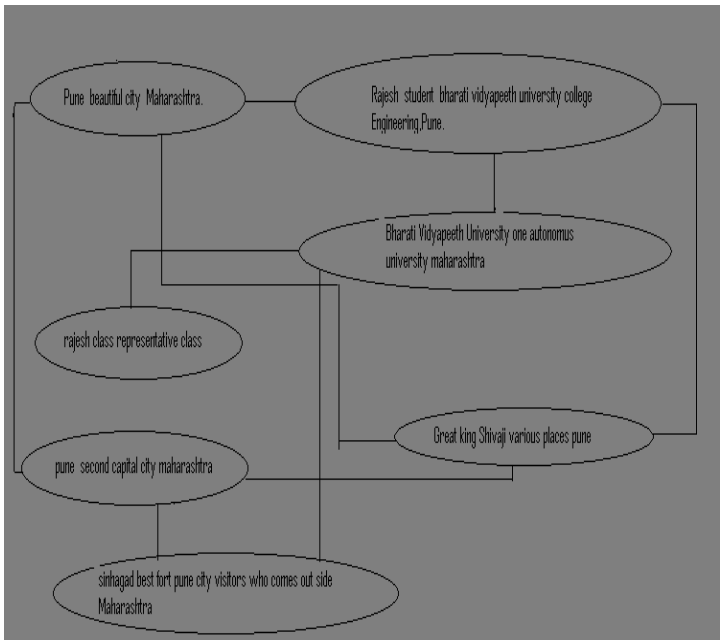


**Fig.1.3 shows Document Graph for above text file**

Suppose Query is **Pune city.**

Then this query is compared with all nodes and accordingly nodes will be selected which contains input query words. From above graph various combinations will be obtained. In text file we have total

seven lines so we are getting only seven nodes. Document graph is made using formula (1) and (2).score of each spanning tree is calculated using formula (3).

**After removing Stop words we get following result.**

Rajesh student bharati vidyapeeth university college Engineering, Pune.

Pune beautiful city Maharashtra.

Bharati Vidyapeeth University one autonomous university Maharashtra.

Rajesh class representative class.

Pune second capital city Maharashtra.

Great king Shivaji various places pune.

Sinhagad best fort pune city visitors who comes out side Maharashtra.

**Out Put**

**In this phase-I the nodes which has input query that sentences will be selected.**

**Phase-I Process**

Rajesh is student of bharati vidyapeeth university college of Engineering,Pune.

Pune is beautiful city in Maharashtra.

Great king Shivaji has various places in pune.

Sinhagad is one of the best fort in pune city for visitors who comes out side of Maharashtra.

In generating summary in final phase score of each spanning tree is calculated and which spanning tree is having less is displayed at first position likewise all spanning tree will be displayed in asending order with summary of text file.

**Output in final phase.**

Pune is beautiful city in Maharashtra.

Sinhagad is one of the best fort in pune city for visitors who comes out side of Maharashtra.

# V. EXPERIMENTAL RESULT

We have run above program on the system with Hardware configuration as follows.

Pentium Processor: –IV, Hard disk: 160 Gb, RAM Capacity: 1 Gb

Software requirement for implementation of above system is

Operating System: Windows XP, JDK 1.6, ORACLE 9 i

We have stored 57 text files in the database, the memory capacity required for these text files were 122 kb.

After running this program we get various results that are shown in table 1.0.

Following table shows the input query and result for the system. First query is “Network” this keyword is searched with all 57 files. Out of 57 files 11 files contains that keyword so that 11 text

files will be considered as documents for generating summary. Starting from first file system may get different paragraph with keyword "Network" .scores of each combination is calculated likewise all spanning tree combinations scores will be calculated for each file. Among these all document which spanning tree has minimum score that is displayed first. After running this system first summary score is displayed as 11.5044016. And time required for input query is 7 seconds. Score is mainly depending on size of file, number of files which are present in the database. Score are calculated using above equation and spanning tree algorithm. Table 1.0 indicates result for input query "Soft", "Software", "Computer", "System". In this fashion score for input query is calculated. If we use different information ranking formulas and TOP-1 expanding search algorithm definitely the time required for execution can be reduced.

| Query Keywords | No of file contains keyword | Output time In second | Score |
|---|---|---|---|
| Network | 11 | 7 | 11.5044016 |
| Soft | 1 | 6 | 100.744885 |
| Software | 11 | 8 | 3.6043922 |
| Computer | 22 | 9 | 3.9982438 |
| System | 24 | 6 | 3.3116584 |

**Table 1.0 Score of Input query**

# VI. CONCLUSION

Query Summarization using graph based algorithm techniques can be applied over internet, intranet and desktop systems for accessing various document files with short access time. Document Graph based algorithms are initially applied over all text files and user query is applied on this document graph so execution time is also reduced. These techniques can be applied with Google, MSN, Yahoo search engines and user waiting time for accessing document files can be reduced in the future by using top1 ranking algorithm performance of graph based systems can be improved.

## ACKNOWLEDGEMENTS

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# ADAPTIVE NEURO-FUZZY SPEED CONTROLLER FOR HYSTERESIS CURRENT CONTROLLED PMBLDC MOTOR DRIVE

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***ABSTRACT***

*The paper presents a methodology for developing adaptive speed controllers in a permanent-magnet brushless DC (BLDC) motor drive system. A proportional-integral controller is employed in order to obtain the controller parameters at each selected load. The resulting data from PI controller are used to train adaptive neuro-fuzzy inference systems (ANFIS) that could deduce the controller parameters at any other loading condition within the same region of operation. The ANFIS controller is tested at numerous operating conditions with hysteresis current controlled position determination. Paper also provides MATLAB developed PMBLDC motor model and simulation of PI speed controller in comparison with ANFIS controller. The BLDC motor drive system with PI controller exhibits higher overshoot and settling time when compared to the designed ANFIS controller.*

***KEYWORDS***

*PMBLDC Motor, adaptive Speed control, ANFIS.*

## I. INTRODUCTION

The Permanent Magnet Synchronous Motor (PMSM) has a sinusoidal back emf and requires sinusoidal stator currents to produce constant torque while the permanent magnet brushless dc (PMBLDC) motor has a trapezoidal back emf and requires rectangular stator currents to produce constant torque [1]. The system is becoming increasingly attractive in high-performance variable-speed drives since it can produce torque-speed characteristic similar to that of a permanent-magnet conventional dc motor while avoiding the problems of failure of brushes and mechanical commutation. The PMBLDC motor is becoming popular in various applications because of its high efficiency, high power factor, high torque, simple control and lower maintenance. BLDC motor is one type of synchronous motor, which can be operated in hazardous atmospheric condition and at high speeds due to the absence of brushes.

Pragasan Pillay and R.Krishnan in 1985-1990 [2]-[4] have investigated that the PMSM a sinusoidal back emf and requires sinusoidal stator currents to produce constant torque, while the BLDC motor has a trapezoidal back emf and motor requires rectangular stator current to produce constant torque. Bhim singh, B P singh and K Jain [5] have proposed a digital speed controller for BLDC motor and implemented in a digital signal processor (DSP). Later in 1998, the rotor position and the speed of permanent magnet have been estimated using Extended Kalman filter (EKF) by Peter Vas [6]. Jadric.M and Terzic .B [7] have proposed that the hall effect sensor are usually needed to sense the rotor position which senses the position signal for every 60 degree electrical. The mathematical model of the BLDC motor has been developed and validated in MATLAB platform with proportional-integral (PI) speed controller [8]. Host of efforts has attempted and solved the problem of non linearity and parameter variations of PMBLDC drive [9]-[13].

The draw-backs of Fuzzy Logic Control (FLC) and Artificial Neural Network (NN) can be over come by the use of Adaptive Neuro-Fuzzy Inference System (ANFIS) [18]-[19]. ANFIS is one of the best tradeoff between neural and fuzzy systems, providing: smooth control, due to the FLC interpolation and adaptability, due to the NN back propagation. Some of advantages of ANFIS are model compactness, require smaller size training set and faster convergence than typical feed forward NN. Since both fuzzy and neural systems are universal function approximators, their combination, the hybrid neuro-fuzzy system is also a universal function approximator. The non-linear mapping in a neuro-fuzzy network is obtained by using a fuzzy membership function based neural network.
Using the developed model of the BLDC motor, a detailed simulation and analysis of a BLDC motor speed servo drive is obtained. Closed loop control of PMBLDC motor drive consisting of PI speed controller and hysteresis current controller is simulated and later compared with the ANFIS controller.

## II. MODELLING OF PMBLDC MOTOR

Fig.1 describes the basic building blocks of the PMBLDCM drive. The drive consists of a speed controller, a reference current generator, a pulse width modulated (PWM) current controller, a position sensor, the motor and a current controlled voltage source inverter (CC-VSI). The speed of the motor is compared with its reference value and the speed error is processed in PI speed controller. The output of this controller sets the torque reference. A limit is put on the speed controller output depending on permissible maximum winding currents. The reference current generator block generates the three phase reference currents ($i_a$*, $i_b$*, $i_c$*) using the limited peak current magnitude decided by the controller and the position sensor. In addition to the PI speed controller, a hysteresis controller is employed for current control.

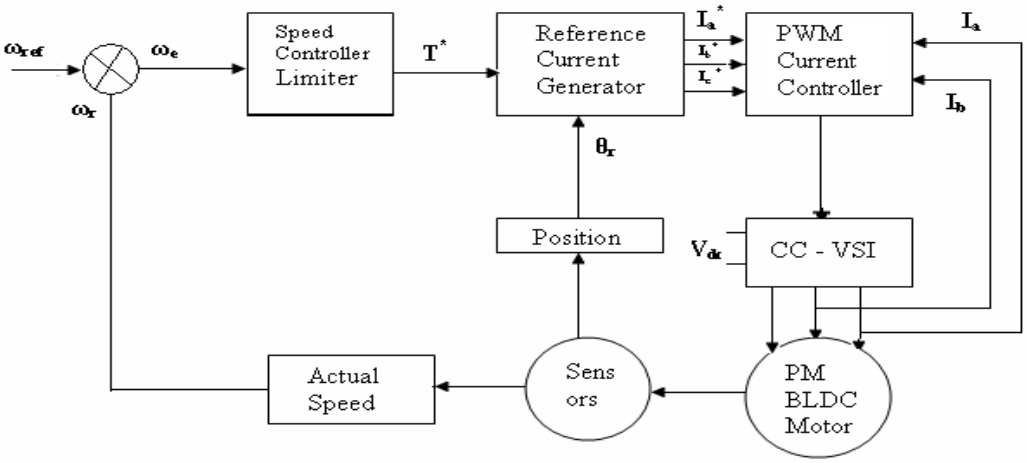


Fig. 1 Block Diagram of PMBLDC Motor Drive

The reference currents have the shape of quasi-square wave in phase with respective back emfs to develop constant unidirectional torque. The PWM current controller regulates the winding currents ($i_a$, ib, ic) within the small band around the reference currents ($i_a$*, ib*, $i_c$*). The motor currents are compared with the reference currents and the switching commands are generated to drive the inverter devices.
The PMBLDC motor is modeled in the three-phase abc frame. The general volt-ampere equation for the circuit shown in the Fig.2 can be expressed as:

$$V_{an} = Ri_a + p\lambda_a + e_{an} \quad (1)$$

$$V_{bn} = Ri_b + p\lambda_b + e_{bn} \quad (2)$$

$$V_{cn} = Ri_c + p\lambda_c + e_{cn} \quad (3)$$

Where, $V_{an}$, $V_{bn}$ and $V_{cn}$ are phase voltages and may be defined as:

$$\begin{aligned} V_{an} &= V_{a0} - V_{n0}, \\ V_{bn} &= V_{b0} - V_{n0}, \text{ and} \\ V_{c0} &= V_{c0} - V_{n0}. \end{aligned} \quad (4)$$

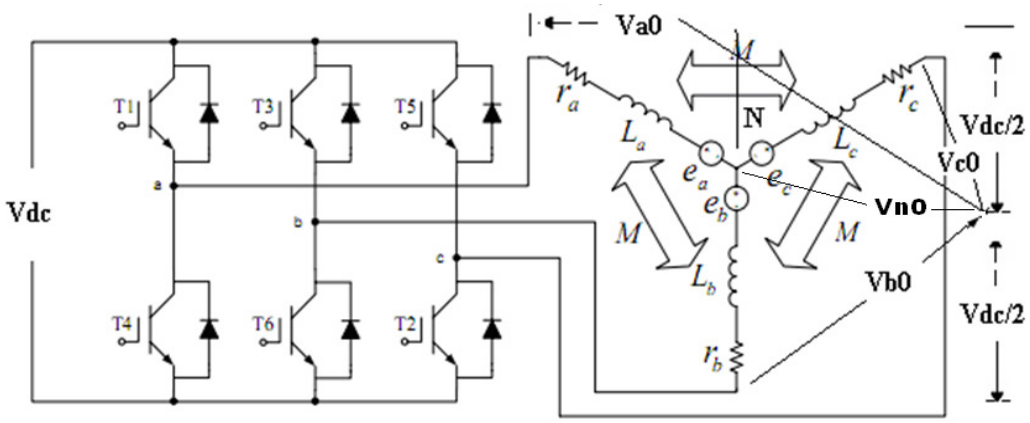


Fig.2 Inverter circuit with PMBLDC motor drive

The phase back emf $e_{an}$ can be expressed as

$$\begin{aligned} f_a(\theta_r) &= E & 0^0 < \theta_r < 120^0 \\ f_a(\theta_r) &= (6E/\pi)(\pi - \theta_r r) - E & 120^0 < \theta_r < 180^0 \\ f_a(\theta_r) &= -E & 180^0 < \theta_r < 300^0 \\ f_a(\theta_r) &= (6E/\pi)(\theta_r r - 2\pi) + E & 300^0 < \theta_r < 360^0 \end{aligned} \quad (5)$$

Where, $E = K_b \omega_r$ and $e_{an}$ can be described by E and normalized back emf function $f_a(\theta_r)$ $[e_{an} = E f_a(\theta_r)]$. Where $V_{a0}$, $V_{b0}$, $V_{c0}$ and $V_{n0}$ are three phase and neutral voltages with respect to the zero reference potential at the mid-point of dc link (0) shown in the Fig.2. R is the resistance per phase of the stator winding, p is the time differential operator, and $e_{an}$, $e_{bn}$ and $e_{cn}$ are phase to neutral back emfs. The $\lambda_a$, $\lambda_b$ and $\lambda_c$ are total flux linkage of phase windings a, b and c respectively. Their values can be expressed as:

$$\lambda_a = L_S i_a - M(i_b + i_c) \quad (6)$$

$$\lambda_b = L_S i_b - M(i_a + i_c) \quad (7)$$

$$\lambda_c = L_S i_c - M(i_a + i_b) \quad (8)$$

Where, '$L_s$' and 'M' are self and mutual inductances respectively.

The PMBLDC motor has no neutral connection and hence this results in,

$$i_a + i_b + i_c = 0 \quad (9)$$

Substituting (9) in (6), (7) and (8), the flux linkages are obtained.

$$\begin{aligned} \lambda_a &= i_a(L_S + M), \\ \lambda_b &= i_b(L_S + M), \text{and} \\ \lambda_c &= i_c(L_S + M) \end{aligned} \quad (10)$$

By substituting (10) in volt-ampere relations (1)-(3) and rearranging these equations in a current derivative of statespace form, gives,

$$pi_a = 1/(L_S + M)(V_{an} - Ri_a - e_{an}) \quad (11)$$

$$pi_b = 1/(L_S + M)(V_{bn} - Ri_b - e_{bn}) \quad (12)$$

$$pi_c = 1/(L_S + M)(V_{cn} - Ri_c - e_{cn}) \quad (13)$$

The developed electromagnetic torque may be expressed as

$$T_e = (e_{an} i_a + e_{bn} i_b + e_{cn} i_c)/\omega_r \quad (14)$$

Where, '$\omega_r$' is the rotor speed in electrical rad/sec. Substituting the back emfs in normalized form, the developed torque is given by

$$T_e = K\{f_a(\theta_r)i_a + f_b(\theta_r)i_b + f_c(\theta_r)i_c\} \quad (15)$$

The mechanical equation of motion in speed derivative form can be expressed as:

$$p\omega_r = (P/2)(T_e - T_L - B\omega_r)/J \quad (16)$$

Where, 'P' is the number of poles, '$T_L$' is the load torque in N-m, 'B' is the frictional coefficient in Nm/rad, and 'J' is the moment of inertia in kg-m$^2$. The derivative of the rotor position ($\theta_r$) in state space form is expressed as:

$$p\theta_r = \omega_r \quad (17)$$

The potential of the neutral point with respect to the zero potential ($v_{n0}$) is required to be interpreted properly to avoid the imbalance in applied phase voltages.

This can be obtained by substituting (4) in (1) to (3) and adding them together to give

$$V_{a0} + V_{b0} + V_{c0} - 3V_{n0} = R(i_a + i_b + i_c) + (L_S + M)(pi_a + pi_b + pi_c) + (e_{an} + e_{bn} + e_{cn}) \quad (18)$$

Substituting (9) in (18) results in

$$V_{a0} + V_{b0} + V_{c0} - 3V_{n0} = (e_{an} + e_{bn} + e_{cn})$$
$$\Rightarrow V_{n0} = [V_{a0} + V_{b0} + V_{c0} - (e_{an} + e_{bn} + e_{cn})]/3 \quad (19)$$

The set of differential equations viz. (11),(12), (13), (16) and (19) defines the developed model in terms of the variables $i_a$, $i_b$, $i_c$, $\omega_r$, and $\theta_r$ for the independent variable, time.

# III. SPEED CONTROL

## 3.1 PI Controller

PI controller is widely used in industry due to its ease in design and simple structure. The rotor speed $\omega_{r(n)}$ is compared with the reference speed $\omega_{r(n)}*$ and the resulting error is estimated at the nth sampling instant as :

$$\omega e(n) = \omega r(n)* - \omega r(n) \quad (20)$$

The new value of torque reference is given by:

$$T_{(n)} = T_{(n-1)} + K_p\{\omega_{e(n)} - \omega_{e(n-1)}\} + K_1\{\omega_{e(n)}\} \quad (21)$$

Where $\omega_{e(n-1)}$ is the speed error of previous interval, and $\omega_{e(n)}$ is the speed error of the working interval. $K_p$ and $K_1$ are the gains of PI speed controller. By using Ziegler Nichols method the $K_p$ and $K_I$ values are determined.

## 3.2 ANFIS Controller

In this section basics of ANFIS and development of ANFIS controller are given. ANFIS uses the neural network's ability to classify data and find patterns. It then develops a fuzzy expert system that is more transparent to the user and also less likely to produce memorization error than a neural network. ANFIS keeps the advantages of a fuzzy expert system, while removing (or at least reducing) the need for an expert. The problem with ANFIS design is that large amounts of training data require developing an accurate system. The ANFIS, first introduced by Jang in 1993, is a universal

approximator and, as such, is capable of approximating any real continuous function on a compact set to any degree of accuracy [14]-[16]. ANFIS is a method for tuning an existing rule base with a learning algorithm based on a collection of training data. This allows the rule base to adapt.

As a simple example, a fuzzy inference system with two inputs x and y and one output z is assumed. The first-order Sugeno fuzzy model, a typical rule set with two fuzzy If–Then rules can be expressed as [17]:

Rule 1: If x is $A_1$ and y is $B_1$, then $f_1=p_1x+q_1y+r_1$

Rule 2: If x is $A_2$ and y is $B_2$, then $f_2=p_2x+q_2y+r_2$

The resulting Sugeno fuzzy reasoning system is shown in Fig. 3. Here, the output $z$ is the weighted average of the individual rules outputs and is itself a crisp value. The corresponding ANFIS architecture is shown in Fig. 4. If the firing strengths of the rules are $w_1$ *and* $w_2$, respectively, for the particular values of the inputs $A_i$ and integral of $B_i$, then the output computed as weighted average,

$$f = \frac{w_1 f_1 + w_2 f_2}{w_1 + w_2} \tag{22}$$

Let the membership functions of fuzzy sets $A_i$ and $B_i$, are $\mu_{Ai}$ and $\mu_{Bi}$ .

***Layer 1:*** Each neuron "i" in layer 1 is adaptive with a parametric activation function. Its output is the grade of membership function; an example is the generalized bell shape function.

$$\mu(x) = \frac{1}{1 + \left[\frac{x-c}{a}\right]^{2b}} \tag{23}$$

Where [a,b,c] is the parameter set. As the values of the parameters change, the shape of the bell-shape function varies.

***Layer 2:*** .Every node in layer 2 is a fixed node, whose output is the product of all incoming signals.

$$W_i = \mu_{Ai}(x)\, \mu_{Bi}(y),\ i=1,2 \tag{24}$$

***Layer 3:*** This layer normalizes each input with respect to the others (The $i^{th}$ node output is the $i^{th}$ input divided the sum of all the other inputs).

$$\bar{w}_i = \frac{w_i}{w_1 + w_2} \tag{25}$$

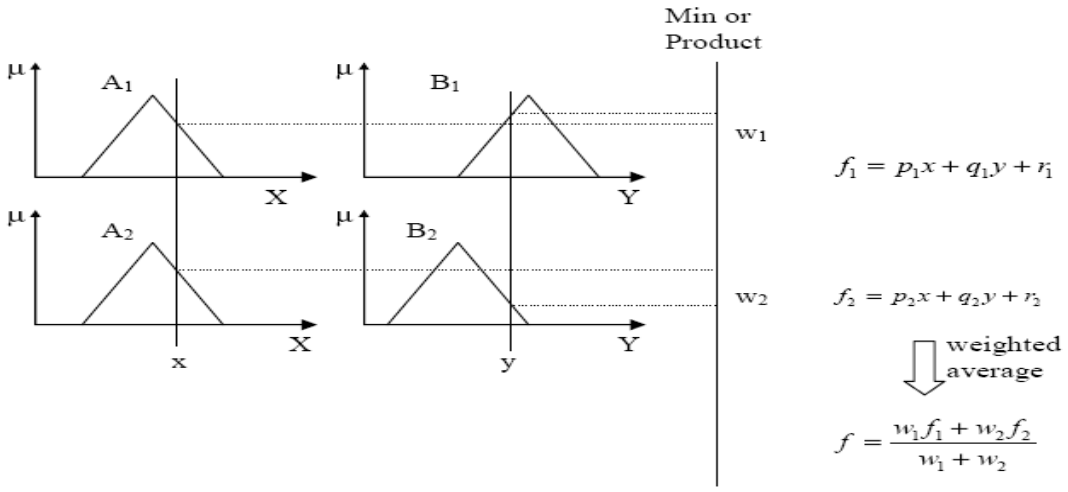


Fig.3 Two-input first-order Sugeno fuzzy model with two rules

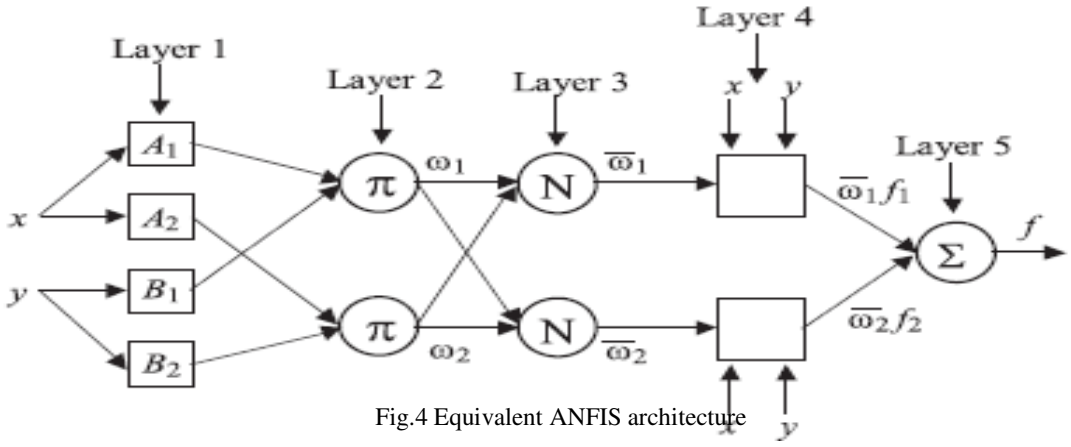


Fig.4 Equivalent ANFIS architecture

***Layer 4:*** This layer's *ith* node output is a linear function of the third layer's *ith* node output and the ANFIS input signals.

$$\bar{w}_i f_i = \bar{w}_i (p_i x + q_i y + r_i) \tag{26}$$

***Layer 5:*** This layer sums all the incoming signals.

$$f = \bar{w}_1 f_1 + \bar{w}_2 f \tag{27}$$

### 3.3 Reference Current Generator

The magnitude of the three phase current (I*) is determined by using reference torque (T*) and the back emf constant ($K_b$) as $I^* = T^* / K_b$. Depending on the rotor position, the reference current generator block generates three-phase reference currents ($i_a^*$, $i_b^*$, $i_c^*$) by taking the value of reference current magnitude as I*, − I* and zero. The reference current generation is detailed in Table 1.

**Table 1 Reference Current Generation**

| Rotor Position Signal | Reference Currents | | |
|---|---|---|---|
| | $I_a^*$ | $I_b^*$ | $I_c^*$ |
| 0° - 60° | I* | -I* | 0 |
| 60° - 120° | I* | 0 | -I* |
| 120° - 180° | 0 | I* | -I* |
| 180° - 240° | -I* | I* | 0 |
| 240° - 300° | -I* | 0 | I* |
| 300° - 360° | 0 | -I* | I* |

### 3.4. PWM Current Controller

The PWM current controller contributes to the generation of the switching signals for the inverter devices. The switching logic is formulated as given below.

If $i_a < (i_a^*)$ switch 1 ON and switch 4 OFF

If $i_a > (i_a^*)$ switch 1 OFF and switch 4 ON

If $i_b < (i_b^*)$ switch 3 ON and switch 6 OFF

If $i_b > (i_b^*)$ switch 3 OFF and switch 6 ON

If $i_c < (i_c^*)$ switch 5 ON and switch 2 OFF

If $i_c > (i_c^*)$ switch 5 OFF and switch 2 ON

## IV. SIMULATION RESULTS

In this section the set of equations representing the model of the drive system developed in section 2 is simulated with PI Speed controller. The results are observed for the motor presented in Appendix (3 phase, 2.0 hp, 4- pole 1500 rpm, 4 A) using developed Simulink model in MATLAB. Figure 5-11 show simulated results for the transient and steady state responses for PI controller.

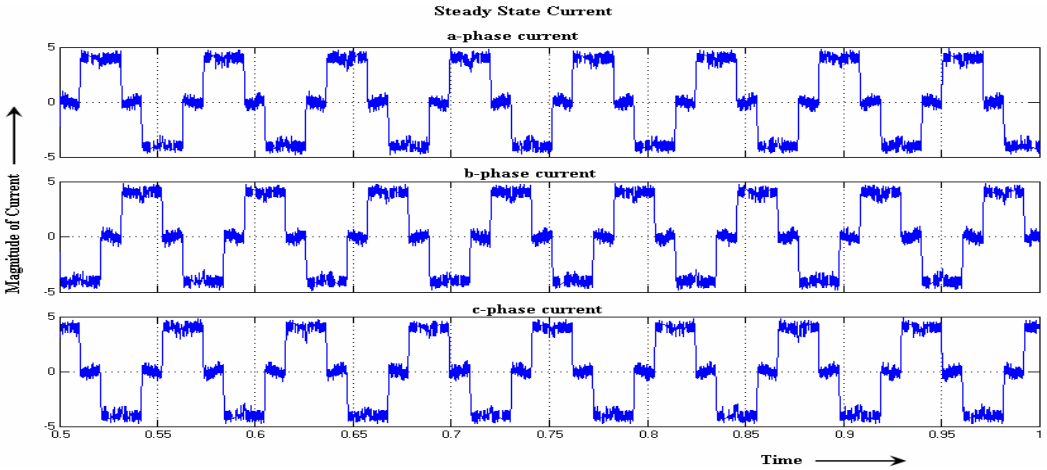


Fig.5 Stator Current of BLDC Motor.

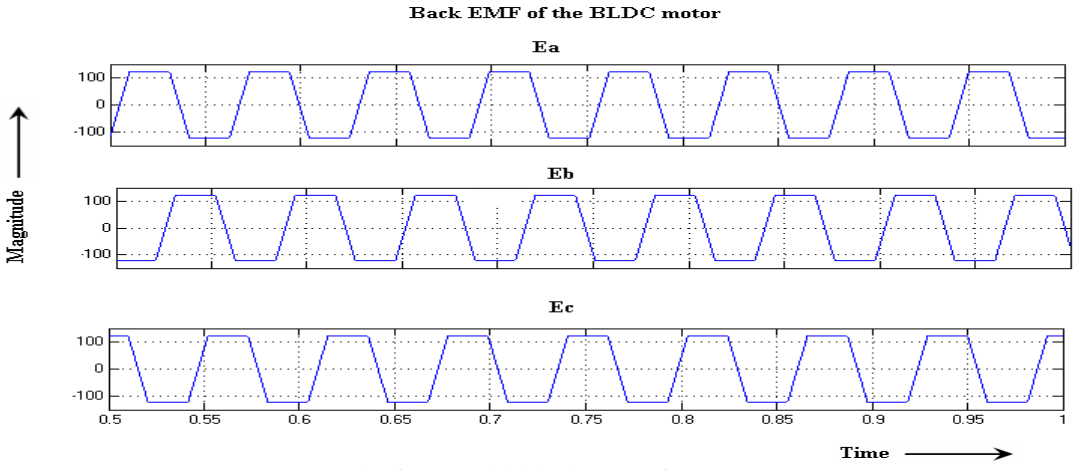


Fig. 6 Trapezoidal back EMF of BLDC Motor

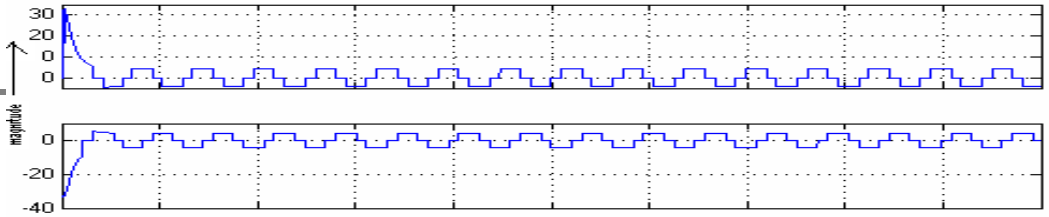

Fig. 7 Reference Current Waveform of BLDC Motor

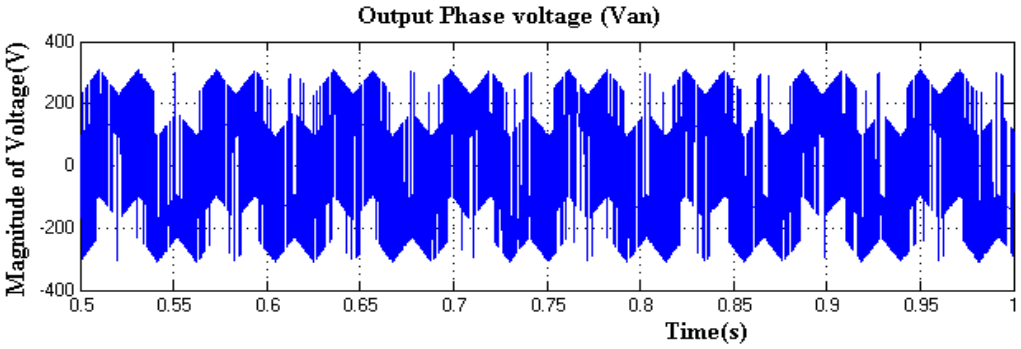


Fig. 8 Phase voltage ($v_{an}$)

The shapes of the simulated current and back emf validate the accuracy of the developed model. In Fig.9 shows the Torque and Speed waveforms for moment of inertia 0.013kg-m$^2$. It reaches the steady state torque and speed suddenly at time 0.03seconds. From these figures it is inferred that increasing the moment of inertia ploys an important role in settling time.

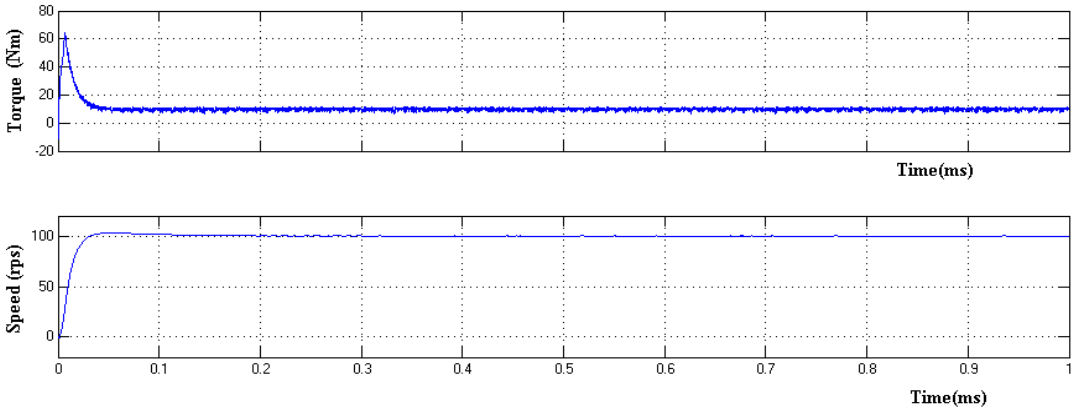


Fig. 9 Torque and Speed Waveforms when moment of inertia =0.013 kg-m$^2$

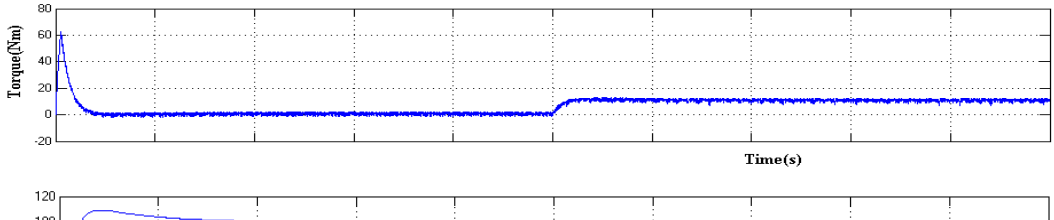

Fig. 10 Torque and speed waveforms for Step Change in Moment of Inertia at 0.5sec.

Fuzzy membership functions can take many forms, but simple straight-line functions are often preferred. Triangular membership functions are often selected for practical applications and different membership functions are tried for the minimum mean root square errors (MRSE). A set of modified membership functions were derived through training the ANFIS by using data obtained from PI controller as illustrated in Fig.11 and Fig.12.
ANFIS controller is designed with two inputs (speed error and change in speed error) and one output and shown in Fig.13. Fig.14 shows the stator currents awhile Fig.15 and Fig.16 show the torque and speed responses respectively for ANSFIS controller.

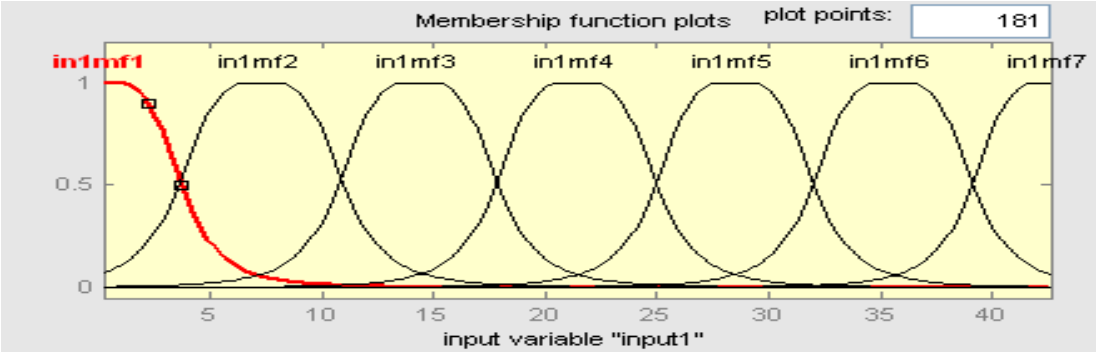


Fig.11. Membership Functions Obtained After Training for Speed Error

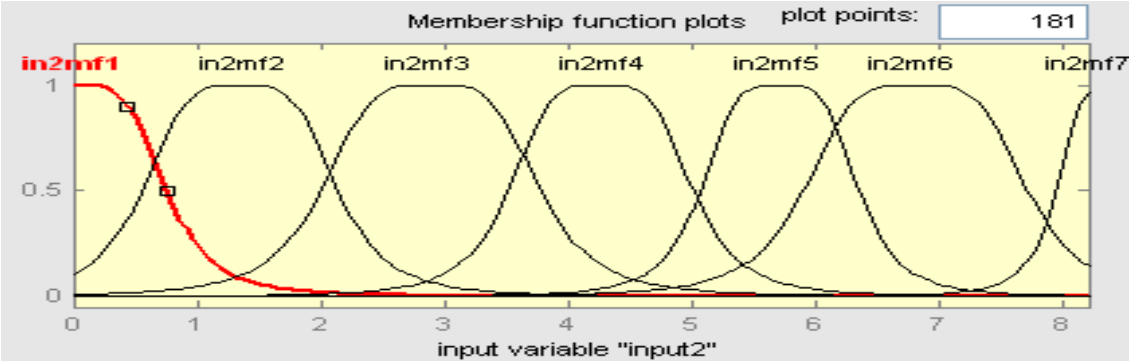


Fig.12. Membership Functions Obtained After Training for Change in Speed Error

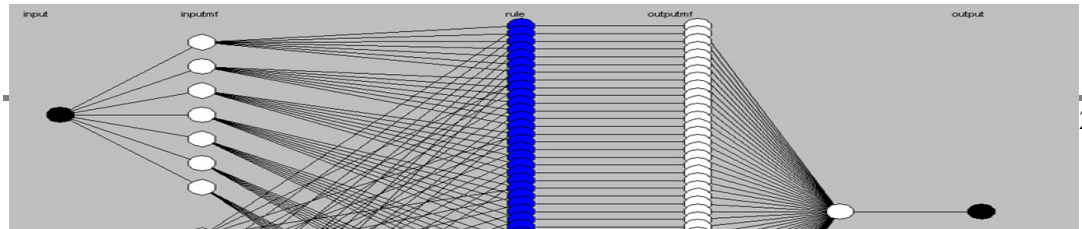

Fig.13. Architecture of ANFIS

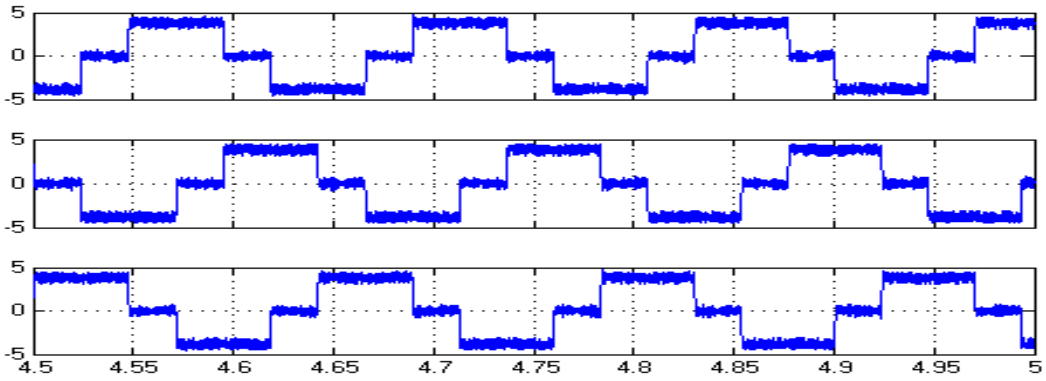


Fig. 14 Stator Current ANFIS controller**.**

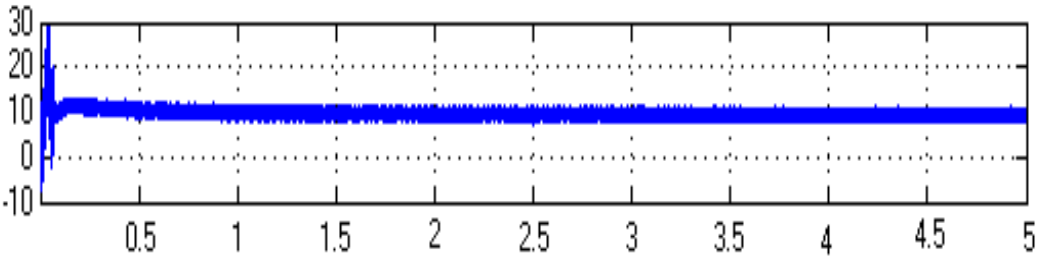


Fig. 15 Torque Response -ANFIS Controller

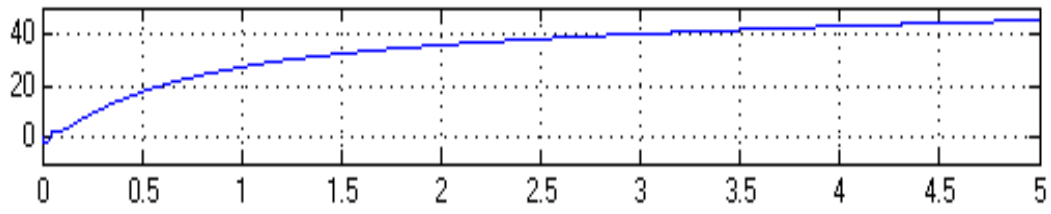


Fig. 15 Speed Response – ANFIS Controller

## V. CONCLUSION

ANFIS served as a basis for constructing a set of fuzzy if-then rules with appropriate membership functions to generate the stipulated input-output pairs. The performance of the developed MATLAB based speed controller of the drive has revealed that the algorithms developed to analyze the behavior of the PMBLDC motor drive system work satisfactorily in software implementation. Using neuro-fuzzy controller error can be reduced and train the membership functions to get the improved speed characteristics. It is found that the ANFIS controller shows reduced overshoot and settling time in both start-up and loaded change conditions and hence robust response.

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# APPENDIX

| | |
|---|---|
| Rating: | 2.0 hp |
| Number of Poles: | 4 |
| Type of connection: | Star |
| Rated speed: | 1500 rpm |
| Rated current: | 4A |
| Resistance/phase: | 2.8 Ω |

Back EMF constant: 1.23V sec/rad
Inductance (Ls + M): 0.00521 H/phase
Moment of Inertia: 0.013 Kg-$m^2$

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# A MODIFIED HOPFIELD NEURAL NETWORK METHOD FOR EQUALITY CONSTRAINED STATE ESTIMATION

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***ABSTRACT***

*Electric power system is a highly complex and non linear system. Its analysis and control in real time environment requires highly sophisticated computational skills. Computations are reaching a limit as far as conventional computer based algorithms are concerned. It is therefore required to find out newer methods which can be easily implemented on dedicated hardware. It is a very difficult task due to complexity of the power system with all its interdependent variables, thus making the neural networks one of the better options for the solution of different issues in operation and control. In this project an attempt has been made to implement ANN's for State Estimation. A Hopfield neural network model has been developed to test Topological Observability of Power System and it is tested on two different test systems. The results so obtained, are comparable with those results of conventional root based observability determination technique. Further a Hopfield model has been developed to determine State Estimation of power system. State Estimation of 6 bus and IEEE 14 bus system is attempted using this Hopfield neural network.*

***KEYWORDS*****:** *State Estimation, Hopfield neural network, Observability, Electrical power systems, conventional algorithms.*

## I. INTRODUCTION

State Estimation processes a set of measurements to obtain the best estimate of the current state of the power system. The set of measurements includes telemetered measurements and pseudo-measurements. Telemetered measurements are the online telemetered data of bus voltages, line flows, injections, etc. Pseudo-measurements are manufactured data such as guessed MW generation or substation load demand based on historical data, in most cases. Telemetered measurements are subject to noise or error in metering, communication system, etc. The errors of some of the pseudo-measurements, especially the guessed ones, may be large. However, there is a special type of pseudo-measurements, known as the zero injections, for which the information contains no error. Zero injection occurs at a node, for example, representing a switching station where the power injection is equal to zero. Zero injection is an inherent property of such a node and no meter need to be installed but the information is always available. A state estimation algorithm must compute estimates, which satisfy exactly such constraints, independent of the quality of online measurements. The enforcing of constraints is in particular useful in networks, consisting of large unobservable parts of network or having very low measurement redundancy.

In its conventional form, the Weighted Least Square method does not enforce the equality and limit constraints explicitly. However, the constraints contain reliable information about physical restrictions and equipment limits and can be used to increase the quality of state estimation result. The zero

injections can be represented by a set of equalities. Various methods have been proposed to process constraints, literature review section lists some of the proposed methods for solving equality constrained State Estimation problem.

Various algorithms of State Estimation using the conventional computer are reaching a limit as far as the solution techniques are concerned, and as long as these computer based algorithms are used, faster methods cannot be expected. However for security monitoring and control in power system, improvement in calculation time is always desired in order to obtain necessary information more quickly and accurately.

In recent years, it has been found that Artificial Neural Networks (ANN's) are well suited as computational tools for solving certain classes of complex problems, although software implementations of the algorithm on general-purpose computers can be too slow for time-critical applications, but the small number of computational 'primitives', suggests advantages of hosting ANN's on dedicated Neural Network Hardware (NNH) to maximize performance at a given cost target. ANN computations may be carried out in parallel, and special hardware devices are being designed and manufactured which take advantage of this capability.

In this chapter a new method for enforcing equality and limit constraints in State Estimation algorithm using a modified Hopfield neural network is presented. This method is tested for 6 bus system and IEEE 14 bus system. The main advantages of using the modified Hopfield neural network proposed in this work are

- The internal parameters of the network are explicitly obtained by the valid-subspace technique of solutions
- Lack of need for adjustment of penalty factors for initialization of constraints
- For real time application, the modified Hopfield network offers simplicity of implementation in analog hardware or a neural network processor
- Training and testing of the neural network under human supervision is not required.

# II. STATE ESTIMATION WITH CONSTRAINTS

State vector of an electric network consists of the complex voltages at the buses. Unmeasured tap positions of transformers may also be included into the state vector. A measurement vector consists of power flows, power injections, voltage and current magnitudes and tap positions of transformers. For a N bus system, the state vector $X=[\delta,V]^T$, of dimension n=2N-1, consists of the N-1 bus voltage angles $\delta_i$ with respect to a reference bus and the N bus voltage magnitudes $V_i$ for i=1,2,3,....N.

The static state estimator measurement model is given as:

$$z=h(X)+\epsilon \quad \ldots (1)$$

Where z is the measurement vector, h(.) is a vector of nonlinear functions, relating the measurement and state vectors, and $\epsilon$ is the vector of measurement errors.

The error-free data are modeled as equality constraints

$$g(X)=0 \quad \ldots (2)$$

Limits on some network variables are modeled as inequality constraints which can be expressed in a compact form by p-dimensional functional inequalities

$$f(x)\leq 0 \quad \ldots (3)$$

General nonlinear programming algorithms for the solution of a constrained minimization problem [2] are not efficient enough for the on-line application. Hence a neural network approach is used for solving this nonlinear programming problem.

## 2.1. Objective function

The objective is to minimize the weighted squared mismatch between measured and calculated quantities. Considering system to be observable and with m>n , where m is the total number of measurements and n is the number of state variables , the mathematical problem is given as follows:

$$\min \frac{1}{2}[Z-h(X)]^T R^{-1}[Z-h(X)] \quad \ldots (4)$$

Subject to the equality and inequality constraints as defined below. The diagonal matrix $R^{-1}$

represents the weights of the individual measurements in the objective function.

### 2.2. Equality constraints

Power flow equations, corresponding to both real and reactive power balance are the equality constraints for all the buses characterized as zero injections, which can be expressed as follows:.

$$P_i=\sum_{m=1}^{N_b} V_i V_m (g_{im}\cos\delta_{im}+b_{im}\sin\delta_{im})=0 \quad \dots (5) \qquad Q_i=\sum_{m=1}^{N_b} V_i V_m (g_{im}\sin\delta_{im}-b_{im}\cos\delta_{im})=0 \quad \dots (6)$$

For i ∈ ( set of zero injection buses)

Where

$P_i$ = Real power injection at bus-i
$Q_i$ = Reactive power injection at bus-i
$V_i$ = Voltage magnitude at bus-i
$\delta_i$ = Load angle at bus-i
$Y_{ij} = g_{ij}+b_{ij}$=i-j$^{th}$ element of Y-bus Matrix.

$N_b$, $N_l$, $N_g$=number of total buses, load buses and generator buses in the system respectively.

### 2.3. Inequality Constraints:

(i) Voltage Limit: This includes upper ($V_i^{max}$) and lower ($V_i^{min}$ ) limits on the bus voltage magnitude.

$$V_i^{min} \le V_i \le V_i^{max} \qquad i=1,2,.....N_b \qquad \dots (7)$$

(ii) Phase Angle Limits: The phase angle at each bus should be between lower ($\delta_i^{min}$) and upper ($\delta_i^{max}$) limits.

$$\delta_i^{min} \le \delta_i \le \delta_i^{max} \qquad i=1,2,.....N_b \qquad \dots (8)$$

These limits may vary depending upon the problem under consideration. Imposing phase angle limits at load buses is another way of limiting the power flow in the transmission lines and for generator buses this limiting is done for stability reasons. Along with the above two constraints the following constraints can also be imposed.

(a) Line Flow Limit, representing the maximum power flow in a transmission line and is usually based on thermal and dynamic stability considerations. Let $P_{Li}^{max}$ be the maximum active power flow in line-*i* respectively. The line flow limit can be written as

$$P_{Li}^{max} \ge P_{Li} \qquad i=1,2,.....N_L \qquad \dots (9)$$

(b) Reactive Power Generator Limit: Let $Q_{gi}^{min}$ and $Q_{gi}^{max}$ are the minimum and maximum reactive power generation limit of the reactive source generators ($N_g$) respectively.

$$Q_{gi}^{min} \le Q_{gi} \le Q_{gi}^{max} \qquad i=1,2,.....N_g \qquad \dots (10)$$

## III. THE MODIFIED HOPFIELD NEURAL NETWORK

Artificial neural networks attempt to achieve good performance via dense interconnection of simple computational elements. Hopfield networks [1] are single-layer networks with feedback connections between nodes. In the standard case, the nodes are fully connected. The node equation for the continuous-time network with n-neurons is given by:

$$u_i(t)=-\eta.u_i(t)+\sum_{j=1}^{n} T_{ij}.v_j(t)+i_i^b \qquad \dots (11)$$

$$v_i(t) = g(u_i(t)) \qquad \dots (12)$$

Where $u_i(t)$ is the current state of the $i^{th}$ neuron, $v_j(t)$ is the output of the $j^{th}$ neuron., $i_i^b$ is the offset bias of the $i^{th}$ neuron., $\eta.u_i(t)$ is the passive decay term, and $T_{ij}$ is the weight connecting the $j^{th}$ neuron to $i^{th}$ neuron. In Eqn. (12), $g(u_i(t))$ is a monotonically increasing threshold function that limits the output of each neuron to ensure that network output always lies in or within a hypercube. It is shown in [3] that the equilibrium points of the network correspond to values of v(t) for which the energy function associated with the network is minimized:

$$E(t)=-\frac{1}{2}v(t)^T.T.v(t)-v(t)^T.i^b \qquad \ldots (13)$$

Mapping of constrained nonlinear optimization problems using a Hopfield network consists of determining the weight matrix T and the bias vector $i^b$ to compute equilibrium points. Some mapping techniques codes the validity constraints as terms in the energy function which are minimized when the constraints ($E^{cons}_i = 0$) are satisfied :

$$E(t)=E^{op}(t)+b_1.E^{cons_1}(t)+b_2.E^{cons_2}(t)+.... \qquad \ldots (14)$$

Where $E^{op}(t)$ represents the objective function to be optimized and $E^{cons}$ represents the constraints of the problem. The $b_i$ parameters in Eqn. (14) are constant weightings given to various energy terms. The multiplicity of terms in the energy function tends to frustrate one another, and success of the network is highly sensitive to the relative values of $b_i$ .It has been shown in [3] that the $E^{op}$ and $E^{cons}$ terms in Eqn. (14) can be separated into different subspaces so that they no longer frustrate one another. A modified energy function E'(t) can be defined as follows:

$$E'(t) = E^{conf}(t) + E^{op}(t) \qquad \ldots (15)$$

Where $E^{conf}(t)$ is a confinement term that groups all the constraints imposed by the problem, and $E^{op}(t)$ is an optimization term that conducts the network output to the equilibrium points. Thus, the minimization of E'(t) of the modified Hopfield network is conducted in two stages:

1): minimization of the term $E^{conf}(t)$ :

$$E^{conf}(t)=-\frac{1}{2}v(t)^T.T^{conf}.v(t)-v(t)^T.i^{conf} \qquad \ldots (16)$$

Where: v(t) is the network output, $T^{conf}$ is weight matrix and $i^{conf}$ is bias vector belonging to $E^{conf}(t)$.

2): minimization of the term $E^{op}(t)$ :

$$E^{op}(t)=-\frac{1}{2}v(t)^T.T^{op}.v(t)-v(t)^T.i^{op} \qquad \ldots (17)$$

Where: $T^{op}$ is weight matrix and $i^{op}$ is bias vector belonging to $E^{op}$. This minimization moves v(t) towards an optimal solution (the equilibrium points).

Thus, the operation of the modified Hopfield network can be summarized as combination of three main steps, as shown in Fig. 1:

**Step (1)**: Minimization of $E^{conf}$ Corresponding, to the projection of v(t) in the valid subspace defined by [4,5]:

$$v(t)=T^{conf}.v(t)+i^{conf} \qquad \ldots (18)$$

Where: $T^{conf}$ is a projection matrix such that $T^{conf}.T^{conf}=T^{conf}$ and $i^{conf}$ is defined such that $T^{conf}.i^{conf}=0$. This operation corresponds to an indirect minimization of $E^{conf}(t)$.

**Step (2):** Application of a nonlinear 'symmetric ramp' activation function constraining v(t) in a hypercube

$$g_i(v_i) = v^{min} \quad \text{if} \quad v^{min} > v_i$$

$$= v_i \quad \text{if} \quad v^{min} \le v_i \le v^{max}$$

$$= v^{max} \quad if \quad v_i > v^{max}$$

Where $v_i \in [\ v^{min}, v^{max}\ ]$

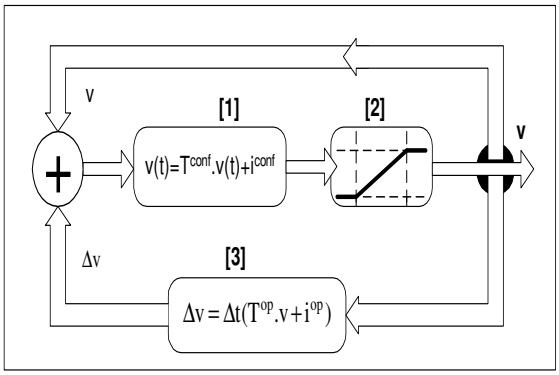


Figure-1: Modified Hopfield Neural Network

**Step (3):** Minimization of $E^{op}$, which involves updating of v(t) so as to direct it to an optimal solution (defined by $T^{op}$ and $i^{op}$) corresponding to network equilibrium points, which are the solutions for the constrained optimization problems. Using the symmetric ramp activation function and $\eta = 0$, Eqn. (12) becomes.

$v(t)=g(u(t))=u(t)$

Comparing Eqn. (11) and Eqn. (16),

$$\frac{dv}{dt} = \dot{v} = -\Delta t.\tilde{N}E^{op}(v) = \Delta t(T^{op}.v + i^{op}) \quad \Delta v = \Delta t.\dot{v} \quad \ldots (19)$$

Therefore, minimization of $E^{op}$ consists of updating v (t) in the opposite direction to the gradient of $E^{op}$. Each iteration has two distinct stages. First, as described in Step (iii) v is updated using the gradient of the term $E^{op}$ alone. Second, after each updating, v is directly projected in the valid subspace. In the next section, the parameters $T^{conf}$, $i^{conf}$, $T^{op}$ and $i^{op}$ are defined.

## IV. FORMULATION OF STATE ESTIMATION PROBLEM BY MODIFIED HOPFIELD NETWORK METHOD

Consider the following nonlinear optimization problem:

**Minimize**

$$E^{op}(X) = f(x) = \frac{1}{2}[Z-h(X)]^T R^{-1}[Z-h(X)] \quad \ldots (20)$$

Where X= [δ,V], z =measurement vector and h(X) represent nonlinear relationship between state vector x and z,

**Subject to** $E^{conf}(X)$: $h_i(X) = 0$,

i.e $P_i=0$ and $Q_i=0$ … (21)

For i∈ (buses identified as zero injections)

$$V^{min} \le V \le V^{max}$$

$$\delta^{min} \le \delta \le \delta^{max} \quad \ldots (22)$$

Where V, $V^{min}$, $V^{max}$, δ, $\delta^{max}$, $\delta^{min} \in R^n$; and all first and second order partial derivatives of f(X) and $h_i(X)$ exist and are continuous. The conditions in Eqn.( 21) and (22) define a bounded convex polyhedron. The vector x must remain within this polyhedron if it is to represent a valid solution for the optimization problem (Eqn.20). However if inequality constraints are also present, they must be transformed into equality constraints by introducing a slack variable $s_w$ for each inequality constraints prior to calculating the parameters $T^{conf}$ and $i^{conf}$. It is to be noted here that $E^{op}$ does not depend on the slack variables $s_w$. A projection matrix to the system can be shown as [6].

$$T^{conf} = [I - \nabla h(X)^T.(\nabla h(X).\nabla h(X)^T)^{-1}.\nabla h(X)] \quad \ldots (23)$$

where

$$\nabla h(X) = \begin{bmatrix} \frac{\partial h_1(X)}{\partial x_1} & \frac{\partial h_1(X)}{\partial x_2} & \cdots & \frac{\partial h_1(X)}{\partial x_N} \\ \frac{\partial h_2(X)}{\partial x_1} & \frac{\partial h_2(X)}{\partial x_2} & \cdots & \frac{\partial h_2(X)}{\partial x_N} \\ \vdots & \vdots & \cdots & \vdots \\ \frac{\partial h_p(X)}{\partial x_1} & \frac{\partial h_p(X)}{\partial x_2} & \cdots & \frac{\partial h_p(X)}{\partial x_N} \end{bmatrix} \quad \ldots (24)$$

Inserting the value of $T^{conf}$ from Eqn. (23) into Eqn. (18).

$$X = [I - \nabla h(X)^T.(\nabla h(X).\nabla h(X)^T)^{-1}.\nabla h(X)].X + i^{conf} \quad \ldots (25)$$

By the definition of the Jacobian, when X leads to equilibrium point h(X) may be approximated as follows:

$$H(X) \approx h(Xc) + J.(X - Xc) \quad \ldots (26)$$

where $J = \nabla h(X)$

In the proximity of the equilibrium point Xc=0,

$$\lim_{v \to vc} \frac{\|h(X)\|}{\|X\|} = 0 \quad \ldots (27)$$

Finally from Eqns. (25-27), X can be written as

$$X = X - \nabla h(X)^T.((\nabla h(X).\nabla h(X)^T)^{-1}).h(X) \quad \ldots (28)$$

Parameters $T^{op}$ and $i^{op}$ in this case are such that the vector X is updated in the opposite gradient direction of the energy function $E^{op}$. Since Eqns. (21) and (22) define a bounded convex polyhedron, the objective function (20) has a unique global minimum. Thus, the equilibrium points of the network can be calculated by assuming the following values of $T^{op}$ and $i^{op}$,

$$i^{op} = -\left[ \frac{\partial f(X)}{\partial x1}, \frac{\partial f(X)}{\partial x2}, \ldots\ldots\ldots\ldots, \frac{\partial f(X)}{\partial xN} \right] \quad \ldots (29)$$

$$T^{op} = 0$$

### 4.1 Estimation Algorithm

The steps followed have been given as under:

**Step 1**: Get the system data, measurements and define the zero injection buses together with boundary limits on the state variables.

**Step 2**: Select an initial erroneous state vector, tolerance limit and set the iteration count.

**Step 3**: Calculate the objective function and say it $f(X)_{old}$.

**Step 4**: Calculate $P_i$ and $Q_i$ corresponding to equality constrained buses.

**Step 5**: Find $\nabla h(X)$ by differentiating zero injection equations w.r.t. State variables using load flow equations.

**Step 6**: Calculate updated state variables by Eqn. (28).

**Step7**: Enforce the boundary limits by passing the state variables through a symmetrical ramp activation function defined by limits $[V_{max}, V_{min}]$ and $[\delta_{max}, \delta_{min}]$ corresponding to each state variable.

**Step 8**: Find $i^{op}$ by differentiating the objective function w.r.t. state variables.

**Step 9**: Find $\Delta X$ by Eqn. (19) and update X computed in step 7.

**Step 10**: Find the mismatch vector between measurements and calculated values and get its weighted squared sum to find out the new objective function value and find the difference between $f(X)_{new}$ and $f(X)_{old}$. If this difference is less than tolerance go next step, else go to step 3 after increasing the iteration count.

**Step11**: Display the results and Stop.

## V. RESULTS

In this chapter 6 bus system and IEEE 14 bus system are used for simulation. The true values were obtained by the result of load flow calculation, and the measurement values were obtained by adding (sigma=0.01) errors to those values. As equality constraints, nodes with zero power injections (nodes

with no load and no generators) are taken.

### 5.1 Six bus system

The measurement set base value for the 6 bus system is shown in Fig. 2 and table (1). Bus no 3 and 4 are characterized as zero injection buses.

| | Hopfield method | | Non linear SE | |
|---|---|---|---|---|
| Bus No. | V | δ | V | δ |
| 1 | 1.0503 | 0 | 1.0482 | 0 |
| 2 | 1.0494 | -4.7065 | 1.0469 | -4.7832 |
| 3 | 0.9892 | -7.6059 | 0.9854 | -7.2324 |
| 4 | 1.0503 | -3.8441 | 1.0513 | -3.7833 |
| 5 | 0.9656 | -6.9388 | 0.9729 | -6.0465 |
| 6 | 0.9683 | -8.8593 | 0.9691 | -8.4704 |

Table 1

| Measurements | Type | Buses | P | Q |
|---|---|---|---|---|
| $z_1$ | Injection | 1 | 0.9740 | -0.0661 |
| $z_2$ | Injection | 2 | 0.5005 | 0.5075 |
| $z_3$ | Injection | 5 | -.7007 | -0.7007 |
| $z_4$ | Injection | 6 | -.7007 | -0.7007 |
| $z_5$ | Line flow | 1-2 | 0.2880 | -0.1550 |
| $z_6$ | Line flow | 1-4 | 0.2830 | -0.0880 |
| $z_7$ | Line flow | 1-5 | 0.4010 | 0.1760 |
| $z_8$ | Line flow | 2-3 | 0.2310 | 0.1940 |
| $z_9$ | Line flow | 2-4 | -0.090 | -0.0700 |
| $z_{10}$ | Line flow | 2-5 | 0.2060 | 0.2110 |
| $z_{11}$ | Line flow | 2-6 | 0.4320 | 0.0440 |
| $z_{12}$ | Line flow | 3-5 | 0.0110 | 0.0520 |
| $z_{13}$ | Line flow | 3-6 | 0.2150 | 0.1810 |
| $z_{14}$ | Line flow | 4-5 | 0.1890 | 0.0900 |
| $z_{15}$ | Line flow | 5-6 | 0.073 | -0.044 |

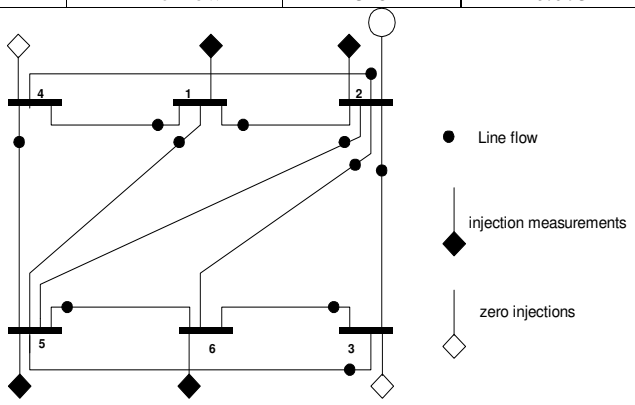


Figure 2: Measurement set for 6 bus system

The estimated state using the method with equality constraints are as shown in table 2

Table 2

| | Hopfield method | | Non linear SE | |
|---|---|---|---|---|
| Bus No. | V | δ | V | δ |
| 1 | 1.0503 | 0 | 1.0482 | 0 |
| 2 | 1.0494 | -4.7065 | 1.0469 | -4.7832 |
| 3 | 0.9892 | -7.6059 | 0.9854 | -7.2324 |
| 4 | 1.0503 | -3.8441 | 1.0513 | -3.7833 |
| 5 | 0.9656 | -6.9388 | 0.9729 | -6.0465 |
| 6 | 0.9683 | -8.8593 | 0.9691 | -8.4704 |

Table 3 shows the errors of the estimate values.

Table 3

| Measurements | ΔP | ΔQ |
|---|---|---|
| $z_1$ | -0.021 | 0.0051 |
| $z_2$ | 0.0068 | 0.0005 |
| $z_3$ | 0.0037 | -0.0003 |
| $z_4$ | 0.0077 | -0.0093 |
| $z_5$ | -0.0083 | 0.0008 |
| $z_6$ | -0.0068 | -0.0013 |
| $z_7$ | -0.006 | -0.0022 |
| $z_8$ | -0.0021 | -0.0014 |
| $z_9$ | 0.0046 | -0.0131 |
| $z_{10}$ | -0.0001 | -0.0016 |
| $z_{11}$ | -0.0033 | -0.0233 |
| $z_{12}$ | 0.0012 | -0.0038 |
| $z_{13}$ | -0.0027 | 0.002 |
| $z_{14}$ | -0.0011 | -0.0036 |
| $z_{15}$ | -0.0019 | -0.0007 |

The energy mismatch delta E was used for the convergence criteria with the tolerance $10^{-02}$. The time step used was $\Delta t=10^{-04}$ in Eq. (19). The convergence characteristics of the energy function with respect to number of iterations is shown in Fig. 3.

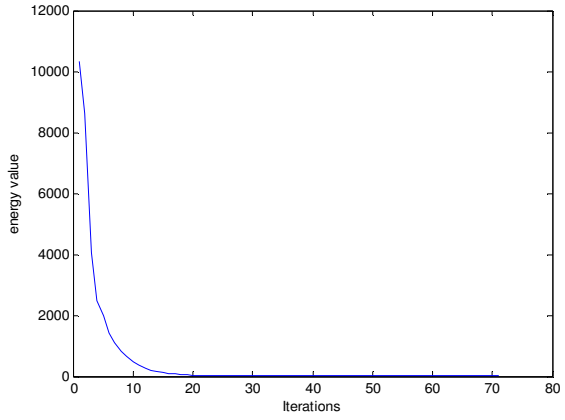


Figure 3: Convergence of energy function

**5.2 IEEE 14 bus system**

The measurement set base value for the IEEE 14 bus system is shown in Fig. 4 and table (4). Bus no 5 and 7 are characterized as zero injection buses. The energy mismatch delta E was

used for the convergence criteria with the tolerance $10^{-05}$.
The time step used was delta t=$10^{-04}$.

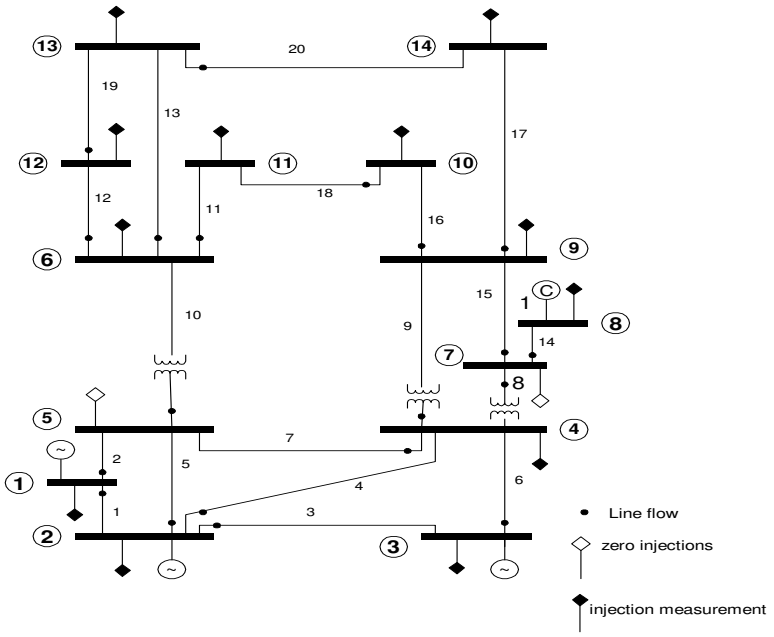


Figure 4: Measurement set for IEEE 14 bus system

Table: 4

| Measurements | Type | Buses | P | Q |
|---|---|---|---|---|
| $z_1$ | Injection | 1 | 2.2462 | -0.1722 |
| $z_2$ | Injection | 2 | 0.1823 | 0.2535 |
| $z_3$ | Injection | 3 | -0.9453 | 0.0426 |
| $z_4$ | Injection | 4 | -0.4783 | 0.0704 |
| $z_5$ | Injection | 6 | -0.1129 | 0.0344 |
| $z_6$ | Injection | 8 | 0.000 | 0.1733 |
| $z_7$ | Injection | 9 | -0.2955 | 0.0234 |
| $z_8$ | Injection | 10 | -0.0922 | -0.0635 |
| $z_9$ | Injection | 11 | -0.0327 | -0.0125 |
| $z_{10}$ | Injection | 12 | -0.061 | -0.016 |
| $z_{11}$ | Injection | 13 | -0.1366 | -0.0605 |
| $z_{12}$ | Injection | 14 | -0.1487 | -0.0489 |
| $z_{13}$ | Line flow | 1-2 | 1.5196 | -0.1628 |
| $z_{14}$ | Line flow | 1-5 | 0.7265 | 0.0479 |
| $z_{15}$ | Line flow | 2-3 | 0.7243 | 0.0603 |
| $z_{16}$ | Line flow | 2-4 | 0.5447 | -0.0123 |
| $z_{17}$ | Line flow | 2-5 | 0.3926 | 0.0099 |
| $z_{18}$ | Line flow | 3-4 | -0.2437 | 0.036 |
| $z_{19}$ | Line flow | 4-5 | -0.6384 | 0.139 |
| $z_{20}$ | Line flow | 4-7 | 0.2806 | -0.1972 |
| $z_{21}$ | Line flow | 4-9 | 0.1607 | -0.0579 |
| $z_{22}$ | Line flow | 5-6 | 0.444 | -0.1794 |
| $z_{23}$ | Line flow | 6-11 | 0.0737 | 0.035 |
| $z_{24}$ | Line flow | 6-12 | 0.0784 | 0.0256 |

| | | | | |
|---|---|---|---|---|
| $z_{25}$ | Line flow | 6-13 | 0.1791 | 0.0745 |
| $z_{26}$ | Line flow | 7-8 | 0.000 | -0.1688 |
| $z_{27}$ | Line flow | 7-9 | 0.2805 | 0.0714 |
| $z_{28}$ | Line flow | 9-10 | 0.0521 | 0.0428 |
| $z_{29}$ | Line flow | 9-14 | 0.0936 | 0.0348 |
| $z_{30}$ | Line flow | 10-11 | -0.0402 | -0.021 |
| $z_{31}$ | Line flow | 12-13 | 0.0166 | 0.008 |
| $z_{32}$ | Line flow | 13-14 | 0.0568 | 0.0177 |

Table 5: The state estimation results

| | **Hopfield method** | | **Non linear SE** | |
|---|---|---|---|---|
| Bus No. | V | δ | V | δ |
| 1 | 1.060 | 0 | 1.060 | 0 |
| 2 | 1.045 | -4.731 | 1.045 | -4.98 |
| 3 | 1.010 | -12.309 | 1.010 | -12.74 |
| 4 | 1.022 | -9.615 | 1.019 | -10.28 |
| 5 | 1.024 | -8.046 | 1.020 | -8.76 |
| 6 | 1.071 | -12.68 | 1.070 | -12.52 |
| 7 | 1.062 | -12.080 | 1.062 | -12.15 |
| 8 | 1.090 | -11.922 | 1.090 | -12.08 |
| 9 | 1.055 | -13.481 | 1.056 | -13.48 |
| 10 | 1.051 | -13.553 | 1.051 | -13.55 |
| 11 | 1.058 | -13.167 | 1.057 | -13.15 |
| 12 | 1.057 | -13.296 | 1.055 | -13.07 |
| 13 | 1.051 | -13.443 | 1.050 | -14.44 |
| 14 | 1.037 | -14.258 | 1.036 | -15.12 |

Table 6 shows the errors of the estimate values for proposed method and Non Linear WLS method.

Table: 6

| | HOPFIELD METHOD | | NR WLS METHOD | |
|---|---|---|---|---|
| Measurements | ΔP | ΔQ | ΔP | ΔQ |
| $z_1$ | 0.0061 | -0.0046 | 0.0037 | -0.0019 |
| $z_2$ | 0.0042 | -0.0066 | -0.0018 | -0.0061 |
| $z_3$ | 0.0018 | -0.0025 | -0.0028 | 0.0028 |
| $z_4$ | 0.0017 | 0.0023 | -0.0014 | 0.0024 |
| $z_5$ | -0.0017 | -0.0051 | -0.0016 | -0.0022 |
| $z_6$ | -0.0018 | 0.0021 | -0.0012 | -0.0081 |
| $z_7$ | -0.0017 | -0.0014 | -0.0082 | 0.0126 |
| $z_8$ | -0.0011 | 0.0012 | -0.0028 | -0.0155 |
| $z_9$ | -0.0016 | 0.0022 | 0.0019 | 0.0657 |
| $z_{10}$ | -0.0021 | 0.0055 | 0.0001 | 0.0509 |
| $z_{11}$ | -0.0017 | 0.0016 | 0.0083 | 0.0852 |
| $z_{12}$ | -0.0023 | 0.0066 | -0.0405 | -0.0067 |
| $z_{13}$ | 0.0275 | -0.0025 | 0.0329 | -0.0087 |
| $z_{14}$ | 0.0329 | -0.0021 | 0.0161 | -0.0433 |
| $z_{15}$ | 0.0063 | -0.0016 | 0.0173 | -0.0147 |
| $z_{16}$ | 0.0316 | -0.0037 | 0.0128 | -0.0046 |
| $z_{17}$ | 0.0305 | -0.0082 | 0.0085 | -0.0054 |
| $z_{18}$ | 0.0237 | -0.0057 | -0.0058 | 0.0013 |
| $z_{19}$ | -0.0063 | -0.0138 | -0.0018 | 0.0129 |

| | | | | |
|---|---|---|---|---|
| $z_{20}$ | 0.0522 | 0.0021 | 0.0096 | -0.0276 |
| $z_{21}$ | 0.0256 | 0.0015 | 0.0525 | -0.0058 |
| $z_{22}$ | 0.0666 | 0.0095 | 0.0148 | 0.0499 |
| $z_{23}$ | 0.0086 | -0.0012 | -0.0012 | -0.0057 |
| $z_{24}$ | 0.0173 | -0.0027 | 0.0003 | -0.0046 |
| $z_{25}$ | 0.0239 | -0.0045 | -0.0001 | -0.0086 |
| $z_{26}$ | 0.0181 | -0.0061 | 0.0126 | 0.0074 |
| $z_{27}$ | 0.0308 | -0.0008 | 0.0083 | 0.0016 |
| $z_{28}$ | 0.0194 | -0.0019 | 0.0243 | 0.0081 |
| $z_{29}$ | 0.0204 | -0.0043 | 0.0298 | 0.0043 |
| $z_{30}$ | 0.0079 | -0.0011 | 0.0047 | -0.0075 |
| $z_{31}$ | -0.0034 | 0.0023 | 0.0022 | 0.0032 |
| $z_{32}$ | 0.0029 | -0.0014 | 0.0011 | 0.0041 |

The convergence characteristics of the energy function with respect to number of iterations is shown in Fig.5

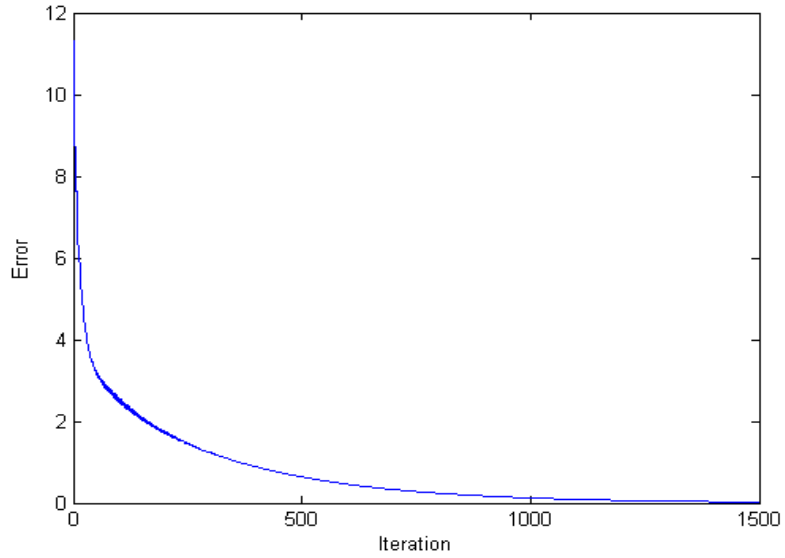


Figure 5: Convergence of energy function

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# DEPLOYMENT ISSUES OF SBGP, SOBGP AND PSBGP: A COMPARATIVE ANALYSIS

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## *ABSTRACT*

*Border Gateway Protocol (BGP) is the protocol backing the core routing decisions on the Internet. It maintains a table of IP networks or 'prefixes' which designate network reachability among autonomous systems (AS). Point of concern in BGP is its lack of effective security measures which makes Internet vulnerable to different forms of attacks. Many solutions have been proposed till date to combat BGP security issues but not a single one is deployable in practical scenario. Any security proposal with optimal solution should offer adequate security functions, performance overhead and deployment cost. This paper critically analyzes the deployment issues of best three proposals considering trade-off between security functions and performance overhead.*

***KEYWORDS:*** *BGP, secure BGP, secure origin BGP, pretty secure BGP, inter domain routing, ASes.*

## I. INTRODUCTION

The Border Gateway Protocol (BGP) [1], has provided interdomain routing services for the Internet's disparate component networks since the late 1980's [2]. Given the central role of routing in the operation of the Internet, BGP is one of the critical protocols that provide security and stability to the Internet [3].

BGP's underlying distributed distance vector computations rely heavily on informal trust models associated with information propagation to produce reliable and correct results. It can be likened to a hearsay network information is flooded across a network as a series of point-to-point exchanges, with the information being incrementally modified each time it is exchanged between BGP speakers. The design of BGP was undertaken in the relatively homogeneous and mutually trusting environment of the early Internet.

Today's inter-domain routing environment remains a major area of vulnerability [3]. BGP's mutual trust model involves no explicit presentation of credentials, no propagation of instruments of authority, nor any reliable means of verifying the authenticity of the information being propagated through the routing system. Hostile actors can attack the network by exploiting this trust model in inter-domain routing to their own ends. Current research on BGP is predominately focused on two major themes; scaling, and resistance to subversion of integrity [4].

A key question is whether further information can be added into the inter-domain routing environment such that attempts to pervert remove or withhold routing information may be readily and reliably detected. Any proposed scheme(s) must also be evaluated for their impact on the scaling properties of BGP [5]. In second section of the paper BGP Architecture is discussed in detail with its vulnerability against associated attack vectors and resulting consequences of such attacks. In third section three best proposals are discussed including their architecture, functionality and mechanism. In forth section a rigorous comparative analysis has been done with deployment issues of each solution. In fifth section conclusion has been obtained with some open questions for further research.

## II. THE BGP ARCHITECTURE

The Internet's routing system is a structured two-level hierarchy [6]. At the bottom level we have routing elements grouped into Autonomous Systems (ASes) [7]. Each AS represents a collection of

routing elements sharing a common administrative context. Where a BGP speaker is presented with multiple paths to the same address prefix from a number of peers, the BGP speaker selects the "best" path to use by minimizing a distance metric across all the possible paths as shown in figure 1. The distance metric used by BGP speakers is the AS Path length. This BGP-selected route object is used to populate the local forwarding table. The BGP speaker then assembles a new route object by taking the locally selected route object, attaching locally significant attributes and adding its own AS value to the route objects AS path vector. This route object is then announced to all BGP peers.

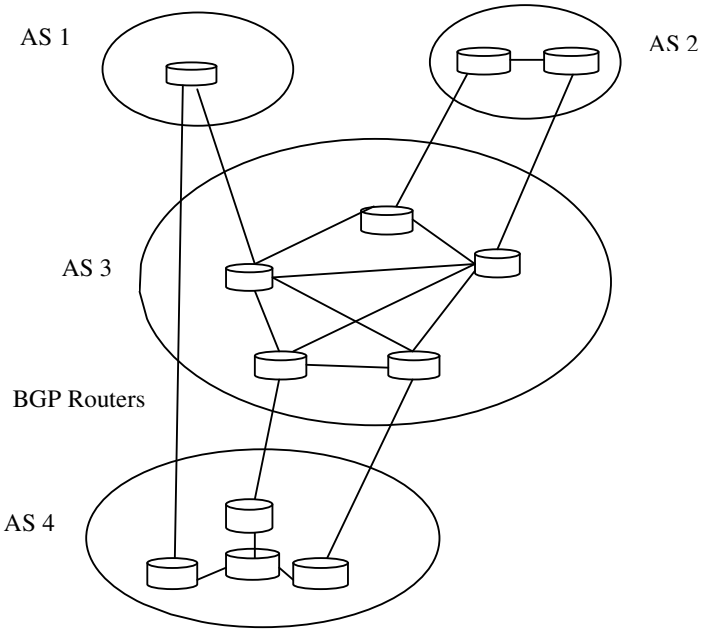


Figure1 BGP Architecture

One approach is to provide taxonomy for threats in routing in general, and BGP in particular, is to view a BGP peer session as a conversation between two BGP speakers and pose a number of questions relating to this conversation which includes the manner in which the BGP session between the BGP speakers is secured, verifying the identity of the other party, verifying the authenticity of the routing information, verifying that the routing information actually represents the state of the forwarding system i.e. Is the information still valid?

### 2.1 Attack Vectors and Securing BGP session

A BGP session between two routers is assumed to have some level of integrity at the session transport level. BGP assumes that the messages sent by one party are precisely the same messages as received by the other party, and assumes that the messages have not been altered, reordered, have spurious messaged added into the stream or have messages removed from the conversation stream in any way. As with any long-held TCP session, the BGP peer session is vulnerable to eavesdropping, session reset, session capture, message alternation and denial of service attacks via conventional TCP attack vectors.

Attack Vectors are eavesdropping, session hijacking, MITM, modification and DOS at TCP/IP level. Validation of members and IP spoofing are common attacks at identification level. Path Validation, prefix hijacking & impersonation etc are vulnerable at information level. Masquerading is a common attack at route validation level.

Route Flap Damping (RFD) [9], [10] is a widespread defensive BGP configuration that monitors the frequency of BGP updates for a given prefix from each peer, and if the update rate exceeds a locally set threshold the peer's advertisement of this prefix will be locally suppressed for a damping interval. The replay of updates could be used to trigger an RFD response in the remote BGP speaker [11]. If a route is fully dampened through RFD, updates for this prefix will not be advertised by the BGP speaker for a damping interval, possibly causing a route to be disrupted within that time frame.

Another form of threat is by withholding traffic. BGP uses KEEPALIVE timers to determine remote end "LIVENESS". By intercepting and withholding all messages for the hold down timer interval, a third party can force the BGP session to be terminated and reset. This causes the entire route set to be re-advertised upon session resumption so that repeated attacks of this form can be an effective form of denial of service for BGP. It is also possible to undertake a saturation attack on a BGP speaker by sending it a rapid stream of invalid TCP packets. In this case the processing capability of the BGP speaker is put under pressure, and the objective of the attack is to overwhelm the BGP speaker and cause the BGP session to fail and be reset.

### 2.2 The Consequences of Attacks

The ability to alter the routing system provides a broad array of potential consequences [6]. The consequences fall into a number of broad categories which comprises of the ability to eavesdrop, Denial of service, the potential to masquerade, the ability to steal addresses and obscure identity [12], MITM, session hijacking, IP spoofing and prefix hijacking.

## III. BGP SECURITY PROPOSALS

The vulnerabilities of BGP arise from four fundamental weaknesses in the BGP and the inter-domain routing environment [6]. These are inability to protect integrity, lack of authenticity verification for an address prefix, inability to verify the authenticity of BGP UPDATE message and no mechanism to verify that the local cache RIB information. The major contribution to this area of study is the secure BGP (sBGP) proposal [13], which is the most complete contribution to date. However, the assumptions relating to the environment in which sBGP must operate, particularly in terms the performance capability of routing systems appear to be beyond the capabilities of routers used in today's Internet [14]. A refinement of this approach, soBGP [15], is an attempt to strike a pragmatic balance between the security processing overhead and the capabilities of deployed routing systems and security infrastructure, where the requirements for AS Path verification are relaxed and the nature of the related Public Key Infrastructure (PKI) is altered to remove the requirement for a strict hierarchical address PKI that precisely mirrors the address distribution framework. Another refinement of the sBGP model, psBGP [16], represents a similar effort at crafting a compromise between security and deployed capability through the crafting of a trust rating for assertions based on assessment of confidence in corroborating material.

### 3.1 Secure BGP

Secure BGP (sBGP) [13], represents one of the major contributions to the study of inter-domain routing security, and offers a relatively complete approach to securing the BGP protocol by placing digital signatures over the address and AS Path information contained in routing advertisements and defining an associated PKI for validation of these signatures. sBGP defines the "correct" operation of a BGP speaker in terms of a set of constraints placed on individual protocol messages, including ensuring that all protocol UPDATE messages have not been altered in transit between the BGP peers, that the UPDATE messages were sent by the indicated peer, the UPDATE messages contain more recent information than has been previously sent to this BGP speaker from the peer, the UPDATE was intended to be received by this BGP speaker, and that the peer is authorized to advertise information on behalf of the peer Autonomous System. In addition, for every prefix and its originating AS, the prefix must be a validly allocated prefix, and the prefix's "right-of-use" holder must have authorized the advertisement of the prefix and must have authorized the originating AS to advertise the prefix. The basic security framework proposed in sBGP is that of digital signatures, X.509 certificates and PKIs to enable BGP speakers to verify the identities and authorization of other BGP speakers, AS administrators and address prefix owners. The verification framework for sBGP requires a PKI for address allocation, where every address assignment is reflected in an issued certificate [17]. This PKI provides a means of verification of a "right-of-use" of an address. A second PKI maps the assignment of ASes, where an AS number assignment is reflected in an issued certificate, and the association between an AS number and a BGP speaking router is reflected in a subordinate certificate. In addition, sBGP proposes the use of IPSEC to secure the inter-router communication paths. sBGP also proposes the use of attestations. The address and attestations, allow a BGP speaker to verify the

origination of a route advertisement and verify that the AS path as specified in the BGP UPDATE is the path taken by the routing UPDATE message via the sequence of nested route attestations. Inter-operation and information exchange between sBGP elements is shown in Figure 2. sBGP proposes to distribute the address attestations and the set of certificates that compose the two PKIs via conventional distribution mechanisms outside of BGP messages. For Route Attestations it is necessary to pass these attestations via path attributes of the BGP UPDATE message, as an additional attribute of the UPDATE message. There is a number of significant issues that have been identified with sBGP including the computation burden for signature generation and validation, the increased load in BGP session restart, the issue of piecemeal deployment and the completeness of route attestations, and the requirement that the BGP UPDATE message has to traverse the same AS sequence as that contained in the UPDATE message [14], [18], [19].

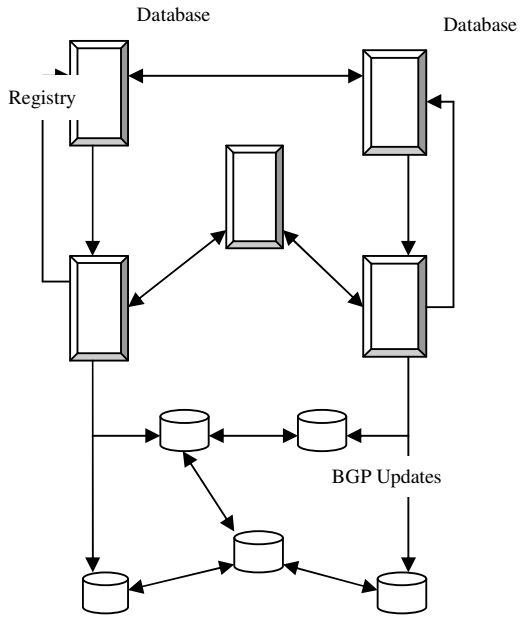


Figure 2 sBGP Mechanism

### 3.2 Secure Origin BGP

Secure Origin BGP (soBGP) [15] is a response to some of the significant issues that have been raised with the sBGP approach, particularly relating to the update processing load when validating the chain of router attestations and the potential overhead of signing every advertised UPDATE with a locally generated router attestation [20]. The validation questions posed by soBGP also includes the notion of an explicit authorization from the address holder to the originating AS to advertise the prefix into the routing system. The AS path validation is quite different from sBGP however, in that soBGP attempts to validate that the AS path, as presented in the UPDATE message, represents a feasible inter-AS path from the BGP speaker to the destination AS. This feasibility test is a weaker validation condition than validating that the UPDATE message actually traversed the AS path described in the message.

soBGP targets the need to verify the validity of an advertised prefix. It verifies a peer which is advertising a prefix that has at least one valid path to the destination. The best feature of soBGP is that it is incrementally deployable and allows deployment flexibility (on-box or off-box encryption), in its working, BGP verifies the route of originator and its authorization. New BGP message is used to carry security information and it has fixed additional scalability requirements. It uses web of trust model to validate certificate.

soBGP uses the concept of an ASPolicyCert as the foundation for constructing the data for testing the feasibility of a given AS Path. An ASPolicyCert contains a list of the AS's local peer ASes, signed by the AS's private key. AS peer is considered valid if both ASes list each other in their respective ASPolicyCerts. The overall approach proposed in soBGP represents a different set of design trade-offs to sBGP, where the amount of validated material in a BGP UPDATE message is reduced. This

can reduce the processing overhead for validation of UPDATE messages. Also it optimizes memory and encourages distributed processing.
The avoidance of a hierarchical PKI for the validation of AuthCerts and EntityCerts could be considered a weakness in this approach, as the derivation of authority to speak on addresses is very unclear in this model.

### 3.3 Pretty Secure BGP

Pretty Secure BGP (psBGP) [16] puts forward the proposition that the proposals relating to the authentication of the use of an address in a routing context must either rely on the use of signed attestations that need to be validated in the context of a PKI, or rely on the authenticity of information contained in Internet Routing Registries. The weakness of routing registries is that the commonly used access controls to the registry are insufficient to validate the accuracy or the current authenticity of the information that is represented as being contained in a route registry object. The information may have been accurate at the time the information was entered into the registry, but this may no longer be the case at the time the information is accessed by a relying party. The psBGP approach is also motivated by the proponent's opinion that a PKI could not be constructed in a deterministic manner because of the indeterminate nature of some forms of address allocations. This leads to the assertion that any approach that relies on trusted sources of comprehensive information about prefix assignments and the identity of current right-of-use holders of address space is not a feasible proposition. Accordingly, psBGP rejects the notion of a hierarchical PKI that can be used to validate assertions about addresses and their use. Interestingly, although psBGP rejects the notion of a hierarchical address PKI, psBGP assumes the existence of a centralized trust model for AS numbers and the existence of a hierarchical PKI that allows public keys to be associated with AS numbers in a manner that can be validated in the context of this PKI. This exposes a basic inconsistency in the assumptions that lie behind psBGP, namely that a hierarchical PKI for ASes aligned to the AS distribution framework is assumed to be feasible, but a comparable PKI for addresses is not. Given that the same distribution framework has been used for both resources in the context of the Internet, it is unclear why this distinction between ASes and addresses is necessary or even appropriate. psBGP uses a rating mechanism similar to that used by PGP [21], but in this case the rating is used for prefix origination. An AS asserts the prefix it originates and also may list the prefixes originated by it's AS peers in signed attestation. The ability of an AS to sign an attestation about prefixes originated by a neighbor AS allows a psBGP speaker to infer AS neighbor relationship from such assertions, allowing the local BGP speaker to construct a local model of inter-AS topology in a fashion analogous to soBGP. One of the critical differences between psBGP and soBGP is the explicit inclusion of the "strict" AS Path validation test, namely that it is a goal of psBGP to allow a BGP speaker to verify that the BGP UPDATE message traversed the same sequence of ASes as is asserted in the AS Path of the UPDATE message. The AS path validation function relies on a sequence of nested digital signatures of each of the ASes in the AS Path for trusted validation, using a similar approach to sBGP. psBGP allows for partial path signatures to exist, mapping the validation outcome to a confidence level rather than a more basic sBGP model of accepting an AS path only if the AS Path in the BGP UPDATE message is completely verifiable. The essential approach of psBGP is the use of a reputation scheme in place of a hierarchical address PKI, but the value of this contribution is based on accepting the underlying premise that a hierarchical PKI for addresses is infeasible. It is also noted that the basis of accepting inter-AS ratings in order to construct a local trust value is based on accepting the validity of an AS trust rating, which, in turn, is predicated upon the integrity of the AS hierarchical PKI. psBGP appears to be needlessly complex and bears much of the characteristics of making a particular solution fit the problem, rather than attempting to craft a solution within the bounds of the problem space. The use of inter-AS cross certification with prefix assertion lists introduces considerable complexity in both the treatment of confidence in the assertions and in the resulting assessment of the reliability of the verification of the outcome. psBGP does not consider the alternate case where the trust model relating to addresses is based on a hierarchical PKI that mirrors the address distribution framework. In such a case the calculation of confidence levels would be largely unnecessary.

The major contribution of psBGP relates to the case of partial deployment of a security solution in relation to AS Path validation, where the calculation of a confidence rating in the face of partial security information may be of some utility.

## IV. RESULTS AND DISCUSSION

The proposal having the most support from the community is the S-BGP architecture, which employs three security mechanisms, Public Key Infrastructure (PKI) to support the authentication of ownership (secure origin), Digital signatures covering the routing information (AS path validation), IPsec to provide data and partial sequence integrity. In sBGP & soBGP a public key certificate is issued to each BGP speaker whereas psBGP employs common public key certificate for all speakers within one AS resulting requirement of fewer BGP speaker certificates [16].

### 4.1 Comparative Analysis

Comparative analysis has been done in table 1 based on trust model, topological authentication, path authentication, and origin authentication. It has been observed that origin authentication is strong in sBGP & soBGP whereas path authentication is strong in sBGP and psBGP, although psBGP uses centralized trust model but it is weaker solution than sBGP.

Table 1: Comparative Analysis

| Proposal | Trust Model | Topo. Auth | Path. Auth | Origin Auth |
|---|---|---|---|---|
| sBGP | Centralized | Strong | Strong | Strong |
| soBGP | Web-of-Trust | Strong | None | Strong |
| psBGP | Centralized | Weak | Strong | Weak |

### 4.2 Deployment Issues

Deploying S-BGP raises a number of other issues like Adoption of S-BGP by several groups, S-BGP's interaction with other exterior and interior routing, BGP-4 to S-BGP transition. The route attestation path attribute is optional for both external and internal BGP exchanges. This allows extensive regression testing before deploying S-BGP on production equipment. Security Mechanism employed by S-BGP is Public Key Infrastructure (PKI) to support the authentication of ownership (secure origin) Digital signatures covering the routing information (AS path validation) and IPsec to provide data and partial sequence integrity. Deployment of soBGP is done by exchanging certificates at all BGP peering points or AS edges, it processes the certification and build the required soBGP tables at each BGP speaker.

Table 2: Deployment Issues

| Proposal | Type | Reference Implementation | Deployed |
|---|---|---|---|
| sBGP | Crypto | Yes | No |
| soBGP | Anomaly | No | No |
| psBGP | Crypto | No | No |

## V. CONCLUSION

BGP does not use traditional Interior Gateway Protocol (IGP) metrics, but makes routing decisions based on path, network policies and/or rule sets. For this reason, it is more appropriately termed a reachability protocol rather than routing protocol. Though all of the above solution have their own impact to combat BGP attacks but still some questions are unanswered like, how many AS must implement secure routing, what kind of policies are most suitable for AS to secure BGP architecture globally looking to its tremendous expansion and what should be priorities in securing AS in order to establish highest number of secure routes. sBGP is the best solution among all of them but problems associated with its deployment are unsolved. The most obvious negligence in today's scenario is PKI for addresses and ASes that would allow anyone to verify a digital attestation.

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# A SOFTWARE REVERSE ENGINEERING METHODOLOGY FOR LEGACY MODERNIZATION

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## *ABSTRACT*

*This paper identified that Legacy Systems have embedded within them, a large investment which ranges from low level code items or objects through to higher level business objects; made by the systems developers and/or owners. Most organizations would at one time or the other be confronted with the problem of migrating their legacy applications to new platforms in order to preserve previous investments and the software engineering community had been confronted with the problem of understanding legacy systems. A reverse engineering methodology for modernization of legacy systems based on a transformation paradigm aimed at preserving capital investments and saving production and maintenance costs were described in this paper. The transformation approach involved retaining and extending the value of the investments on the legacy system through migration and modernization of the subject system.*

***KEYWORDS:*** *Legacy application, system modernization, reverse engineering, artifacts, software capital investments*

## I. INTRODUCTION

Most organizations would at one time or the other be confronted with the problem of converting their legacy applications and the software engineering community had been confronted with the problem of understanding legacy systems. Originally, legacy code was used to refer to programs written in old compilers; however, today's software developers predominantly use Object Oriented languages and this implied that tomorrow's legacy code is being written today, since object oriented programs are even more complex and difficult to comprehend, even when rigorously documented; most organizations end up with software that is even more obscure accompanied by insufficient design documentation [1].

Reverse engineering focuses on obtaining high-level representations of programs (probably written by another programmer). It typically starts with a low level representation of a system (such as binaries, plain source code, or execution traces), and try to distil more abstract representations from these such as, source code, architectural views, or use cases, respectively. The methods and technologies play an important role in many software engineering tasks, such as program comprehension, system migrations, and software evolution [2]. As observed by [3]; upward migration from procedural and structured programs to object-based technologies is very difficult and it is often impossible, to predict how the system is going to evolve during the process of development. Also Software systems; as artifacts will continually change over time, or become increasingly less useful, and the structure of evolving software will degrade unless remedial action is taken.

This paper described a methodology for modernization of legacy systems based on a transformation paradigm and an application to real-life software system. The transformation approach involves retaining and extending the value of the investments on the legacy system through migration and modernization of the subject system and extending it beyond the architectural barriers.

## II. REVIEW OF RELATED WORK

A migration approach that involved the identification of software artifacts in the subject system and the aggregation of these artifacts to form more abstract system representations was presented in [4]. This approach led to the emergence of the RIGI tool. Early industrial experience showed that the

software engineers using Rigi can quickly build mental models from the discovered abstractions that are compatible with the mental models formed by the maintainers of the underlying software.

A program analysis approach using Synchronized Refinement as a systematic approach to detecting design decisions in source code and relating the detected decisions to the functionality of the system was described by [5] in 1994. The methodology; in addition to this approach, used approaches and representations typically found in the forward software development process, including a high-level, textual overview and graphical representations of data flows and file structures.

A case for legacy transformation, as opposed to complete discard of the legacy system based on the fact that existing application are a result of past capital investments for the organization was made by [6]. The work took the view that *J2EE* or *.NET* were suitable target platforms for transformation. The arguments in favour were based on technical and cost factors, on the fact that most automatic translation products target these platforms, on a growing skill-base in J2EE and .NET, making it easier to recruit staff, and on the availability of standard XML-based protocols for use by other applications, which facilitate the publication of application function to a network (usually referred to as 'Web Services').

A process to extract original architecture from a legacy system was developed in [3]. The methodology was a cognitive design recovery process and utilized several sources of domain knowledge to obtain relevant information about the application and get into the minds of the earlier developers with the aim of reconstructing the architecture. The re-constructed architecture is further compared with the original architecture to obtain the level of conformance.

A model for industrial large-scale software modification projects was described by [7]. The paper comprised a discussion on the process for problem analysis, pricing and contracting for such projects, design and implementation of tools for code exploration and code modification, as well as details of service delivery. These concerns were illustrated by way of a real-world example where a deployed management information system required an invasive modification to make the system fit for future use.

A report submitted by [8] described an enterprise framework that characterized the global environment in which system evolution takes place and provided insight into the activities, processes, and work products that shape the disciplined evolution of legacy systems. The work included exemplary checklists that identified critical enterprise issues corresponding to each of the framework's elements. Preliminary results indicated that the enterprise model was a useful tool for probing and evaluating planned and ongoing system evolution initiatives and the model served to draw out important global issues early in the planning cycle and provided insight for developing a synergistic set of management and technical practices to achieve a disciplined approach to system evolution. [9]; outlined a comprehensive system evolution approach that incorporated an enterprise framework for the application of the promising technologies in the context of legacy systems. The report revealed that the approach that one chooses to evolve software-intensive systems depends on the organization, the system, and the technology and concluded that there must be a framework in which to motivate the organization to understand its business opportunities, its application systems, and its road to an improved target system.

A white paper by [10] pointed out that Legacy systems contain useful business knowledge, but extracting that value is becoming increasingly difficult. The paper described the Cognizant approaches, methodologies, and its proven processes in restoring the legacy applications that are developed using various technologies that require specific answers.

## III. METHODOLOGY

The model is an Architecture reconstruction process where the "as-built" architecture is obtained from an existing legacy system based on a modernization process sub-divided into many process steps which cut across understanding the goals of the evolutional changes that will have to be made to the legacy system and the actual modernization exercise (Figure 1). Modernization generally transforms a legacy system in in three phases: Initialization, Extraction and Modernization (Figure 2).

The first process required that the reverse engineering effort have a goal and a set of objectives or questions in mind before undertaking an architecture reconstruction project. An important goal might be for example, reusing part of the system in a new application and without these goals and

objectives, a lot of efforts could be spent on extracting information and generating architectural views that may not be helpful or serve any purpose.

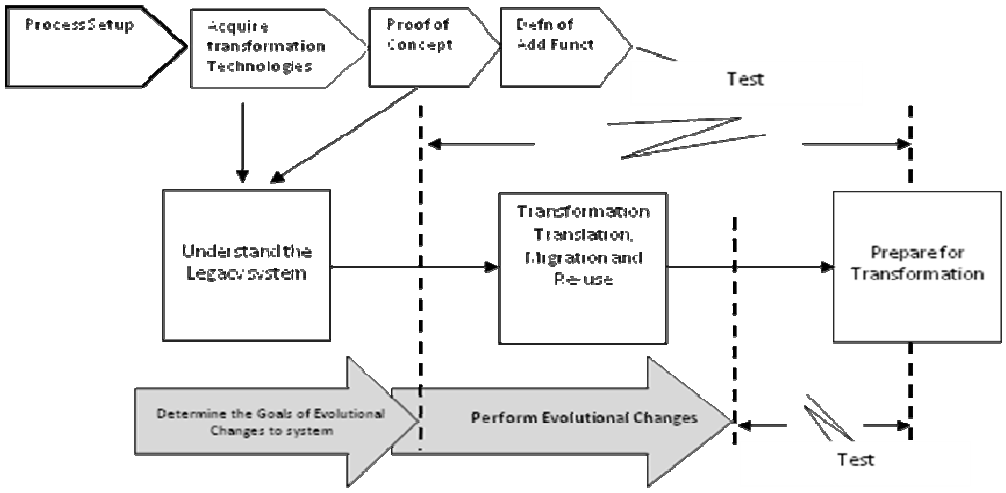


Figure 1: Evolution of a Modernized Legacy System

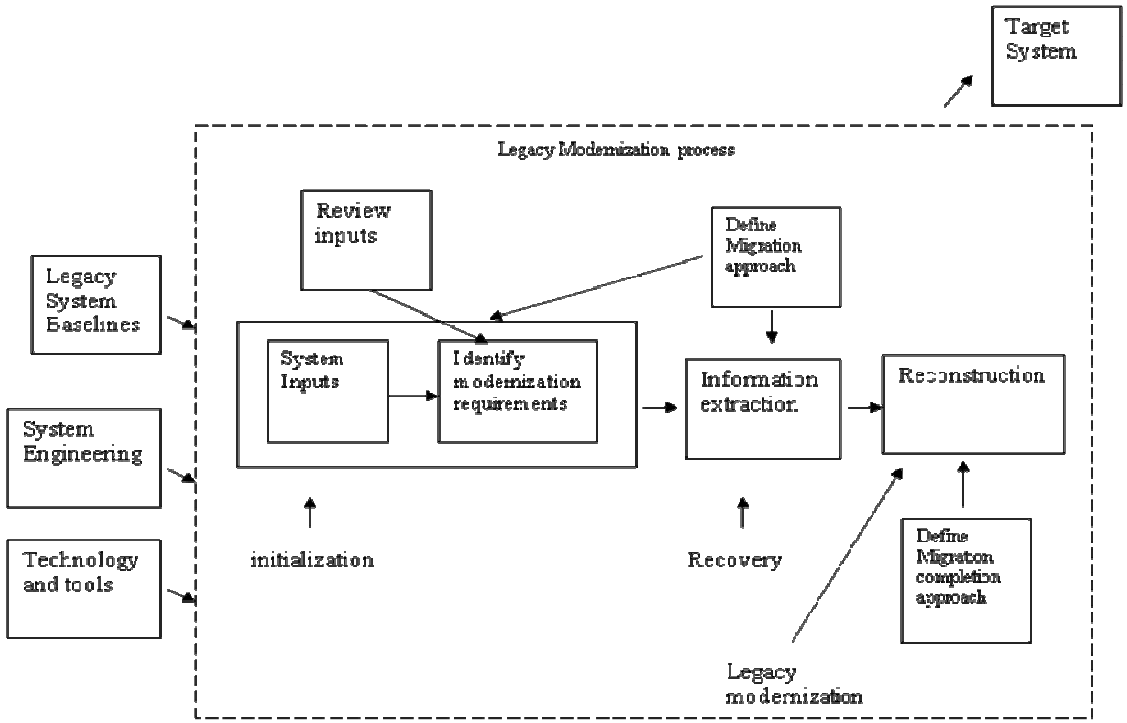


Figure 2. Modernization Model

Architectural extraction involved obtaining a high-level view of the legacy system after extracting helpful information and using the extracted information to generate a different view of the system in a higher level of abstraction. Other factors considered include the operating environments for the legacy system and the modernized version and the required support environments. The methodology also involved an evaluation of how the on-going enhancements to the legacy systems will be managed while the target system is phased in and the mechanisms to ensure that users will be able to fully convert to the new system at specific points.

The input to the system is the legacy system and the output is the modernized version with enhanced legacy assets. Other inputs required to bring about the modernization process include relevant technologies and tools and system engineering processes.

## IV. RESULTS AND DISCUSSIONS

The authors in this work presented a multi-level legacy modernization roadmap that involved; information extraction; which in turn involves artifacts gathering from many sources, knowledge organization, analysis, and information abstraction involving aggregating components, relationships, synthesizing abstractions, building hierarchical mental models and ensuring that the subject system is not altered; but additional knowledge about the system is produced (Figure 2).

Within this multi-level view of transformations, the methodology was intended to depict architecture-level transformations as the context in which lower-level transformations subsist; and the various levels of abstractions identified were application, structure, function and implementation. The methodology defined application architecture and legacy modernization roadmap after evaluating various modernization options with ETCR (Effort, Time, Cost and Risk) technique to build multiple hierarchical mental models and subsystems based on software engineering principles (classes, modules, directories, cohesion, data & control flows, slices), design and change patterns, business and technology models, function, system, and application architectures, common services and infrastructure. The methodology also supported building on the foundations of a legacy asset, procuring enabling technologies for translation, data migration, and re-use, or a suitable partner identified to provide the technologies thereby leading to a smooth transition. The concept here is that the modernization project plan needs to gradually build up the knowledge about the existing and target applications, and create the knowledge for its extended support.

## V. CONCLUSION

There will always be old software that needs to be understood. It is critical for the software industry to deal with the problems of software evolution and the understanding of legacy software systems. Bearing in mind that legacy systems are products of capital investments of a firm and since the primary focus of the industry is changing from completely new software construction to software maintenance and evolution, software engineering research and education must make some major adjustments. In particular, more resources should be devoted to software analysis in balance with software construction.

The authors in this paper had proffered a transformation of legacy software using modernization process. Legacy transformation project exhibits many of the characteristics of traditional development projects such as objectives setting, user involvement, testing, scheduling, monitoring, and so on. There are however some factors that differentiate it from the traditional software development and these includes:

- The solution is built on the foundations of a legacy asset, rather than starting with a discovery of business requirements. Of course there may be additional functional requirements to be added, but the usual procedure is to add this functionality after the transformation is complete.
- Enabling technologies need to be procured for translation, data migration, and re-use, or a suitable partner identified to provide the technologies.
- Because the legacy application is already part of today's business operations, a smooth transition is vital.
- Know-how needs to be built up over the course of the project so that support capabilities are in place on completion.
- Adjustments will be needed to existing development methodologies to ensure that the work is structured to fit the needs of a transformation project and delivers to business and technical objectives, schedule, and budget.

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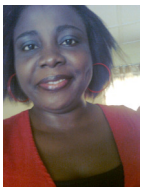
**Authors' Biography**



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# OPTIMUM POWER LOSS IN EIGHT POLE RADIAL MAGNETIC BEARING USING GA

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## *ABSTRACT*

*This paper includes principle of working and design of eight pole active magnetic journal bearing (AMJB). A study of eight pole magnetic bearing design is done for peak load carrying capacity and with this condition stator dimensions, coil dimensions are obtained for finding different stator and rotor losses like copper loss, eddy current loss hysteresis loss, wind age loss . Also it includes study of these various stator and rotor losses with equations, loss dominating parameters. The objective function for optimum total energy loss is considered for four variables such as air gap length, magnetic flux density, rotor speed, lamination thickness. Suitable constraints and bounds are chosen for each loss and optimal loss is calculated using single objective genetic algorithm.*

***KEYWORDS:*** *Radial magnetic bearing, eight poles, optimum loss, genetic algorithm.*

## I. INTRODUCTION

Active magnetic bearings (AMB) are experiencing an increased use in many rotating machines like compressors, milling spindles, flywheels, as an alternative to conventional mechanical bearings such as fluid film and rolling element bearings. An AMB provides a non-contact means of supporting a rotating shaft through an attractive magnetic levitation force and hence they offer many advantages over conventional bearings. Active magnetic bearings are a typical mechatronic product. They are composed of mechanical components combined with electronic elements such as sensors, power amplifiers and controllers which may be in the form of a microprocessor.

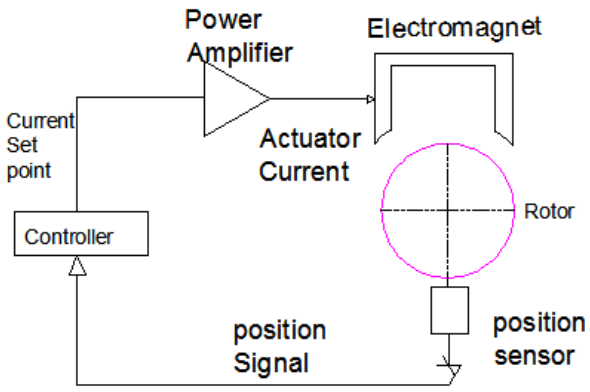


Figure 1. Block diagram of AMB system

Whenever a current carrying conductor is wound around a closed path magnetic field is created following right hand thumb rule. This magnetic field has strength to attract the rotor. Bearings provide support to rotating machinery by allowing relative movement in a plane of rotation. A body is said to

be levitated if it is in a state of stable or of independent equilibrium relative to the earth, in which material contact between the body and its environment is not essential (Maslen, 2000). Magnetic bearing systems incorporate this feature, which makes its application possible in huge, weighted rotational systems having high rotational speeds.

The typical AMB system block diagram is illustrated in Fig.1. Besides the controller, the general control system also includes the sensor, A/D and D/A conversion and power amplifier.

The rotor' displacement along one of the axes is detected by these position sensors and converted into signals of standard voltage. Then compared with the setting value, the error signal enters the controller. After A/D conversion, the controller processes this digital signal according to a given regulating rule (control arithmetic) and generates a signal of current setting. After D/A conversion, this current signal enters the power amplifier, whose function is to maintain the current value in the electric magnet winding at the current level set by the controller. Therefore, if the rotor leaves its center position, the control system will change the electromagnet current in order to change its attraction force and, respectively, draws the rotor back to its balance position.[6]

In the present paper, a theoretical design of eight pole radial magnetic bearing and single objective total loss optimization procedure have been presented and illustrated. Objective functions have been considered, namely minimization total power loss considering four variables like air gap length, rotor speed, magnetic flux density and lamination thickness of rotor. The optimization model, the implementation algorithm, discussion of results and conclusions has been detailed in the following sections.

### a. Eight pole active magnetic bearing

The active magnetic journal bearings are located in the AMB system shown in Fig. 2.The AMB system consists of two bearings with a rotor of length 1m and diameter 0.06 m, and weight of the rotor is 653.3 N. Total weight including auxiliary bearing is taken as 700 N. The radial bearing nominal air gap is 0.5 mm. Initially the rotor is kept on an auxiliary bearing at rest position with a gap of 0.25 mm.

The main parameters of the magnetic bearings are mentioned below.

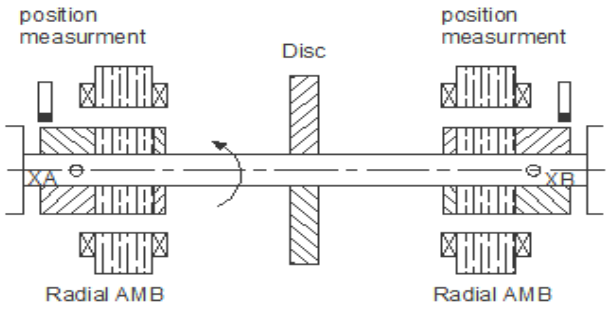


Figure 2. Radial Magnetic Bearing with rotor arrangement

## II. Design Of Radial Magnetic Bearing

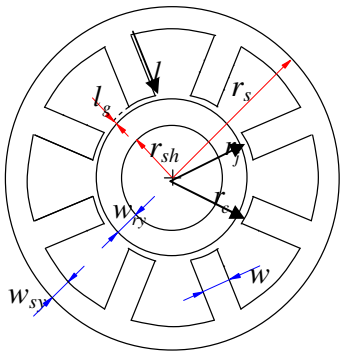


Figure 3. Stator geometry showing eight poles.

## 2.1. Design Steps for Eight Pole Bearing

Following are design steps for eight pole magnetic bearing [6],

**2.1.1 Calculation of gap area,** $(A_g)$ :

We know that maximum force, $F_{\max}$ carried by AMB

$$F_{\max} = \frac{\sigma' B_{sat}^2 n_p A_g}{2\mu_0} \tag{1}$$

Where,

$A_g = w_p.l_p$ , ( $w_p$ -width of pole, $l_p$ -length of pole) , $\mu_0$ -Permeability of Vacuum ($4\pi\times10^{-7}$ H/m), stress, $n_p$ -Number of poles, $const.\sigma'$ -0.24 (for 8 number of legs of actuator),

$A_g = 0.003398m^2$

**2.1.2 Journal dimensions**: Journal radial dimension at least 0.5 or 1.0 times width to avoid saturation.

$$r_j > r_r + f_s.w_p \tag{2}$$

Where, $f_s$ –split flux(0.5)

$r_j$ -Radius of journal, $r_r$ –radius of rotor

$$A_g = 2\gamma w_p (r_r + f_s w_p) \tag{3}$$

Solving equation (3) , the width and length of pole are 0.81cm and 11.6 cm .

Diameter of journal, $d_j = 2(r_r + f_s w_p)$

$d_j = 11.62cm$

So, radius of journal, $r_j = 5.81cm$

**2.1.3 Bias point selection**: $\frac{F_{dy}}{F_{\max}} = \frac{\beta^2}{\sigma'}$

Where, Dynamic load capacity , $F_{dy}$ = 300 Nm

we get, $\beta$ =0.46

**2.1.4 Coil design**: For available coil space thickness of coil is calculated as,

$$t_c = r_p \tan\left(\frac{\pi}{n_p}\right) + \left(\frac{w_p}{2}\right) \tag{4}$$

Where,

$t_c$ –Thickness of coil, $r_p$ – pole tip radius,

$r_p = r_j + l_g$

$r_p = 10.81cm$

$t_c = 10.81\tan\left(\frac{3.14}{8}\right) + \left(\frac{0.81}{2}\right) = 0.47cm$

**a) Required Coil Area** $(A_c)$ :

$$A_c = \left(\frac{\beta B_{sat} l_g}{f_c J \mu_0}\right)\sqrt{1 + \left(\frac{Fdy\sigma}{F_{\max}\beta}\right)^2} \tag{5}$$

Where,

Saturation flux density, $B_{sat}$ = 1.2T,

Copper current density, $J = 600 A/mm^2$

$A_c$=0.00167m²

***b)*** **length of coil**: Comparing available coil area to the required coil area,

$A_v = \eta A_c$ when $1 \le \eta \le 2$

$A_v = 2A_c = 8cm^2$

$A_v = t_c l_c$

$t_c$ –Thickness of coil, $l_c$ – length of coil

$l_c = 20.4cm$

$$l_c = \sqrt{r_c^2 - \left(\frac{w_p}{2} + t_c\right)^2} - r_p \tag{6}$$

Putting, $r_p$, $t_c$, $l_c$ , $w_p$, in (6),coil space radius, $r_c$ is calculated .

$r_c = 27.84cm$ (Stator inner radius or coil space radius.)

**c) Pole length in radial direction**: Subtracting pole tip radius $r_p = 10.81cm$ through coil space radius $r_c = 27.84cm$ we get radial pole length, $l_p = r_c - r_p$ =17.03 cm

**d) Stator outer radius:**

$$r_s = r_c + f_s w \tag{7}$$

$r_s$ = 28.65 cm

**e) Stator axial length,** $l_s$ : It is sum of Iron length, $l_i$ and coil thickness, $t_c$

$$l_s = l_i + 2t_c \tag{8}$$

$l_s$ =11.6 +2x0. 47 =12.54 cm

**f) Amplifier capacity:** It is detected by slew rate requirement, $\left|\frac{dF}{dT}\right|_{\max}$

$$\left|\frac{dF}{dT}\right|_{\max} = \frac{2I_b V_{\max}}{l_g} \tag{9}$$

Where, $I_b$ –Bias current, $V_{\max}$ – maximum voltage

$$\frac{2I_b V_{\max}}{l_g} = \frac{2\times 0.5\times 200}{0.005} = 4000 \text{ N/s}$$

$$VA_{\max} = \left|\frac{dF}{dt}\right|_{\max}\left(\frac{\eta l_g}{\beta n}\right) = 4000\left(\frac{4\times 0.0005}{0.46\times 8}\right)$$

$$VA_{\max} = 2.17KVA(select 2.4KVA)$$

From user manual[6], for available amplifier capacity 2.4 KVA,we choose amplifier of peak current 30A and peak voltage 80 V, for model 30A8 available in market.

$$NI_{sat} = NI_{\max} = 30N = \frac{B_{sat} l_g}{\mu_0} \tag{10}$$

$N = 29.17 \left(\approx 30 turns\right)$

Table I. Designed dimensions of eight pole bearing.

| parameters | symbol | value |
|---|---|---|
| Gap area, $m^2$ | $A_g$ | 0.00339 |
| Width of pole, cm | $w_p$ | 0.81 |
| Length of pole ,cm | $L_p$ | 11.6 |
| Diameter of Journal ,cm | $d_j$ | 11.62 |
| Bias ratio | $\beta$ | 0.46 |
| Thickness of coil, cm | $t_c$ | 0.47 |
| Pole tip radius ,cm | $r_p$ | 10.81 |
| Length of coil ,cm | $l_c$ | 20.4 |
| Coil space radius , cm | $r_c$ | 27.84 |
| C/s area of coil, $m^2$ | $A_c$ | 0.0016 |
| Radial Pole length, cm | $l$ | 17.03 |
| Stator outer radius, cm | $r_s$ | 28.65 |
| Overall stator diameter, cm | $d_s$ | 57.3 |
| Stator axial length, cm | $l_s$ | 12.54 |
| No. of turns | N | 30 |
| Amplifier capacity, KVA | $VI_{\max}$ | 2.4 |

## III. LOSSES IN RADIAL MAGNETIC BEARING

Ha-Yong Kim and Lee (2002) proposed an analytical expression based on eddy current brake model for eddy current loss. Hetropolar and homopolar AMB with non laminated cores and rotor are compared for verification of test result. Sun Y. and Yu, (2002) studied power loss using drag force acted on rotor and stiffness including eddy current effect from radial force. Sun Y.and Yu, (2002) indicates loss is promotional to lamination thickness and flux density. Finally rotational loss is calculated by integrating resistance loss over volume of lamination. Hu T., Lin Z., and Allaire P. E.(2004) investigate the fundamental reasons behind the performance degradation under actuator allocation strategy. For laminated rotor Meeker D., Filatov A. and Maslen H.(2004) used thin plate assumption to simplify the magnetic field calculation in lamination of journal and power loss could be calculated if the flux density at the journal surface is known. Bakay L., and Dubois M., (2007) studied effect of Cu and Iron losses of optimized eight pole radial AMB on discharge time of no load long term flywheel energy storage. NSSN configuration is used. It concludes that for high discharge time for low loss AMB mass is smaller than in case of low discharge time. Optimal solution is for class of sinusoidal force signal. Also presented static allocation strategy for suboptimal power loss. Hyun and Kang (2008) studied magnetic force to current input relation for new bearing is analyzed with 1D magnetic circuit and 3D magnetic field modeling. A novel permanent magnet biased heteropolar type magnetic bearing is developed. Bakay L., Dubois M., and Ruel J., (2009) optimized AMB to minimize Cu and Iron loss for different magnitude of external force. For the purpose of reducing eddy current loss laminated material is used. For this reason steel M19-29 Ga material has been chosen in both stator and rotor lamination while 304 stainless steel material has been chosen for shaft.

The loss components of the magnetic journal bearing can be summarized as

$$P_{loss} = (P_{cu}) + (P_{iron}) + (P_{mech}) \tag{11}$$

$$P_{loss} = (p_{cu}) + (P_{eddy} + P_{hys}) + (P_{windage} + P_{friction}) \tag{12}$$

Where,

$P_{loss}$ - Total power loss in Watt,

$P_{cu}$ - Copper loss,

$P_{iron}$ - Stator core (iron) loss,

$P_{mech}$ - Mechanical loss,

$P_{eddy}$ - Rotor eddy current loss,

$P_{hys}$ – Hysteresis loss,

$P_{windage}$ - Windage loss.

$P_{friction}$ - Frictional loss(negligible)

### 3.1. Copper Loss Analysis

Copper loss occurs due to resistance to flow of current through coil. Copper loss equation is given by[10]

$$P_{cu,\max} = R_{cu} I_{\max}^2 \tag{13}$$

$$P_{cu,\max} = \rho \eta J^2 A_c V_c \tag{14}$$

Where,

Resistivity, $\rho = 2\times10^{-5}\,\Omega m$; coil packing factor, $\eta = 0.85$;

$$\text{Current density, } J_{\max,\min} = \left(\frac{K_a l_{g_{\max,\min}}}{K_i \eta A_c}\right)\sqrt{\frac{4F_{\max,\min}}{\mu_0 A_g}} \tag{15}$$

$$F_{\max,\min} = (0.25\mu_0 A_g)\left(\frac{K_i n_p i_{\max,\min}}{K_a l_{g_{\max,\min}}}\right) \tag{16}$$

$$l_{g_{\max,\min}} = (l_g \pm x_{\max,\min}) \tag{17}$$

Maximum displacement of rotor in terms of force and displacement stiffness,

$$x_{\max} = (F_{\max} - F)/K_x \tag{18}$$

cross sectional area and the volume of the coil are expressed as

$$A_c = t_c(r_c - r_p)\ ;\ V_c = A_c l_c \tag{19}$$

Hence, constraint becomes,

$$J_{sat} \geq J_{\max}\ ; J_{\min} \geq 0 \tag{20}$$

### 3.2. Iron Core loss

These occur due to variation of flux density in electro-magnetic material. The flux variation create eddy current and magnetic hysteresis in the iron lamination. (a) Eddy current loss depends on time rate of change of flux density. (b) Magnetic hysteresis loss in laminating layer depends on peak value and frequency of flux density. Under alternating flux conditions, the stator core loss density $P_{f_e}$ in W/kg can be separated into a hysteresis $P_h$ and an eddy current component $P_e$, and can be written in terms of the Steinmetz (2007) equation as given below.

$$P_{f_e} = P_h + P_e = K_h B^n f + K_e B^2 f^2 \tag{21}$$

Where,

$K_h$, $K_e$ and $n$ are constants. For silicon Iron laminates $n$=1.8-2.0, $K_h$ = 40-55 Ws/T$^2$m$^3$, $K_e$ =0.004-0.007 Ws/T$^2$m$^3$

#### 3.2.1. Eddy current loss

In high-speed permanent-magnet machine applications, rotor losses generated by induced eddy currents may amount to a major part of the total losses. The eddy currents are mainly induced in the permanent magnets, which are highly conductive, and also in the rotor steel. The eddy current problem can be

solved one-dimensionally by using Maxwell equations[5].
Taking time average of energy, $E_{(t)^2}$ over one period, The eddy current power loss per unit volume is,

$$P_{eddy} = \frac{\sigma \pi^2 f^2 B_{\max}^2 t^2}{6} \tag{22}$$

### 3.2.2. Hysteresis Loss

Since, energy loss in each cycle is proportional to area enclosed by BH curve .i. e. area inside of hystersis curve increases with frequency. Every portion of rotating core passes under S ,N polarity alternatively[7].
Hysteresis loss $p_h$ is directly proportional to frequency of magnetic reversal,

$$P_h = K_h B^n f \tag{23}$$

Where,
For silicon Iron laminates $n$=1.8-2.0, $K_h$ = 45 Ws/T$^2$m$^{3,}$

### 3.3 Mechanical loss

#### 3.3.1 Windage loss[9]

In a simple rotor-stator system if speed increases, Taylor vortices disappear shear stress, $\tau_r$

$$\tau_r = \frac{1}{2} C_f \rho_1 V^2$$

Where,
$C_f$ Friction coefficient, $\rho_1$ ,density of rotor material.
Tangential frictional force on rotor is given as below,

$$F_r = C_f \rho_1 \omega^2 \pi r^3 L \tag{24}$$

Where,
$L$, length of rotor, $r$, radius of rotor.
This frictional force balanced by electromagnetic torque,

$$T_{f_r} = C_f \rho_1 \pi L \omega^2 r^4$$

Using this friction torque of a rotating cylinder we can calculate Wind age loss, $P_w = T_{f_r} \omega$

Hence, $$P_w = C_f \rho_1 \pi L \omega^3 r^4 \tag{25}$$

#### 3.3.2 Frictional power loss

$$P_f = F\left[0.02\left(\frac{\omega}{100}\right) + 0.005B\left(\frac{\omega}{100}\right)^2\right] \tag{26}$$

## IV. OPTIMUM TOTAL LOSS ANALYSIS USING GENETIC ALGORITHM

The parameters most contribute to evolution in genetic algorithm are crossover and fitness based selection/reproduction. Mutation also plays a role in this process[14].
Unlike the standard search techniques, genetic algorithms search among a population of points, work with a coding of the parameter set and use probabilistic transition rules. Populations of m points are chosen initially at random in the search space. The objective function values are calculated at all points and compared. From these points, two points are selected randomly, giving better points higher chances. The selected two points are subsequently used to generate a new point in a certain random manner with occasionally added random disturbance. This is repeated until new points are generated. The generated populations of points are expected to be more concentrated in the vicinity of optima

than the original points. The new population of points, which can again be used to generate another population and so on, yields points more and more concentrated in the vicinity of the optima.

### 4.1 Input parameters

Permeability of vacuum, $\mu_0 = 4\pi \times 10^{-7} H / m$;

Area of gap, $A_g = 0.003m^2$;

Area of coil, $A_c = 0.0016m^2$;

Resistivity, $\rho = 2 \times 10^{-5} \Omega m$;

Lamination conductivity, $\sigma = 7460000W / mc$;

Radius of rotor, $r = 0.03m$;

Length of rotor, $L = 1m$;

Friction coefficient, $C_f = 0.005m$;

Saturated flux density, $B_{sat} = 1.2T$;

Coil mmf .loss factor, $K_i = 1.394$;

Actuator loss factor, $K_a = 1.072$;

Coil packing factor, $\eta = 0.85$;

Electromagnetic force, $F = 350N$;

Maximum volume of coil, $V_{\max} = 100 \times 10^{-6} m^3$;

Maximum copper loss, $P_{\max} = 5000W$;

Iron saturation factor, $\alpha = 0.5$;

Current density, $J_{ub} = 600000A / m^2$;

Basic seed=0.01;

Crossover =0.1;

Mutations=0.01.

### 4.2 Bounds of the variables

$l_{g_{\min}} = 0.0005m, l_{g_{\max}} = 0.004m$;

$f_{\min} = 50rev / s, f_{\max} = 250rev / s$;

$t_{\min} = 0.001m, t_{\max} = 0.004m$;

$B_{\min} = 0.2T, B_{\max} = 1.2T$;

### 4.3 The summary of the formulation of the magnetic bearing design for the single objective optimization

Minimize; $f_i(x) = 1$ where x = $\{l_g, f, t, B\}$

Subject to;

$g_i(x) \geq 0;\ i = 0,1,...9;\ h_k(x) = 0,\ k = 1,2;\ x^p \leq x_p \leq x^p;\ p = 1,....,4.$

Where,

$f(x) = P_{Total}.$

$g_0(x) = J_{sat} - J_{\max}$;

$g_1(x) = J_{\min}$;

$g_2(x) = V_{\max} - V_c$;

$g_3(x) = B_{\min} - \alpha_{\min} B_{sat}$;

$g_4(x) = \alpha_{\max} B_{sat} - B_{\max}$;

$g_5(x) = P_{cu}$;

$g_6(x) = P_{eddy}$;

$g_7(x) = P_{hys}$;

$g_8(x) = Pw$;

$g_9(x) = P_f$;

$h_1(x) = F_{\max} - F\left(l_{g_{\max}}, i_{\max}\right)$;

$h_2(x) = F_{\min} - F\left(l_{g_{\min}}, i_{\min}\right)$;

## V. RESULTS

Results are obtained for following conditions:
Initial population size=100;
Final population=1000;
Generation=1000
Optimum value of copper loss, eddy current loss, hystersis loss, windage, frictional loss to population size 1000 are
14.177W, 4368.47W, 90.2797W, 309.73W, 62.059W respectively.

| Optimum values of variable vectors for population size 100 and run 1 | | | | |
|---|---|---|---|---|
| Variables: | $l_g$ | $B$ | $f$ | $t$ |
| Values: | 0.002587m | 0.05190T | 57.87rev/sec | 0.001128m |

| Optimum values of variable vectors for population size 1000 and run 47 | | | | |
|---|---|---|---|---|
| Variables: | $l_g$ | $B$ | $f$ | $t$ |
| Values: | 0.0015m | 0.0376T | 50rev/sec | 0.001m |

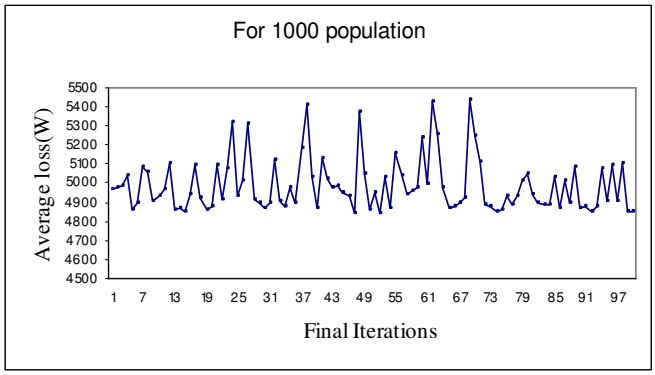


Figure 4. Average loss for final population

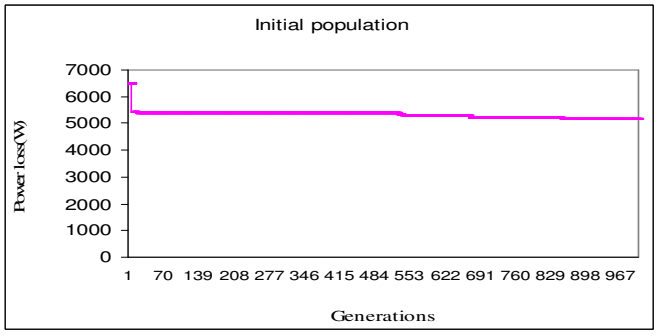


Figure 5. Total power loss showing best fitness for initial population 100.

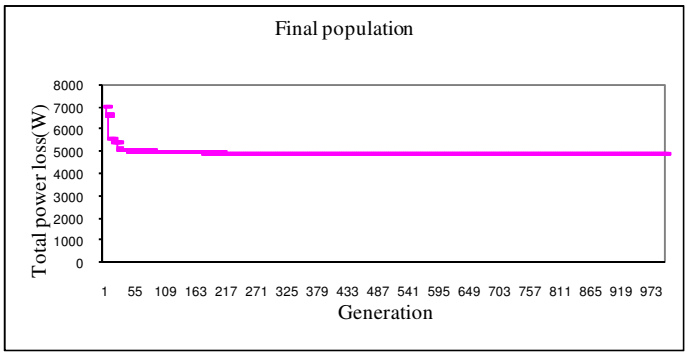


Figure 6. Total power loss showing best fitness for final population 1000.

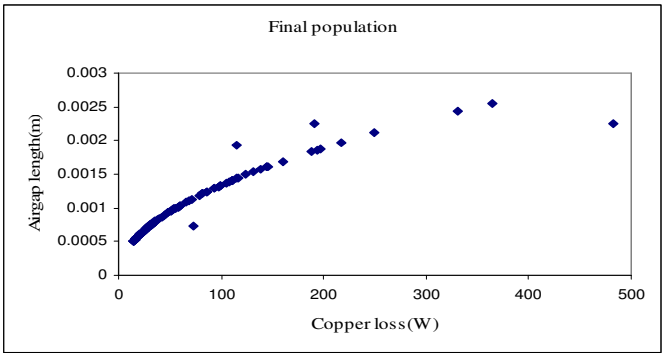


Figure 7. Effect of air gap on copper loss.

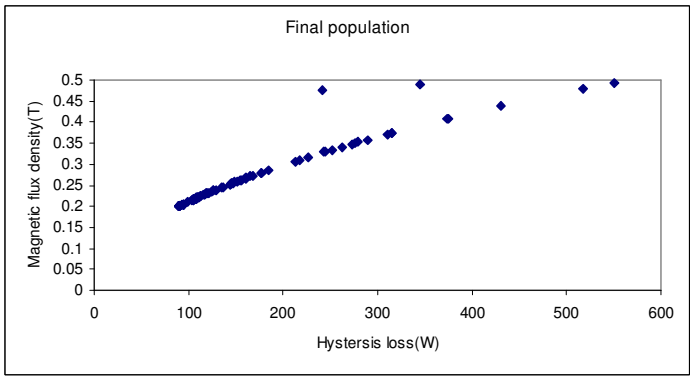


Figure 8. Effect of magnetic flux density on hystersis loss

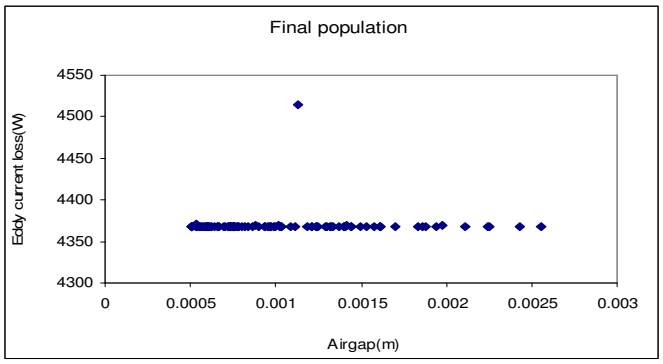


Figure 9. Effect of magnetic flux density on eddy current loss

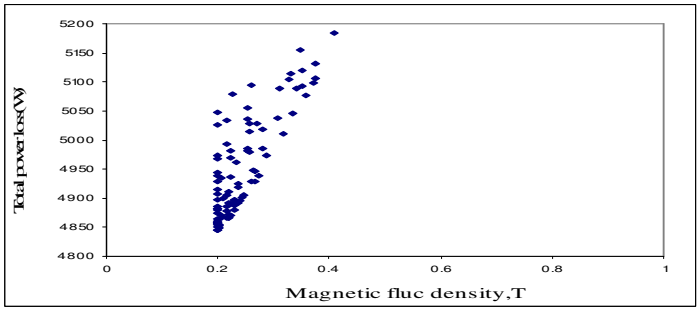


Figure 10. Effect of magnetic flux density on total loss at final population.

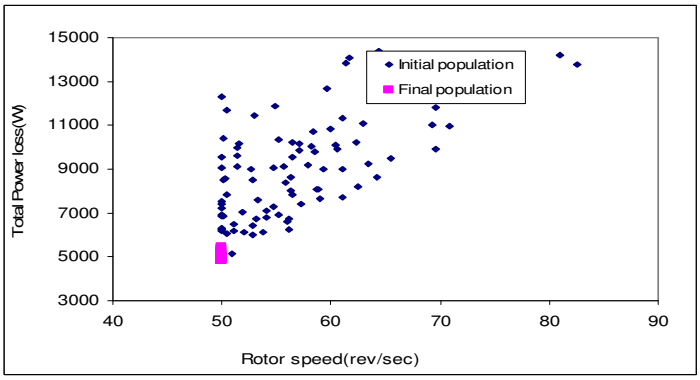


Figure 11. Effect of rotor speed on total loss

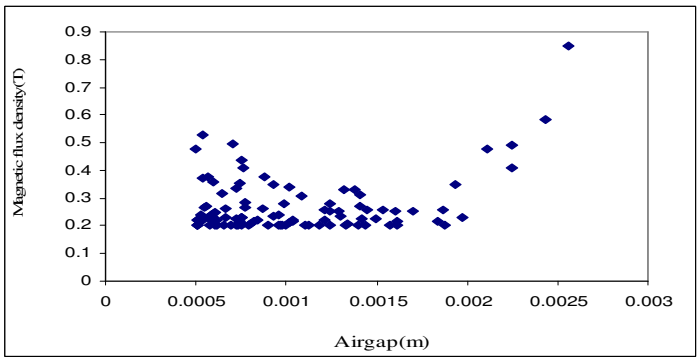


Figure 12. Effect of air gap on magnetic flux density at final population

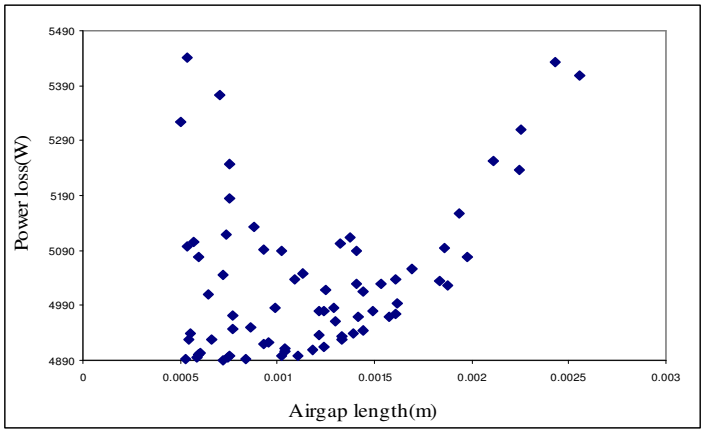


Figure 13. Effect of air gap on total power loss at final population

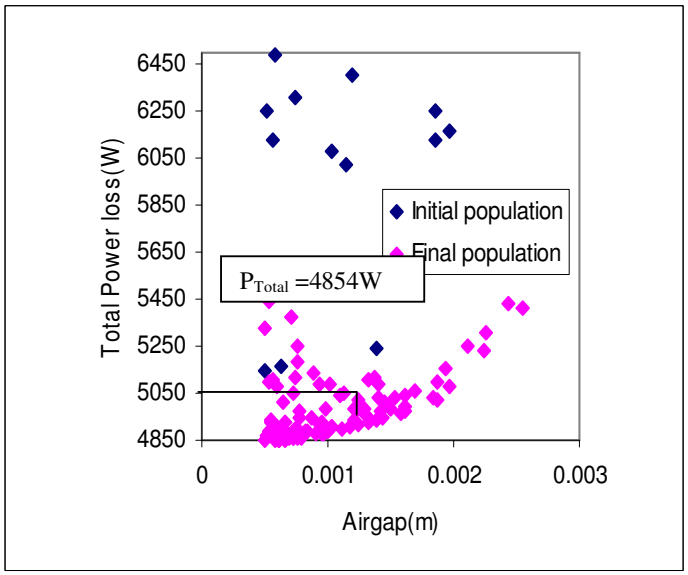


Figure 14. Effect of air gap on total loss for combined initial and final population

## VI. CONCLUSION

All types of losses are considered for finding optimum power loss in eight pole radial magnetic bearing. Most power loss affecting parameters are studied and these are fixed as constraints with bounds. Each loss is simplified in terms of loss affecting variables and objective function is defined as sum of loss variables. Single objective genetic algorithm Optimization tool is used to compute the objective function. Simulation results are obtained for initial population 100 and final population 1000 with 100 runs. Total power loss obtained in each run is plotted as shown in figure 4. Further as shown in figure 5 and 6 the best fitness curve for total loss with 1000 generation is plotted at initial and final population for run 01 and 47 respectively. Selection of these runs based on curve satisfies convergent criteria. Whereas from graphs 7 and 9 we concludes, copper loss increases with increase in air gap ,magnetic flux density plays important role in hysteresis loss which increases proportionally whereas eddy current loss unaffected . From figure 10 to 13 at final population we obtained effect of each variable on total power loss, graphs are convex in nature which satisfies optimum value of each variable. From graph 14, it was found that total power loss initially decreases to 4854W with increase

in air gap unto 0.0015m.But further increase in air gap, total power loss increases. Hence optimum value of total power loss is chosen as 4854 W.

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# REAL TIME ANPR FOR VEHICLE IDENTIFICATION USING NEURAL NETWORK

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## *ABSTRACT*

*This paper deals with problematic from field of artificial intelligence, machine vision and neural networks in construction of an automatic number plate recognition system (ANPR). This paper includes brief introduction of automatic number plate recognition, which ensure a process of number plate detection, processes of proper characters segmentation, normalization and recognition. Automatic Number Plate Recognition (ANPR) is a real time embedded system which automatically recognizes the license number of vehicles. In this paper, the task of recognizing number plate is considered. First the image of number plate is captured by camera. Number plate is segmented by using horizontal and vertical projection. After that feature extraction techniques are used to extract the characters from segmented data. Neural Network algorithms are used to recognize the characters which improve the color and brightness. ANPR project is very much useful in applications like, automated traffic surveillance and tracking system, automated high-way/parking toll collection systems, automation of petrol stations, travelling time monitoring.. In this paper, introduction of number plate segmentation, feature extraction, recognition of character based on Neural Network and syntax checking analysis of recognized characters is described.*

***KEYWORDS:*** *Artificial Intelligence, Neural Networks, Optical Character Recognition, ANPR*

## I. INTRODUCTION

ANPR is a mass surveillance system that captures the image of vehicles and recognizes their license number. Some applications of an ANPR system are, automated traffic surveillance and tracking system, automated high-way/parking toll collection systems, automation of petrol stations, travelling time monitoring.

Such systems automate the process of recognizing the license number of vehicles, making it fast, robust, time- efficient and cost-effective.

### 1.1 ANPR systems as a practical application of artificial intelligence

Massive integration of information technologies into all aspects of modern life caused demand for processing vehicles as conceptual resources in information systems. Because a standalone information system without any data has no sense, there was also a need to transform information about vehicles between the reality and information systems. This can be achieved by a human agent, or by special intelligent equipment which is to be able to recognize vehicles by their number plates in a real environment and reflect it into conceptual resources. Because of this, various recognition techniques have been developed and number plate recognition systems are today used in various traffic and security applications, such as parking, access and border control, or tracking of stolen cars.

In parking, number plates are used to calculate duration of the parking. When a vehicle enters an input gate, number plate is automatically recognized and stored in database. When a vehicle later exits the parking area through an output gate, number plate is recognized again and paired with the first-one stored in the database. The difference in time is used to calculate the parking fee. Automatic number plate recognition systems can be used in access control. For example, this technology is used in many companies to grant access only to vehicles of authorized personnel.

In some countries, ANPR systems installed on country borders automatically detect and monitor border crossings. Each vehicle can be registered in a central database and compared to a black list of stolen vehicles. In traffic control, vehicles can be directed to different lanes for a better congestion control in busy urban communications during the rush hours.

### 1.2 Current systems

ANPR systems have been implemented in many countries like Australia, Korea and few others. Strict implementation of license plate standards in these countries has helped the early development of ANPR systems. These systems use standard features of the license plates such as: dimensions of plate, border for the plate, color and font of characters, etc. help to localize the number plate easily and identify the license number of the vehicle.

In India, number plate standards are rarely followed. Wide variations are found in terms of font types, script, size, placement and color of the number plates. In few cases, other unwanted decorations are present on the number plate. Also, unlike other countries, no special features are available on Indian number plates to ease their recognition process. Hence, currently only manual recording systems are used and ANPR has not been commercially implemented in India.

In this section, we have given brief introduction of Automatic Number Plate Recognition system which is based on Artificial Intelligence and Neural Network. Also explained the applications of ANPR and current trends of ANPR system.

## II. NUMBER PLATE AREA DETECTION

The first step in a process of automatic number plate recognition is a detection of a number plate area. The algorithms that are able to detect a rectangular area of the number plate in an original image. Humans define a number plate in a natural language as a "small plastic or metal plate attached to a vehicle for official identification purposes", but machines do not understand this definition as well as they do not understand what "vehicle", "road", or whatever else is. Because of this, there is a need to find an alternative definition of a number plate based on descriptors that will be comprehensible for machines.

Let us define the number plate as a "rectangular area with increased occurrence of horizontal and vertical edges". The high density of horizontal and vertical edges on a small area is in many cases caused by contrast characters of a number plate, but not in every case. This process can sometimes detect a wrong area that does not correspond to a number plate. Because of this, we often detect several candidates for the plate by different algorithms.

In general, the captured snapshot can contain several number plate candidates. Because of this, the detection algorithm always clips several bands, and several plates from each band. There is a predefined value of maximum number of candidates, which are detected by analysis of projections. By default, this value is equals to nine.

There are several heuristics, which are used to determine the cost of selected candidates according to their properties. These heuristics have been chosen ad hoc during the practical experimentations. The recognition logic sorts candidates according to their cost from the most suitable to the least suitable. Then, the most suitable candidate is examined by a deeper heuristic analysis. The deeper analysis definitely accepts, or rejects the candidate. As there is a need to analyze individual characters, this type of analysis consumes big amount of processor time.

The basic concept of analysis can be illustrated by the following steps:

1. Detect available number plate inputs.
2. Sort them according to their cost which is based on heuristics.
3. Cut the first plate from the list with the best cost.
4. Segment the number plate.
5. Analyze it by a deeper analysis which is time consuming.
6. If the deeper analysis rejects the plate, return to the step 3.

In this section, we have given the introduction of detection of number plates once the image is captured by camera. The basic steps are discussed for analysis of segmentation of number plate

# III. NUMBER PLATE SEGMENTATION

The next step after the detection of the number plate area is a segmentation of the plate. The number plate can be segmented based on horizontal or vertical projection. The segmentation is one of the most important processes in the automatic number plate recognition, because all further steps rely on it. If the segmentation fails, a character can be improperly divided into two pieces, or two characters can be improperly merged together.

We can use a horizontal projection of a number plate for the segmentation, or one of the more sophisticated methods, such as segmentation using the neural networks. If we assume only one-row plates, the segmentation is a process of finding horizontal boundaries between characters. The segment of plate contains besides the character also redundant space and other undesirable elements. We understand under the term "segment" the part of a number plate determined by a horizontal segmentation algorithm. Since the segment has been processed by an adaptive thresholding filter, it contains only black and white pixels. The neighboring pixels are grouped together into larger pieces, and one of them is a character. Our goal is to divide the segment into the several pieces, and keeps only one piece representing the regular character.

The second phase of the segmentation is an enhancement of segments. The segment of a plate contains besides the character also undesirable elements such as dots and stretches as well as redundant space on the sides of character. There is a need to eliminate these elements and extract only the character. The piece chosen by the heuristics is then converted to a monochrome bitmap image. Each such image corresponds to one horizontal segment. These images are considered as an output of the segmentation phase of the ANPR process.

In this section, we have given the introduction of segmentation of number plates once the number plate is detected. For the segmentation of number plate, we have used horizontal and vertical projection.

# IV. FEATURE EXTRACTION

Before extracting feature descriptors from a bitmap representation of a character, it is necessary to normalize it into unified dimensions. We understand under the term "resampling" the process of changing dimensions of the character. As original dimensions of unnormalized characters are usually higher than the normalized ones, the characters are in most cases downsampled. When we downsample, we reduce information contained in the processed image.

There are several methods of resampling, such as the pixel-resize, bilinear interpolation or the weighted-average resampling. We cannot determine which method is the best in general, because the successfulness of particular method depends on many factors. For example, usage of the weighed-average downsampling in combination with a detection of character edges is not a good solution, because this type of downsampling does not preserve sharp edges. Because of this, the problematic of character resampling is closely associated with the problematic of feature extraction.

To recognize a character from a bitmap representation, there is a need to extract feature descriptors of such bitmap. As an extraction method significantly affects the quality of whole OCR process, it is very important to extract features, which will be invariant towards the various light conditions, used font type and deformations of characters caused by a skew of the image.

The description of normalized characters is based on its external characteristics because we deal only with properties such as character shape. Then, the vector of descriptors includes characteristics such as number of lines, bays, lakes, the amount of horizontal, vertical and diagonal or diagonal edges, and etc. The feature extraction is a process of transformation of data from a bitmap representation into a form of descriptors, which are more suitable for computers. If we associate similar instances of the same character into the classes, then the descriptors of characters from the same class should be geometrically closed to each other in the vector space. This is a basic assumption for successfulness of the pattern recognition process.

### 4.1 Feature extraction algorithm

At first, we have to embed the character bitmap $f(x, y)$ into a bigger bitmap with white padding to ensure a proper behavior of the feature extraction algorithm. Let the padding be one pixel wide. Then, dimensions of the embedding bitmap will be $w+2$ and $h+2$.

The embedding bitmap $f'(x, y)$ is then defined as:

$$f'(x,y) = \begin{cases} 1 & if\ x = 0 \vee y = 0 \vee x = w+1 \vee y = h+1 \\ f(x-1, y-1) & if\ \neg(x = 0 \vee y = 0 \vee x = w+1 \vee y = h+1) \end{cases}$$

where $w$ and $h$ are dimensions of character bitmap before embedding. Color of the padding is white (value of 1). The coordinates of pixels are shifted one pixel towards the original position.

The structure of vector of output descriptors is illustrated by the pattern below. The notation $h_j@r_i$ means "number occurrences of an edge represented by the matrix $h_j$ in the region $r_i$".

X= ($h_0@r_0$, $h_1@r_0$,... $h_{n-1}@r_0$, $h_0@r_1$, $h_1@r_1$, ..., $h_{n-1}@r_1$, $h_0@r_{p-1}$, $h_1@r_{p-1}$,..., $h_{n-1}@r_{p-1}$)

We compute the position $k$ of the $h_j@r_i$ in the vector **x** as $k = i.n + j$ , where $n$ is the number of different edge types (and also the number of corresponding matrices).

The following algorithm demonstrates the computation of the vector of descriptors **x:**

```
zerosize vector x
for each region r_i , where i ∈ 0,⋯,ρ −1 do
begin
    for each pixel [x, y] in region r_i do
    begin
        for each matrix h_j, where j ∈ 0,⋯,n −1 do
        begin
            if h_j = [ f'(x,y)      f'(x+1,y)   ]
                     [ f'(x,y+1)    f'(x+1,y+1) ] then
            begin
                let k=i.n +j
                let x_k= x_k+1
            end
        end
    end
end
```

In this section, feature extraction algorithm is explained.

# V. NORMALIZATION OF CHARACTERS

The first step is a normalization of a brightness and contrast of processed image segments. Second step is the characters contained in the image segments must be then resized to uniform dimensions. Third step is, the feature extraction algorithm extracts appropriate descriptors from the normalized characters. The brightness and contrast characteristics of segmented characters are varying due to different light conditions during the capture. Because of this, it is necessary to normalize them. There are many different ways, but this section describes the three most used: histogram normalization, global and adaptive thresholding.

Through the histogram normalization, the intensities of character segments are re-distributed on the histogram to obtain the normalized statistics. The areas of lower contrast will gain a higher contrast without affecting the global characteristic of image.

Techniques of the global and adaptive thresholding are used to obtain monochrome representations of processed character segments. The monochrome (or black and white) representation of image is more appropriate for analysis, because it defines clear boundaries of contained characters.

### 5.1 Adaptive Scheduling

The number plate can be sometimes partially shadowed or non-uniformly illuminated. This is most

frequent reason why the global thresholding fail. The adaptive thresholding solves several disadvantages of the global thresholding, because it computes threshold value for each pixel separately using its local neighborhood.

### 5.2 Chow and Kaneko approach

There are two approaches to finding the threshold. The first is the Chow and Kaneko approach, and the second is a local thresholding. The both methods assumes that smaller rectangular region are more likely to have approximately uniform illumination, more suitable for thresholding. The image is divided into uniform rectangular areas with size of (m x n) pixels. The local histogram is computed for each such area and a local threshold is determined. The threshold of concrete point is then computed by interpolating the results of the sub images.
In this section, character normalization techniques are discussed. Adaptive Scheduling and Chow and Kaneko approach are the techniques which are used to normalization of characters.

## VI. CHARACTER RECOGNITION AND SYNTAX CHECKING

The segmentation algorithm can sometimes detect redundant elements, which do not correspond to proper characters. The shape of these elements after normalization is often similar to the shape of characters. Because of this, these elements are not reliably separable by traditional OCR methods, although they vary in size as well as in contrast, brightness or hue. Since the feature extraction methods do not consider these properties, there is a need to use additional heuristic analyses to filter non-character elements. The analysis expects all elements to have similar properties. Elements with considerably different properties are treated as invalid and excluded from the recognition process.
The analysis consists of two phases. The first phase deals with statistics of brightness and contrast of segmented characters. Characters are then normalized and processed by the piece extraction algorithm. Since the piece extraction and normalization of brightness disturbs statistical properties of segmented characters, it is necessary to proceed the first phase of analysis before the application of the piece extraction algorithm.
In addition, the heights of detected segments are same for all characters. Because of this, there is a need to proceed the analysis of dimensions after application of the piece extraction algorithm. The piece extraction algorithm strips off white padding, which surrounds the character.
Respecting the constraints above, the sequence of steps can be assembled as follows:
1. Segment the plate (result is in figure 6.1.a).
2. Analyze the brightness and contrast of segments and exclude faulty ones.
3. Apply the piece extraction algorithm on segments (result is in figure 6.1.b).
4. Analyze the dimensions of segments and exclude faulty ones.

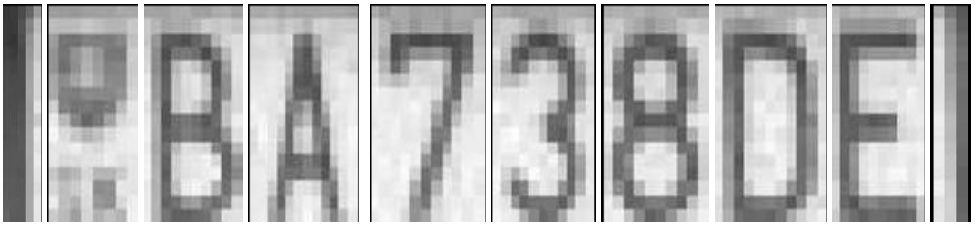

**Figure 6.1 (a):** Character segments before application of the piece extraction algorithm.

**Figure 6.1(b):** Character segments after application of the piece extraction algorithm.

In some situations when the recognition mechanism fails, there is a possibility to detect a failure by a syntactical analysis of the recognized plate. If we have country-specific rules for the plate, we can evaluate the validity of that plate towards these rules. Automatic syntax-based correction of plate numbers can increase recognition abilities of the whole ANPR system.

For example, if the recognition software is confused between characters "8"and "B", the final decision can be made according to the syntactical pattern. If the pattern allows only digits for that position, the character "8"will be used rather than the character "B". This is the most critical stage of the ANPR system. Direct template matching can be used to identify characters. However, this method yields a very low success rate for font variations which are commonly found in Indian number plates.

Artificial Neural Networks like BPNNs can be used to classify the characters. However, they do not provide hardware and time optimization. Therefore statistical feature extraction has been used. In this method, initially the character is divided into twelve equal parts and fourteen features are extracted from every part. The features used are binary edges (2X2) of fourteen types. The feature vector is thus formed is compared with feature vectors of all the stored templates and the maximum value of correlation is calculated to give the right character. Lastly syntax checking is done to ensure that any false characters are not recognized as a valid license number.

In this section, we have discussed how the characters are recognitioned by using Neural Network techniques. Also discussed the syntax analysis techniques once the character is recognitioned.

# VII. RESULTS

ANPR solution has been tested on static snapshots of vehicles, which has been divided into several sets according to difficultness. Sets of blurry and skewed snapshots give worse recognition rates than a set of snapshots, which has been captured clearly. The objective of the tests was not to find a one hundred percent recognizable set of snapshots, but to test the invariance of the algorithms on random snapshots systematically classified to the sets according to their properties.

The table 7.1 shows recognition rates, which has been achieved while testing on various set of number plates. According to the results, this system gives good responses only to clear plates, because skewed plates and plates with difficult surrounding environment causes significant degradation of recognition abilities.

**Table 7.1:** Recognition rates of the ANPR system.

| | Total Number of Plates | Total Number of Characters | Weighted score |
|---|---|---|---|
| Clear plates | 62 | 425 | 88.76 |
| Blurred plates | 41 | 324 | 50.43 |
| Skewed plates | 34 | 264 | 54.26 |
| Average plates | 104 | 1137 | 75.34 |

# VIII. CONCLUSIONS

The system works satisfactorily for wide variations in illumination conditions and different types of number plates commonly found in India. It is definitely a better alternative to the existing manual systems in India.

Currently there are certain restrictions on parameters like speed of the vehicle, script on the number plate, cleanliness of number plate, quality of captured image, skew in the image which can be aptly removed by enhancing the algorithms further.

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# AN EFFICIENT FRAMEWORK FOR CHANNEL CODING IN HIGH SPEED LINKS

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## *ABSTRACT*

*This paper explores the benefit of channel coding for high-speed backplane or chip to chip interconnects, referred to as the high-speed links. Although both power constrained and bandwidth-limited, the high-speed links need to support data rates in the Gbps range at low error probabilities. Modeling the high-speed link as a communication system with noise and inter symbol interference (ISI), this work identifies three operating regimes based on the underlying dominant error mechanisms. The resulting framework is used to identify the conditions under which standard error control codes perform optimally, incur an impractically large overhead, or provide the optimal performance in the form of a single parity check code. For the regime where the standard error control codes are impractical, this thesis introduces low complexity block codes, termed pattern-eliminating codes (PEC), which achieve a potentially large performance improvement over channels with residual ISI. The codes are systematic, require no decoding and allow for simple encoding. They can also be additionally endowed with a (0, n − 1) run-length-limiting property. The simulation results show that the simplest PEC can provide error-rate reductions of several orders of magnitude, even with rate penalty taken into account. It is also shown that channel conditioning, such as equalization, can have a large effect on the code performance and potentially large gains can be derived from optimizing the equalizer jointly with a pattern-eliminating code. Although the performance of a pattern-eliminating code is given by a closed-form expression, the channel memory and the low error rates of interest render accurate simulation of standard error-correcting codes impractical.*

## I. INTRODUCTION

The field of channel coding started with Claude Shannon's 1948 landmark paper [1]. For the next half century, its central objective was to find practical coding schemes that could approach channel capacity (hereafter called Bthe Shannon limit) on well-understood channels such as the additive white Gaussian noise (AWGN) channel. This goal proved to be challenging, but not impossible. In the past decade, with the advent of turbo codes and the rebirth of low-density parity-check (LDPC) codes, it has finally been achieved, at least in many cases of practical interest. Currently, communication bus links in various applications approach Gb/s data rates. Such links are often an important part of multi-processor interconnection [10], processor-to-memory interfaces [11], and SONET/Fibre channels [12], high-speed network switching, and local area networks [13]. It is also likely that many high-speed digital signals will be transmitted between analog and digital chips. Traditionally, system designers have addressed the need for high-speed chip-to-chip links by increasing the number of high-speed signals, which leads to an increase in the cost and complexity of the system. Therefore, the per-pin interconnection bandwidth should be increased. Improving the performance of both parallel and serial interconnects has been an important research area over the last decade [14-16]. Although each type of interconnect has some advantages and disadvantages, the general trend has been toward serial links. However at the same time, significant amount of research has been performed to improve the performance of popular, general purpose parallel buses [17]

## II.CODING FOR THE AWGN CHANNEL

A coding scheme for the AWGN channel may be characterized by two simple parameters: its signal-to-noise ratio (SNR) and its spectral efficiency η in bits per second per Hertz (b/s/Hz). The SNR is the ratio of average signal power to average noise power, a dimensionless quantity. The spectral efficiency of a coding scheme that transmits R bits per second (b/s) over an AWGN channel of bandwidth W Hz is simply η=R/W b/s/Hz. Coding schemes for the AWGN channel typically map a sequence of bits at a rate R b/s to a sequence of real symbols at a rate of 2B symbols per second; the discrete time code rate is then r = R/2B bits per symbol. The sequence of real symbols is then modulated via pulse amplitude modulation (PAM) or quadrature amplitude modulation (QAM) for transmission over an AWGN channel of bandwidth W. By Nyquist theory, B (sometimes called the B Shannon bandwidth [3]) cannot exceed the actual bandwidth W. If B≈W, then the spectral efficiency is

$$\eta = R/W \approx R = B \, ¼ \, 2r. \qquad \text{(II.1)}$$

We therefore say that the nominal spectral efficiency of a discrete-time coding scheme is 2r, the discrete-time code rate in bits per two symbols. The actual spectral efficiency η=R/W of the corresponding continuous-time scheme is upper bounded by the nominal spectral efficiency 2r and approaches 2r as B→W. Thus, for discrete-time codes, we will often denote 2r by η, implicitly assuming B ≈W. Shannon showed that on an AWGN channel with a given SNR and bandwidth W Hz, Shannon showed that on an AWGN channel with a given SNR and bandwidth W Hz, the rate of reliable transmission is upper bounded by

$$R < W \log_2(1+SNR). \qquad \text{(II.2)}$$

Moreover, if a long code with rate R<W log2(1+SNR) . is chosen at random, then there exists a decoding scheme such that with high probability the code and decoder will achieve highly reliable transmission (i.e., low probability of decoding error). Equivalently, Shannon's result shows that the spectral efficiency is upper bounded by

$$\eta < log \; 2(1+SNR) \qquad \text{(II.3)}$$

or, given a spectral efficiency η, that the SNR needed for reliable transmission is lower bounded by

$$SNR > 2\boldsymbol{\eta}\text{-}1 \qquad \text{(II.4)}$$

So, we may say that the Shannon limit on rate (i.e., the channel capacity) is

$$W \log_2(1+SNR) \text{b/s} \qquad \text{(II.5)}$$

or equivalently that the Shannon limit on spectral efficiency is log2(1+SNR) b/s/Hz, or equivalently that the Shannon limit on SNR for a given spectral efficiency η is $^{2}\boldsymbol{\eta}$-1 Note that the Shannon limit on SNR is a lower bound rather than an upper bound. These bounds suggest that we define a normalized SNR parameter SNR norm as follows:

$$\text{SNR norm} = (\text{SNR}/^{2}\boldsymbol{\eta}\text{-}1) \qquad \text{(II.6)}$$

Then, for any reliable coding scheme, SNR norm >1 i.e., the Shannon limit (lower bound) on SNR norm is 1 (0 dB), independent of η. Moreover, SNR norm measures the Bgap to capacity,[ i.e., 10log 10SNRnorm is the difference in decibels (dB)1 between the SNR actually used and the Shannon limit on SNR given η , namely $^{2}\boldsymbol{\eta}$-1 If the desired spectral efficiency is less than 1 b/s/Hz (the so called power-limited regime), then it can be shown that binary codes can be used on the AWGN channel with a cost in Shannon limit on SNR of less than 0.2 dB. On the other hand, since for a binary coding scheme the discrete-time code rate is bounded by r<=1 bit per symbol, the spectral efficiency of a binary coding scheme is limited to $\boldsymbol{\eta} \leq 2r \leq 2$ b/s/Hz, so multilevel coding schemes must be used

if the desired spectral efficiency is greater than 2 b/s/Hz (the so-called bandwidth-limited regime). In practice, coding schemes for the power-limited and bandwidth-limited regimes differ considerably. A closely related normalized SNR parameter that has been traditionally used in the power-limited regime is Eb/N0, which may be defined as

$$Eb/No = SNR/\eta = ((2^{\eta}-1)/\eta)\ SNRnorm \qquad (II.7)$$

For a given spectral efficiency $\eta$ , Eb/N0 is thus lower bounded by

$$Eb/No > ((2^{\eta}-1)/\eta) \qquad (II.8)$$

so we may say that the Shannon limit (lower bound) on Eb/N0 as a function of $\eta$ is $(2^{\eta}-1)/\eta$ This function decreases monotonically with $\eta$ and approaches ln2 as $\eta \to 0$ so we may say that the ultimate Shannon limit (lower bound) on Eb/N0 for any $\eta$ is ln2(-1.59db). We see that as $\eta \to 0$ Eb/N0$\to$ SNRnorm ln 2, so Eb/N0 and SNRnorm become equivalent parameters in the severely power-limited regime. In the power-limited regime, we will therefore use the traditional parameter Eb/N0.

## III. ALGEBRAIC CODING

The algebraic coding paradigm dominated the first several decades of the field of channel coding. Indeed, most of the textbooks on coding of this period (including Peterson [4], Berlekamp [5], Lin [6], Peterson and Weldon [7], Mac Williams and Sloane [8], and Blahut [9]) covered only algebraic coding theory. Algebraic coding theory is primarily concerned with linear (n,k,d) block codes over the binary field F2. A binary linear (n,k,d)block code consists of 2k binary n-tuples, called code words, which have the group property: i.e., the component wise mod-2 sum of any two code words is another codeword. The parameter d denotes the minimum Hamming distance between any two distinct code words, i.e., the minimum number of coordinates in which any two code words differ. The theory generalizes to linear (n,k,d)block codes over non binary fields Fq. The principal objective of algebraic coding theory is to maximize the minimum distance d for a given (n,k). The motivation for this objective is to maximize error correction power. Over a binary symmetric channel (BSC: a binary-input, binary-output channel with statistically independent binary errors), the optimum decoding rule is to decode to the codeword closest in Hamming distance to the received n-tuple. With this rule, a code with minimum distance d can correct all patterns of (d-1)/2 or fewer channel errors (assuming that d is odd), but cannot correct some patterns containing a greater number of errors.

## IV. SYSTEM MODEL

A simplified model of a high-speed link is shown in Fig. 1. The bit stream, which can be coded or uncoded (unconstrained), is modulated to produce the equivalent symbol stream and transmitted over a communication channel. The system employs PAM2 modulation with detection performed on a symbol-by-symbol basis with the decision threshold at the origin. The transmitter and receiver may contain equalizers, in which case the channel's impulse response may contain residual ISI. The two main mechanisms that account for the most significant portion of the residual ISI in high-speed links are dispersion and reflection. In addition, residual interference may also include co-channel interference, caused, for instance, by electro-magnetic coupling (crosstalk). As accounting for co-channel interference involves the same set of mathematical tools as accounting for the ISI, the remainder of the paper focuses on the effects of the ISI.

The quantity of interest is the received signal at the input to the decision circuit at time, denoted Yi and expressed as

$$Yi = Zi + Ni \qquad (IV.1)$$

where Zi denotes the received signal in the absence of noise and is the noise term. Specifically, denoting the channel's pulse response by h -k,…….,h -1,h0 ,……hm where l =k + m + 1 represents the length of the pulse response and h0 is associated with the principal signal component, and letting {Xi} denote a sequence of transmitted symbols, then

Zi= j (IV.2)

The noise term, representing the combined thermal noise and timing jitter, is assumed to be Gaussian with the standard deviation of σ=3mV relative to the peak values of +/-1 V.

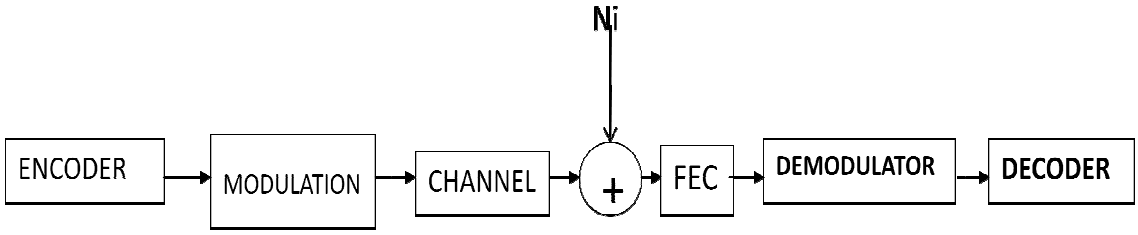


Fig. 1. Simplified model of a high-speed link. Transmit/receive equalization is reflected on the symbol-spaced pulse response.

## V. COST-EFFICIENT SIGNALING SCHEMES

Recently, the noise margin on digital chip-to-chip interconnects has been decreasing for two main reasons. One reason is that supply voltages in digital complementary metal oxide semiconductor (CMOS) processes are decreasing thereby reducing the voltage available for driving I/Os. A second reason is that small signal swings are being used to reduce dynamic power dissipation on high-speed busses. It has long been known that fully-differential signals effectively reject common-mode noise and even-order distortion terms. Since common-mode noise is prevalent on matched printed circuit board (PCB) traces, differential signaling is effective for both voltage [14], [15] and current mode [16] digital chip-to-chip interfaces. Fully differential signals are now used in the Scalable Coherent Interface and RamLink [17] standards. Unfortunately, a practical problem with their implementation is that two signal paths are required for each signal. For example, using fully differential signals for a 64-bit data bus would require 128 pins on each IC package and 128 PCB traces routed between ICs. These additional costs are often prohibitive. Therefore, one important approach is to reduce the required number of pins of interconnects. A signaling scheme that has most of the advantages of fully differential signaling scheme with reduced number of signal paths is proposed in Chapter 3 to help alleviate this problem.

## VI. POWER-EFFICIENT SIGNALING SCHEMES

Multi-level signaling, such as 4-level pulse amplitude modulation (4-PAM), can be used to reduce the required number of signal paths in a link or to increase the data rate of a link. Channel coding can be used to reduce the power consumption of a high-speed inter-chip link by introducing some redundancy at the transmitter. There is still a significant gap between the Shannon limit, the theoretical limit for channel capacity, and the data rates of the current state-of-the-art designs. To find a low-power scheme, channel coding can be employed as an attempt to approach the Shannon limit [1]. Finding codes that can approach Shannon limit is not a complicated task. Indeed, randomly generated codes with a large block size can be used to approach this limit [1]. The problem lies in the fact that while encoding is always a rather simple task, the decoding complexity increases exponentially with the block size, and thus quickly becomes unmanageable. On the other hand, to maintain high system performance, not only high-speed circuits but also low-loss matched transmission lines for interconnect are necessary to ensure good propagation properties such as minimum crosstalk, delay, reflection, and dispersion[17]. Achieving a highly dense system by bringing the chips closer together is only a partial solution since denser systems require denser interconnects, which in turn cause more crosstalk. Indeed, crosstalk is the dominant noise in most microstrip interconnects.

# VII. POWER-EFFICIENT CIRCUIT ARCHITECTURES

Employing circuit techniques for designing the building blocks of a high-speed link is another efficient method to reduce the power and cost of high-speed links[16][17]. The potential benefits of 4-PAM signaling for increasing data rates in physical short-bus systems have been shown. Since there are several drivers in a parallel bus signaling system, the power dissipation of each driver is extremely important. Therefore, power-efficient drivers are desirable. The reported high-speed multi-level drivers have used power-inefficient unipolar architectures.

# VIII. RESULTS

The simulation will vary in the parameter Message Block Length. The message block length is changed in the range: 500, 1000, 2000, 4000 and 8000.

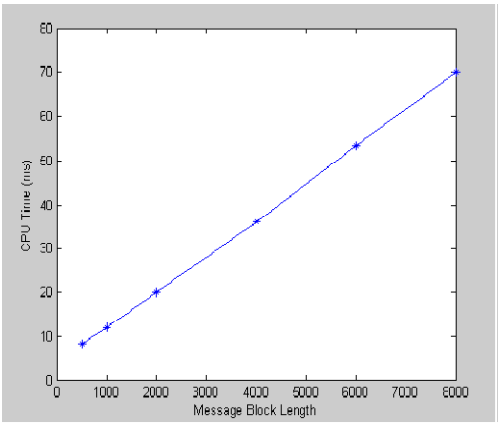


Figure 2: CPU time for generating a n ∗ 2n matrix for different message block lengths and saving it in the row wise.

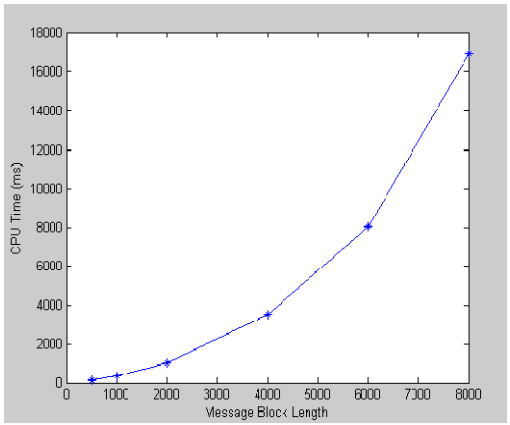


Figure 3: CPU time for generating a n ∗ 2n matrix for different message block lengths and saving it in the row and column wise.

Figure 2 and Figure 3 shows the different CPU time for generating and saving a n ∗ 2n sparse matrix in different manners in software simulation. From the graphs we could see that the CPU time has a linear increasing when saving matrix by row but has a quadratic increasing when saving the matrix by column.

Figure 4 shows the CPU time fore encoding various block length messages. We could see that when the block length increased, the encoding time has a approximate linear increasing. Actually, the encoding time is increasing by $n \cdot \ln(n)$ which is equal to the total amount of degrees. To achieve a linear encoding time, the CHANNEL code should be extent to initial code by involving appropriate pre-coding algorithms.

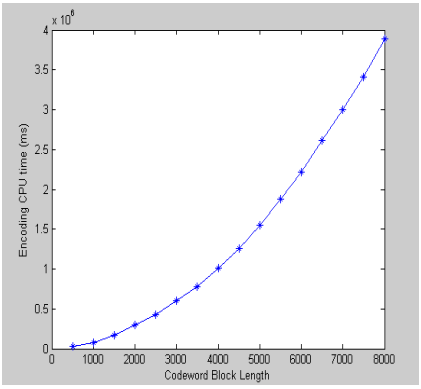


Figure 4: CPU time for encoding various block length messages.

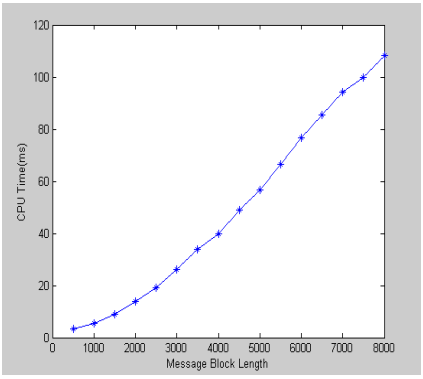


Figure 5: CPU time for decoding various block length messages symbols in the encoding process.

But the number of codeword symbols are decoded is non-fixed and depends on the binary erasure rate. Note that both the encoding time and decoding time we have shown in Figure 4 and Figure 5 does not include the time for generating the sparse matrix.

## IX. CODING PERFORMANCE ANALYSIS

In this section, we are focus on the coding performance of CHANNEL codes. The simulations are based on three main parameters: Block Length, Binary Erasure Rate and Code Rate. Two sets of simulations are built. The first one is based on a binary erasure channel with arbitrary binary erasure rates. The second one is based on a AWGN channel with modified BPSK modulation method

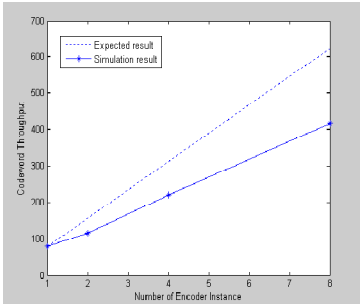


Figure 6: Throughput of parallel encoder

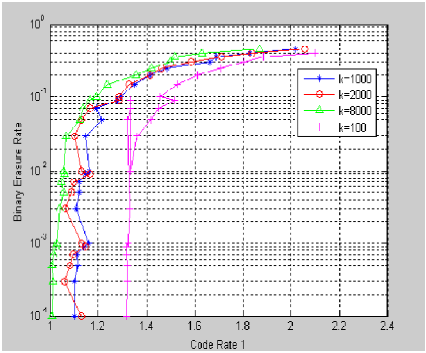


Figure 7: Average code rate for decoding messages with various block length.

In the first simulation, CHANNEL coding is performed on a Binary Erasure Channel with arbitrary binary erasure rates. The block length is changed in the range: 100, 1000, 2000 and 8000. The binary erasure rate is changed in the range: 0.0001, 0.0003, 0.0005, 0.0007, 0.0009, 0.001, 0.003, 0.005, 0.007, 0.009, 0.01, 0.03, 0.05, 0.07, 0.09, 0.1, 0.15, 0.25, 0.3, 0.35 and 0.4. The simulation shows the average code rate for decoding various block length messages. When the binary erasure rate becomes bigger, the codes with different block length have similar behaviors.

The second sets of simulation are based on AWGN channel with modified BPSK modulation method. One new parameter is used here: Threshold which implies how many received symbols will be declared as "erasures" after demodulation. The threshold is changed in the range: 0.2, 0.5, and 0.8.

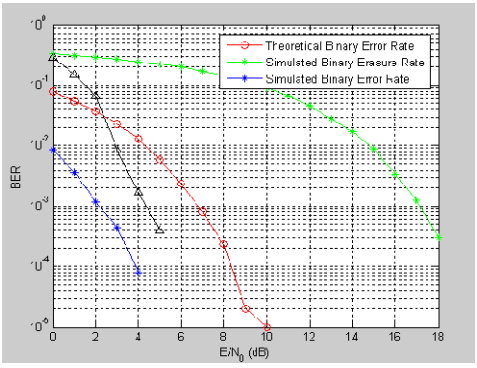


Figure 8: CHANNEL Coding over AWGN channel and modified BPSK modulation with threshold 0.3.

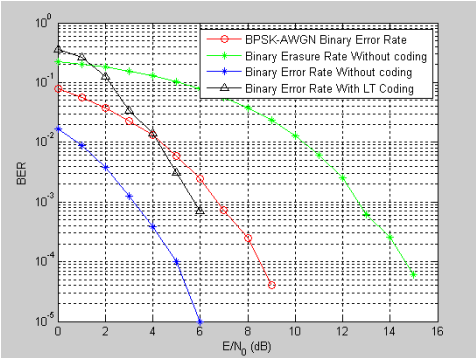


Figure 9: CHANNEL Coding over AWGN channel and modified BPSK modulation with threshold 0.5.

The bigger the threshold is, the less the received symbols will be "erasured". Figure 7, Figure 8 and Figure.9 shows the simulation results for the different sets of parameters. From these graphs we can see that the CHANNEL coding cannot correct any binary errors, whereas it actually increases the binary error rates by about ten times. However, when the binary error rate decreased, the CHANNEL code can still have some coding gains. When we compare Figure and Figure we can see that by lowing threshold in modified BPSK Modulation, we can decrease the binary error rate to get more coding gains. But at the same time we increased the binary erasure rate so the CHANNEL code will have a lower code rate. In Figure 10 we compared three 1000-bits CHANNEL codes with a (255, 223, 32) block code and the non-coding code. We can see that the block code is over-performed than the CHANNEL codes. However, considering the block code may have a longer coding time, e.g. RS code

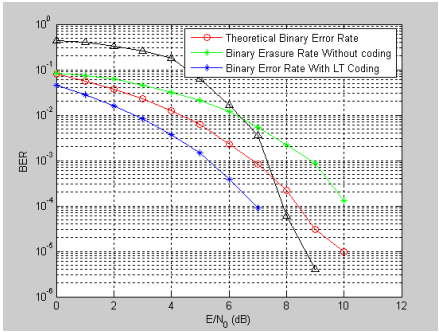


Figure 10: CHANNEL Coding over AWGN channel and modified BPSK modulation with threshold 0.8.

## X. CONCLUSION:

Modeling a high-speed link as an ISI-limited system with additive white Gaussian noise allows for an abstracted framework suitable for a more theoretical approach to studying the benefit of coding for high-speed links. Possible error mechanisms are categorized according to three regimes- the large noise, the large-set-dominant and the worst-case-dominant—which are entirely specified by the system's noise level and the channel's pulse response. In the large-noise and large-set-dominant regimes, classical coding theory provides an exhaustive characterization of different error-control codes, whose hardware complexity has already been partially addressed. While the worst-case-dominant regime occurs rarely in a high-speed link, the quasi-worst-case dominant regime is shown to occur. However, further work is required on extending the pattern-eliminating properties to deal with a wider range of operating conditions. In particular, one of the remaining problems consists of identifying or developing suitable equalization or channel conditioning techniques that optimize the performance of a pattern-eliminating code. Such equalization is, in principle, significantly more power-efficient compared to that employed in current high-speed links, as the equalizer no longer needs to ensure a low error probability. The corresponding scheme could potentially yield significant

benefits for high-speed links by enabling the communication at higher data rates than those achieved previously, or by providing the same signaling speeds at greater energy efficiency.

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# TRANSITION METAL CATALYZED/NaBH4/MeOH REDUCTION OF NITRO, CARBONYL, AROMATICS TO HYDROGENATED PRODUCTS AT ROOM TEMPERATURE

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***ABSTRACT***

*Reduction of nitrobenzene, 4-ethyl nitrobenzene, 4-isopropyl nitrobenzene, 4-nitro 1-phenyl acetate, acetophenone, with $CuCl_2$/MeOH/$NaBH_4$ provided hydrogenated products in quantitative yields. In order to evaluate the best catalytic systems various transition metal catalysts were examined for the first time and $CuCl_2$ catalysts was superactive system. And a solvent system was also studied with methanol being the best solvent evolved. The reactions were exceedingly clean with no byproduct formation, negating the need for further purification. Most reactions provided moderate to excellent yields.*

***KEYWORDS:*** *Reduction, $CuCl_2$, $NaBH_4$, nitrobenzene, aniline.*

## I. INTRODUCTION

The pioneering discovery by Brown describing the use of Ni borides in accelerating $CuCl_2$-mediated reactions has resulted in widespread applications of $NiCl_2$-$NaBH_4$ catalysts. This combination is utilized in several reduction reactions. Due to its ability to enhance reaction outcomes, $NaBH_4$ is the preferred reducing agent in $CuCl_2$-mediated reactions.

Homogeneous catalysts have attracted interest for reductions reactions due its conversions and high selectivity [1,2]. H.C. Brown [3] and A. Rahman [4] co-workers have explored the use of Ni-Boride[3], Ni-Boride silica catalysts[4,5] Au complexes[6], Ni[7],Pt, Ru[8], Fe[9] for reduction of nitroaromatics, and other aromatics to hydrogenated products at room temperature and at low temperature (0-5$^{o}$C) methanol co-solvents in reduction reactions.

Comparison with other reported protocols with Pd, Ni complexes, Ru, Rh[4] using raney nickel catalysts (which is pyrophoric) reveals some interesting trends were observed with longer reaction times, use of sophisticated instruments, high pressure, temperature precludes the wide use of these reagents and conditions.

The effects of water and DMPU[2] in the reduction of ketones. These additives have proven to be useful in several reactions but unfortunately do not have the broad applicability of HMPA, and as a consequence, the search for an alternative is ongoing. The major drawback of using HMPA is carcinogenic. The use of $SmI_2$/$H_2O$/$Et_3N$ mixture in the reduction of ketones [10,11]. The use of the above mentioned catalysts requires stringent conditions and the authors developed a new CuCl2 /NaBH4 system for these reduction reactions. These reactions are instantaneous and provide yields of reduced products. The author studied the comparison of the $H_2O$/$NaBH_4$ method and the $NaBH_4$/MeOH method in reduction of ketones indicates that MeOH/$NaBH_4$/$CuCl_2$ is approximately 100 times faster. This method has also been applied in the reduction of nitroaromatics, ketones,

aldehydes, olefins. These examples clearly show the utility of $CuCl_2$/MeOH/$NaBH_4$ mixtures in reduction of several functional groups.

# II. EXPERIMENTAL SECTION:

## 2.1 Materials Used:

All these materials were purchased from fluka company, $CuCl_2$, $NaBH_4$, EtOH, MeOH, ethylacetate, THF.

## 2.2 Experimental Procedure:

In a 25 ml single neck round bottom flask 5ml of methanol is added to 2mmol substrate to it $CuCl_2$ and $NaBH_4$ is added with more 5 ml of MeOH and the reaction mixture is stirred for 5-10min monitoring through TLC. Upon completion of reaction mixture it is quenched with water and extracted with organic solvent ethyl acetate upon evaporation of ethyl acetate affording product which is subjected to column chromatography affording pure product which is analyzed by GC, H NMR and compared with the standard samples.

# III. RESULTS AND DISCUSSION:

Moreover, they provide better yields and require less time than the HMPA/alcohol systems. The workup and the subsequent purification of the products are straight forward during the course of the reaction. Therefore, the combination of $CuCl_2$/$NaBH_4$/MeOH provides an excellent alternative to HMPA[12-17] in $SmI_2$-based reactions.

Initial mechanistic studies show that water and $NaBH_4$ do not accelerate the reactions separately. The acceleration is a result of the $CuCl_2$/$NaBH_4$/MeOH mixture.

Other borohydrides such as $KBH_4$, $KCNBH_4$ have the same effect as $NaBH_4$ but required more quantity of these borides for the reaction to be completed compared to $NaBH_4$, while replacement of water by alcohols has a deleterious impact on the rates of reduction. It has been proposed that rapid precipitation of $Cu(OH)_3$ and $NaBH_4$, provides the driving force for the reduction[11-12]. To expand the applicability of the $CuCl_2$/MeOH/$NaBH_4$ reagent and to determine its general utility in important single electron- transfer-promoted reactions, the reduction of nitro aromatics to aromatic amines was studied. Recent work in our laboratory has shown that solvation also plays an important role in determining the outcome of these reductions[13]. In order to check the best suitable solvents the author analyzed with $H_2O$, MeOH, ethanol and THF for reduction of nitroaromatics in four solvents showed that, in most cases, MeOH provided superior solvent for reduction reactions over ethanol, THF and $H_2O$.

Transition metal chemistry have attracted interest for chemists over decades for hydrogenation reactions, since the nature of metals is known to influence its outcome in $CuCl_2$/MeOH/$NABH_4$-mediated reactions a series of lewis acid catalysts $ZnCl_2$, $ZnNO_3$,$CuSO_4$,$CuNO_3$, $CaCl_2$, $BaCl_2$,$CoCl_2$, $FeSO_4$, $FeCl_3$, $MgCl_2$, $BiNO_3$, [14-16] were used for nitrobenzene reduction to evaluate the best catalytic system. With these systems only starting material was recovered upon continuation of reaction for 24 h. From these results its evident that the best catalytic system was $CuCl_2$ based lewis acid system the results are presented in table 1.

Table 1 Reduction of nitrobenzene to aniline with various lewis acids with $NaBH_4$ in MeOH at room temperature.

| S. No | Catalysts | Time | Conversion% | Result |
|---|---|---|---|---|
| 1. | $ZnCl_2$ | 20h | - | No reaction |
| 2. | $CuSO_4$ | 20m | 96 | |
| 3. | $Cu(NO_3)_2$ | 20m | 96 | |
| 4. | $CaCl_2$ | 20h | 20 | |
| 5. | $BaCl_2$ | 24h | - | No reaction |
| 6. | $CoCl_2$ | 24h | - | No reaction |

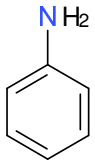
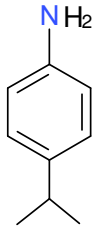
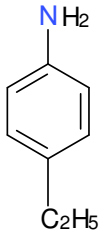
| | | | | |
|---|---|---|---|---|
| 7. | $FeSO_4$ | 24h | - | No reaction |
| 8. | $FeCl_3$ | 24h | - | No reaction |
| 9. | $MgCl_2$ | 24h | - | No reaction |
| 10. | $Bi(NO_3)_2$ | 20h | 30 | |

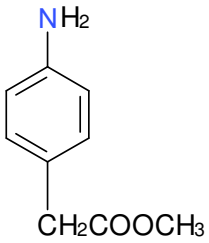
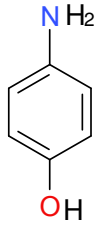
# Means duplicate runs

The results obtained with Cu lewis acids catalysts encouraged the author to run reactions with a series of substituted aromatics were reduced to hydrogenation products presented in table 2. 4-Isopropyl nitrobenzene, 4-Ethyl nitrobenzene, 4-Nitro-1-phenylacetate, acetophenone, 4-nitrophenol, 1-nitronaphthalene. These reactions were performed at room temperature, and all the reactions were completed within 5-10min after 5 min of addition of the $NaBH_4$ to $CuCl_2$. The products were determined by gas chromatography, and utilizing the protocol described by A Rahman[2].

All reactions were quantitative, and the precipitation of byproducts $Cu(OH)_3$ made purification quite simple. Filtration of the precipitate and extraction with organic solvent then evaporating the solvent on rotary evaporator provided clean product, and no further purification was necessary. Inspection of the results in Table 2 shows a number of interesting trends. Most reactions provided selective product.

Table 2 Reduction of substituted aromatics to hydrogenated products with $CuCl_2/NaBH_4$/MeOH at room temperature.

| S. No | Substrates | Time | Conv% | Products |
|---|---|---|---|---|
| 1. | $C_6H_5$-$NO_2$ | 5 min | 98 |  |
| 2. | $(CH_3)_2$-CH-$C_6H_5$-$NO_2$ | 10 min | 90 |  |
| 3. | 4-$C_2H_5$-$C_6H_4$-$NO_2$ | 5 min | 95 |  |
| 4. | 4-$NO_2$-$C_6H_4$-$CH_2COOCH_3$ | 10 min | 80 | |

| | | | | |
|---|---|---|---|---|
| 5. | $C_6H_5$-$COCH_3$ | 5 min | 98 |  |
| 6. | 4-HO-$C_6H_4$-$NO_2$ | 5 hr | 50 |  |
| 7. | $C_{12}H_{10}$-$NO_2$ | 5min | 97 | $C_{12}H_{10}$-$NH_2$ |

# Means duplicate runs

All the substrates were reduced with greater selectivity by $CuCl_2$/MeOH/$NaBH_4$ but with entry no 6 showed less conversion to 50% in 5h duration this owing to its hydroxyl group present at the para position. It's important to assess various mechanistic scenarious responsible for reaction outcomes so that practitioners can make judicious choices best suited to their system of interest. The reduction of ketones by $CuCl_2$ in the presence of proton sources likely proceeds through a House-type mechanism,[16 ]and recent mechanistic work has shown that the rate-limiting step is the first proton transfer to the initially formed ketyl radical anion[17-25]. The radical produced after protonation of the ketyl is reduced to a carbanion by a second equivalent of Cu (II).

## IV. CONCLUSION

Nitrobenzene, substituted nitro benzene and other aromatics was reduced to aniline with $CuCl_2$/$NaBH_4$/MeOH system in 5min and various transition metal lewis acid catalysts were examined for this transformation and the best catalytic system evolved to be $CuCl_2$. And variety of substrates were reduced to its hydrogenated product notable being 4-Isopropyl nitrobenzene, 4-ethyl nitrobenzene, 4-nitro-1-phenyl acetate and 1-nitro naphthalene. Methanol was the best solvent evolved among other solvents tested THF, EtOH and $H_20$. Regardless of the exact mechanistic details of the present reductions, the data presented herein show the utility and ease of $CuCl_2$/MeOH/$NaBH_4$

reducing system in the reduction reactions. This methodology is simple, economic, eco friendly and requires less time for the reaction to complete.

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# PERFORMANCE COMPARISON OF TWO ON-DEMANDS ROUTING PROTOCOLS FOR MOBILE AD-HOC NETWORKS

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## *ABSTRACT*

*Mobile Ad-hoc networks are the collection of mobile nodes connected by a wireless link, where each node acts as a router. Ad-hoc networks are characterized by a lack of infrastructure, and by a random and quickly changing network topology: thus the need for a robust dynamic routing protocol that can accommodate such an environment. In addition to this routing protocols face many challenges like short battery backup, limited processing capability. Two protocols AODV and DSR have compared in terms of number of routes selected, number of hop counts, number of RREQ packets and number of RREP packets. Simulation results shows that AODV compared with DSR reduces the number of hop count nodes, we will also see that AODV has less number of routes as compare to DSR, which helps AODV to be more efficient and less bulky. While comparing route request packets AODV is again better with good some of packets which made it more efficient in finding a new route and each time in replacing a stale link.*

***KEYWORDS:*** *Ad-hoc networks, Performance, AODV, DSR, Routing protocols.*

## I. INTRODUCTION

A Mobile Ad-hoc Network (MANET) [2] is an autonomous network that can be formed without any established infrastructure. As these networks are rapidly deployable and they don't rely on external infracture, it makes them an ideal candidate for rescue and emergency operations, military operations in the battlefield etc .The routing protocols for MANET can be categorized into two main types: reactive and proactive. In case of proactive protocols like DSDV, STAR and GSR [2] the nodes in the adhoc network must keep track of all the routes to all other nodes. In case of reactive routing protocols such as DSR, AODV, ABR and SSA, a lazy approach is applied. The nodes do not keep the routes to all other nodes. Thus, there is no need of constant replacement of routing information between nodes which results to save limited battery power of the nodes. To find out the routes to the destinations on demand flooding of route query packets on whole network is being done. In this paper we carry out a systematic performance [3] study of the two routing protocols for mobile ad-hoc network – Ad-hoc On Demand Distance Vector Routing (AODV) and Dynamic Source Routing (DSR) protocol. We have used the means of simulation using QualNet 5.0(evaluation version) to gather data about these routing protocols in order to evaluate their performance.

This work is ordered as follows. We described the related work in section 2 and simulation model in Section 3. Section 4 details the key performance metrics used in the study. In Section 5 we present the simulation results and analysis of our observation. Finally Section 6 concludes the paper and defines topics for further research.

## II. RELATED WORK IN MANET PROTOCOLS:

The key issue with ad-hoc networking is how to send a message from one node to another with no direct link. The nodes in the network are moving around randomly, and it is very difficult that which nodes are directly linked together. Same time topology of the network is constantly changing and it is very difficult for routing process. A number or routing protocols are available at present; some of them are taken here for discussion purpose.

### 2.1. Types of MANET Routing

Nodes in MANET function as routers that discover and maintain routes to other nodes in the network. The primary goal in ad-hoc network is to establish a correct and efficient route between a pair of nodes and to ensure the correct and timely delivery of packets. The protocols for routing can be classified as:

**2.1.1 Proactive/Table-Driven Routing Protocols:** In proactive routing protocols, each node maintains routing information to every other node in the network. The routing information is usually kept in a number of different tables. These tables are periodically updated and/or if the network topology changes. The difference between these protocols exists in the way the routing information is updated, and the type of information kept at each routing table. Keeping routes to all destinations up-to-date, even if they are not used, is a disadvantage with regard to the usage of bandwidth and of network resources. It is also possible that the control traffic delays data packets, because queues are filled with control packets and there are more packet collisions due to more network traffic. Proactive protocols do not scale in the frequency of topology change. Therefore the proactive strategy is appropriate for a low mobility network.

**2.1.2. Reactive/ On-Demand Routing Protocols:** These protocols were designed to overcome the wasted effort in maintaining unused routes. Routing information acquired only when there is a need for it. The needed routes are calculated on demand. This saves the overhead of maintaining unused routes at each node, but on the other hand the latency for sending data packets will considerably increase. It is obvious that a long delay can arise before data transmission because it has to wait until a route to the destination is acquired. As reactive routing protocols flood the network to discover the route, they are not optimal in terms of bandwidth utilization, but they scale well in the frequency of topology change. Thus this strategy is suitable for high mobility networks. Reactive protocols can be classified into two categories, Source routing and Hop-by-hop routing. In Source routed on-demand protocols, each data packets carry the complete source to destination address. Therefore, each intermediate node forwards these packets according to the information kept in the header of each packet. This means that the intermediate nodes do not need to maintain up-to-date routing information for each active route in order to forward the packet towards the destination. Furthermore, nodes do not need to maintain neighbor connectivity through periodic beaconing messages neighbors through the use of beaconing messages. In hop-by-hop routing (also known as point-to-point routing), each data occurs by coding route request packets through packet only carries the destination address and the next hop address. Therefore, each intermediate node in the path to the destination uses its routing table to forward each data packet towards the destination. Here we are discussing two on-demand routing protocols for MANET.

*A*. ***The Ad-hoc On Demand Distance Vector*** (AODV) routing algorithm is a routing protocol designed for ad-hoc mobile networks. It can perform both unicast and multicast routing. AODV is an on demand algorithm, meaning that it builds routes between nodes only as desired by source nodes. Here the routes are maintained as long as they are needed by the sources. Furthermore, it forms trees which connect multicast group members. AODV uses sequence numbers to ensure the freshness of routes. It is loop-free, self-starting, and scales to large numbers of mobile nodes [5]. AODV makes routes by a route request / route reply message packets. When a source node desires a route to a destination for which it does not already have a route, it broadcasts a route request (RREQ) packet across the network [6]. Nodes receiving this packet update their information for the source node and set up backwards pointers to the source node in the route tables. Along with the source node's IP address, current sequence number, and broadcast ID, the RREQ also contains the most recent sequence number for the destination. A node may send a route

reply (RREP) message after receiving the RREQ if it is either the destination or if it has a route to the destination with corresponding sequence number greater than or equal to that contained in the RREQ. If this is the case, it unicasts a RREP back to the source. Otherwise, it rebroadcasts the route request message (RREQ). Nodes keep track of the RREQ's source IP address and broadcast ID. If they receive a RREQ which they have already processed, they discard the RREQ and do not forward it.

***B***. ***Dynamic source routing*** (DSR) is an on demand routing [9] protocol which is designed for the purpose of multihop wireless networks. DSR contains two mechanisms of route discovery and route maintenance. The route discovery [19] phase initiate when source does not know route to the destination. Route cache [20] is also maintained for the purpose of storing old routes. When source sends a message to destination it first search it into the route cache if not found it generates a RREQ message and work in RREQ/RREP fashion. The DSR protocol allows nodes to dynamically discover a *source route* across multiple network hops to any destination in the ad hoc network. Each data packet sent then carries in its header the complete, ordered list of nodes through which the packet must pass, allowing packet routing to be trivially loop-free and avoiding the need for up-to-date routing information in the intermediate nodes through which the packet is forwarded. By including this source route in the header of each data packet, other nodes forwarding or overhearing any of these packets may also easily cache this routing information for future use.

**2.1.3 Hybrid Routing** The combinations of reactive and proactive protocols are called Hybrid protocols. It takes advantages of these two protocols and as a result, routes are found very fast in the routing zone. Zone Routing Protocol (ZRP) is an example of Hybrid protocol.

# III. SIMULATION MODEL:

We have used a detailed simulation model based on QualNet 5.0 (evaluation version), with GUI [10] tools for system/protocol modeling. The simulator contains standard API for composition of protocols across different layers. QualNet support a wider range of networks and their analysis, some of them are MANET, QoS, Wired Networks, Satellite and cellular.

# IV. PERFORMANCE METRICS:

We have primarily selected the following four performance metrics in order to study the performance comparison of AODV and DSR [11].

**1.** ***Number of route selected***: This is defined as the number of routes offered by a routing protocol for an upcoming request.

**2**. ***Number of Hop count***: This is defined as the number of intermediate nodes between a source and destination.

**3**. ***Number of route request packets (RREQ)***: This is defined as the number of route requesting packets used by a routing protocol to establish a connection between source and destination.

**4.** ***Number of route reply packets (RREP)***: This defined as the number of route replying packets as a result of RREQ packets.

# V. SIMULATION RESULTS AND ANALYSIS:

For doing our analysis we have chosen some set of parameters to make the comparison between two exiting protocols. The table1 summarizes the simulation parameters that we have selected in order to evaluate the performance of the two routing protocols AODV and DSR; Simulation area size-1500 x 1500; [24] Mobility model-Random way point; Traffic type-Constant bit rate (CBR) [13]; Max speed-30m/sec.

**Table1. Simulator Parameters**

| Configured Parameters : | |
|---|---|
| Physical Layer Protocol | 802.11 |
| Routing protocol | AODV, DSR |
| Fading Model | Rayleigh |
| Shadowing Model | Constant |
| Energy Model | Linear |
| Battery power | Simple Linear |
| Area | 1500X1500 |
| Mobility | Random way point |
| Mobility Speed | 0-30mps |
| Data Link Layer | 802.11.DCF |
| Application Layer | CBR Traffic |

Our simulation [14] experiments show the following different results for our four performance measuring parameters.

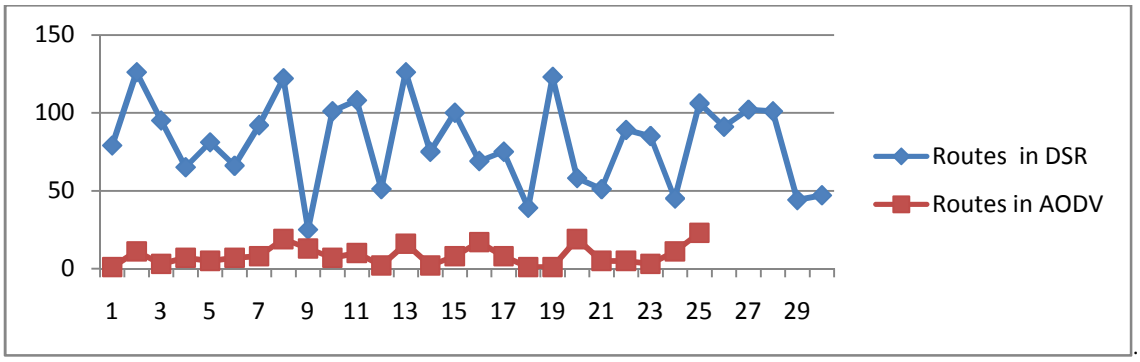


*Figure 1. Number of routes selected by AODV and DSR*

Figure1. gives the comparison between Routes selected by both reactive routing protocols. Considering the various configured parameters it has been observed that the AODV routing protocol uses on demand approach for finding routes. The major difference between AODV and DSR stems out from the fact that DSR uses source routing in which a data packet carries the complete path to be traversed, while in AODV the source node and the intermediate node stores the next hop information corresponding to each flow data packet transmission.

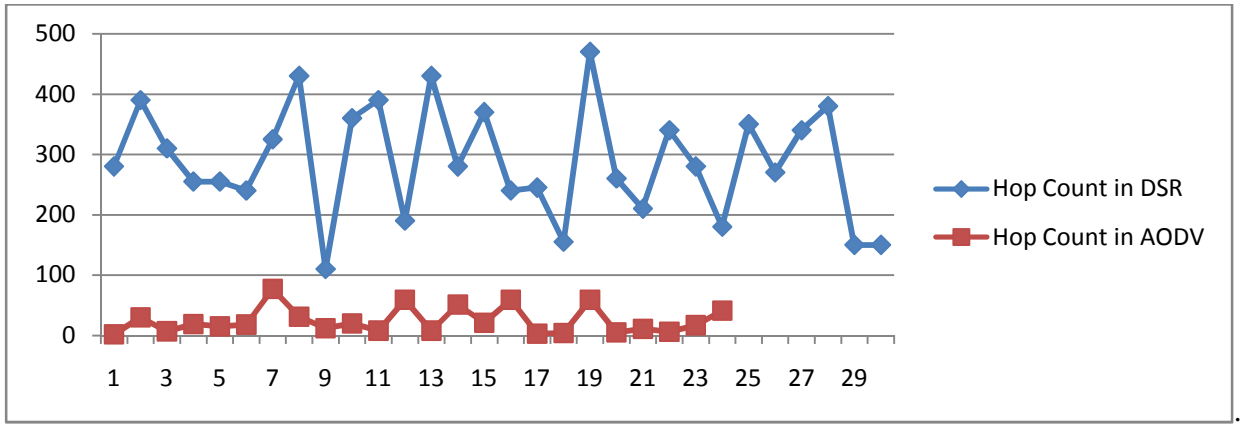


*Figure 2. Comparison of Hop counts given by AODV and DSR*

We see that AODV has less number of routes as compare to DSR, which helps AODV to be more efficient and less bulky [15]. Figure 2 is the comparison of Hop counts chosen by AODV and DSR.
Here again we see that AODV has less number of intermediate [16] (nodes between source and destination) nodes in comparison to DSR, which shows its efficient behavior [18] as we know that more are the intermediate nodes more is the chance of path break [17] and insecure network along with high energy consumption [19] per message transfer by a node.

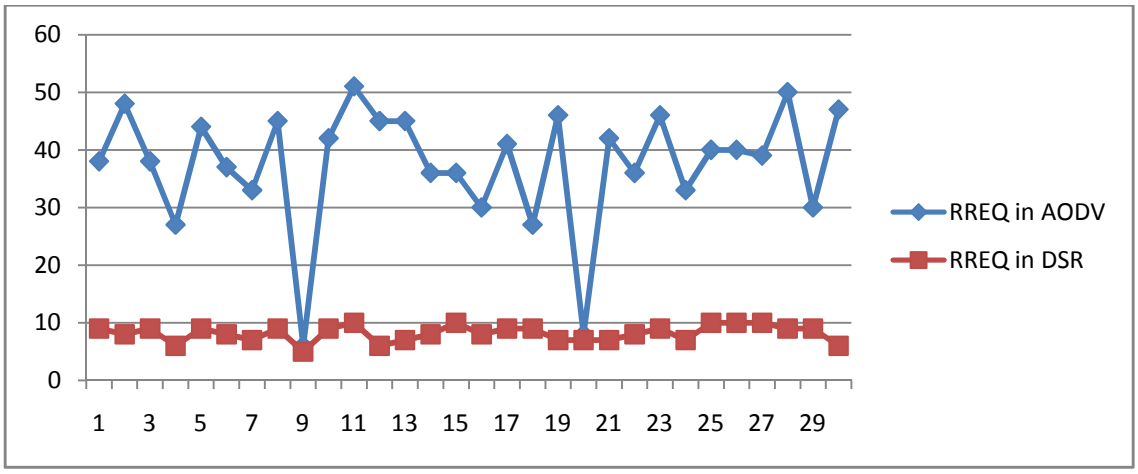


*Figure 3. Comparison of route request packets in AODV and DSR*

We have taken route request as the third comparison and is being shown in Figure 3. Comparing the route request made by AODV and DSR it is clear that DSR has less number of route request packets as compare to AODV, which made it less efficient in finding a new route and each time in replacing a stale link.

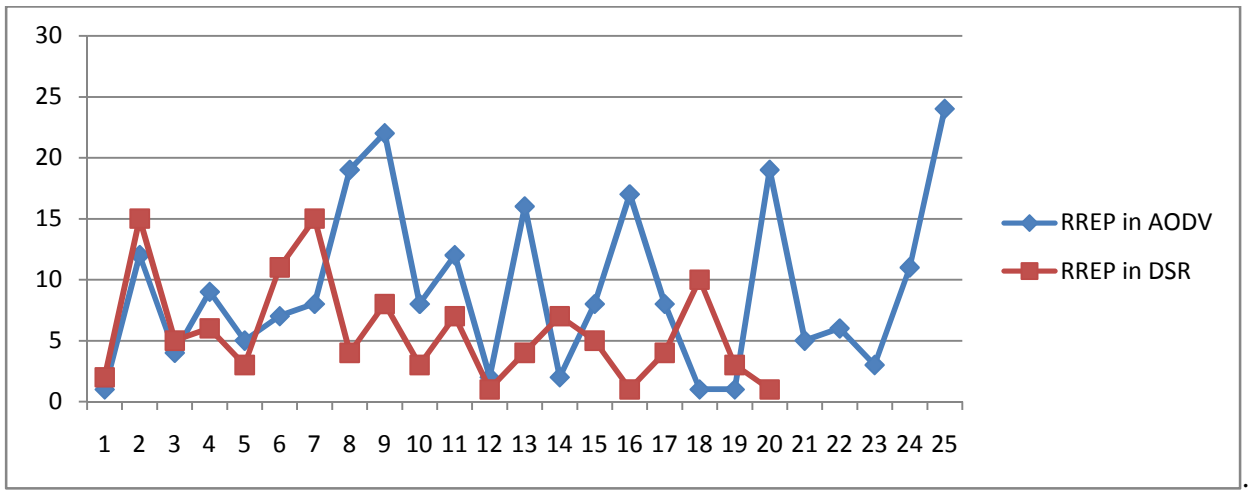


*Figure 4. Route Reply packets in AODV and DSR*

Figure 4 is the comparison of route reply packets made by AODV and DSR Here we see that AODV has more route reply options as compare to DSR; also DSR maintains multiple routes to the same destination in the cache. But unlike AODV, DSR has no mechanism to determine the freshness of the routes. It also does not have any mechanism to expire the stale routes. With high mobility, link breaks are frequent and there is the possibility of more routes becoming stale quickly. This requires the DSR to initiate the route discovery process which further adds to the increasing delay. From here also we can see that AODV is more efficient as compare to DSR.

# VI. CONCLUSION:

Our simulation results show that the performance characteristics of these two protocols with respect to route selection are better in case of AODV. Simulation results also indicate that DSR exhibits more intermediate nods in comparison to AODV. This is due to the fact that DSR being a source routing protocol, the initial path set up time is significantly higher as during the route discovery process every intermediate node needs to extract the information before forwarding the data packet. DSR has no mechanism to determine the freshness of the routes or to expire the stale [23] routes. With high mobility link breaks will be frequent and thus there is the possibility of more routes becoming stale quickly. Simulation results also indicate that AODV has more RREQ and RREP options which made it more efficient as compare to DSR. In our future work, we plan to study the performance of these protocols under other network scenarios by varying the network size, [26] the number of source nodes, the mobility models and the speed of the mobile nodes etc.

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# CROSS-LAYER BASED QOS ROUTING PROTOCOL ANALYSIS BASED ON NODES FOR 802.16 WIMAX NETWORKS

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## *ABSTRACT*

*A cross-layer framework to favor the video-on-demand service in multi-hop WiMax mesh networks. . This will guarantee that the required data rate is achieved for video streams, which is crucial for multimedia streaming applications. An efficient and light-weight multicast routing technique is also proposed to minimize the bandwidth cost of joining a multicast tree Cross-layer design for quality of service (QoS) in WiMax has attracted much research interest recently. The research on traditional cross- layered architecture which has served well for wired networks seems to be inefficient and not suitable for the wireless networks. Most of the cross-layer design proposals for wireless networks involve exchanging information between multiple layers or between just two layers. In this paper, we propose to develop a Cross-Layer Based QoS Routing (CLBQR) Protocol for 802.16 WiMAX Networks. In our protocol, the cross layer routing is based on the routing metrics which includes power, link quality and end-to-end delay. Then the routing is performed by estimating the combined cost value of these metrics. By simulation results, we show that our proposed protocol achieves higher packet delivery ratio with reduced energy consumption and delay.*

***KEYWORDS***: QOS, WiMax, CLBQR, AODV Protocol, EETT (Exclusive Expected Transmission Time)

# I. INTRODUCTION

## 1.1 WiMAX Networks

WiMAX (Worldwide Interoperability for Microwave Access) is a telecommunications protocol that provides fixed and fully mobile internet access. Wi-Fi, refers to interoperable implementations of the IEEE 802.11 and is similar to the WiMAX which refers to interoperable implementations of the IEEE 802.16 wireless-networks standard. The vendors can sell their equipments as WiMAX certified by using the WiMAX Forum certification. Hence it ensures a level of interoperability with other certified products, as long as they fit the sample profile [1].

For providing mobile broadband or home broadband connectivity, companies use WiMax across whole cities or countries. WiMAX network has relatively low cost when compared to the GSM, DSL, or Fiber-Optic. Due to this broadband connection can be provided in places where it is not economically possible. Cellular phone technologies such as GSM and CDMA are replaced by WiMAX or can be used as an overlay to increase capacity [1].

WiMAX is concerned as a disruptive wireless technology with many impending applications. With the QoS support it is probable for WiMAX to support business applications. WiMAX network can work in different modes point-to-multipoint (PMP) or Mesh mode, depending upon the applications and network investment [2]. The Cross Layer QOS frame work for IEEE 802.16 mesh mode as shown in Figure1.

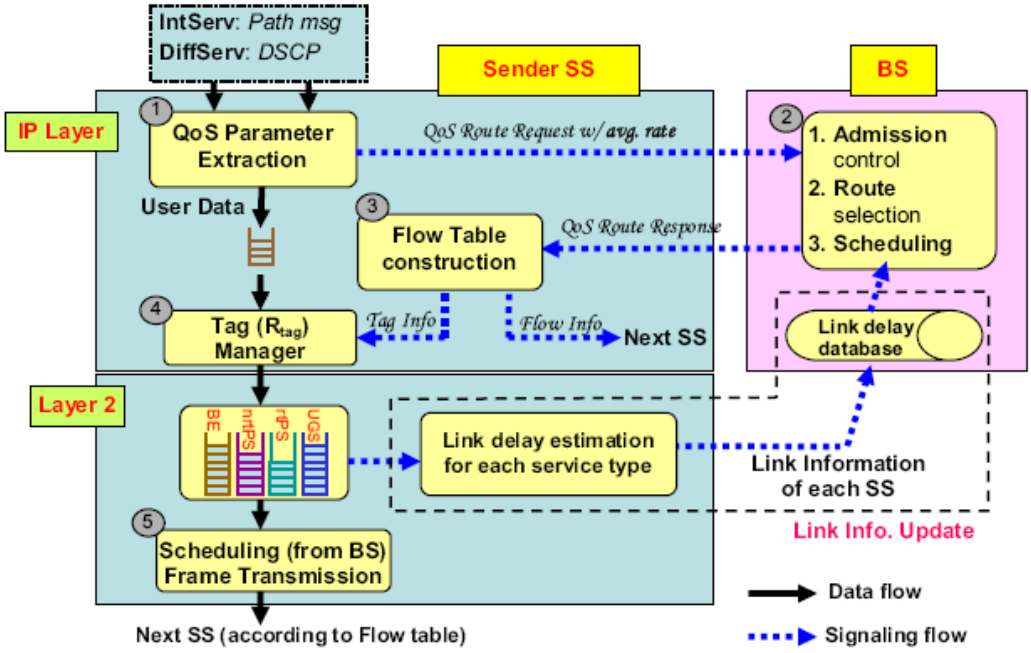


Figure 1. Cross Layer QOS Framework for IEEE 802.16 mesh mode

## 1.2 Routing types in WiMAX networks

There are two basic mechanisms for routing in the IEEE 802.16 mesh network

- Centralized routing
- Distributed routing

- **Centralized Routing**

In mesh mode concept, BS refers to the station that has directed connection to the backhaul services outside the Mesh Network and the remaining stations are termed as SSs. There are no downlink or uplink concepts within the Mesh Networks. However a Mesh network performs like PMP with a variation that all the SSs should not be connected directly with the BS. The resources are approved by the Mesh BS and this is considered as centralized routing [1].

- **Distributed Routing**

In distributed routing, with the help of its adjacent nodes each node receives some information about the network and it used to forward the traffic of each router. The BS is not defined appropriately in the network when using the distributed routing [1].

## 1.3 Routing Issues in WiMax Networks

The following are some of the routing issues in wimax networks:

- Routing in Wireless Mesh Network (WMN) is challenging because of the unpredictable variations of the wireless environment.
- Challenges for the routing in WiMax mesh includes delay, long transmission scheduling, and increasingly stringent Quality of Service (QoS) support and load balance and fairness limitations [3].
- The network topology in an 802.16 standard is a tree rooted at the base station and the problem is to determine the routing and link scheduling for the tree, either jointly or separately.
- Routing design has to address issues in both short and long time scales [3].
- WiMAX networks also face all the problems related to the hostile wireless environment, where power constraints make it difficult to provide hard QoS guarantees.

- While the Base Station can have continuous, unlimited power supply, other nodes usually have limited power supply and are battery-powered. It is inconvenient to replace them once they are deployed. Sometimes, replacement is even impossible. Thus, energy efficiency is a critical design consideration of WiMAX networks.
- Communication is a dominant source of energy consumption in WiMAX networks.
- Security is one of the main barriers and is crucial to wide-scale deployment of WiMAX networks, but has gained little attention so far. Once a node has been compromised, the security of the network degrades quickly if no measures are taken to deal with this event. Other security concerns may include the location privacy of a person, passive eavesdropping, denial-of-service (DoS) attacks, and so forth.
- Nodes energy cannot support long haul communication to reach a remote command site and hence they require multi-tier architecture to forward data. It is a fact that 70% of the energy is spent in data transmission [4].
- Wireless routing also has to ensure robustness against a wide spectrum of soft and hard failures, ranging from transient channel outages, links with intermediate loss rates, from several channel disconnections, nodes under denial-of-service (DOS) attacks, and failing nodes.
- A good wireless mesh routing algorithm has to ensure both long-term route stability and achieve short-term opportunistic performance

### 1.4 Cross Layer Routing

The joint optimization control of over two or more layers in a cross-layer paradigm provides considerably improved performance. Cross-layer design for quality of service (QoS) in wireless mesh networks (WMNs) has attracted much research interest recently. Various types of applications with different and multiple QoS and grade-of-service (GoS) requirements can be supported with these networks. Several key technologies spanning all layers, from physical up to network layer should be utilized for supporting the QoS and GoS. In addition to this, essential algorithms must be designed for harmonic and efficient layer interaction [5].
In our previous work [12], we have proposed a channel condition based rate allocation method which takes into account the channel error. It consists of two phases; Admission Control Phase and Rate Control Phase. In the first phase, the admission control is performed based on the estimated channel condition. In the second phase, we have developed a predictive rate control technique, using queue length and bandwidth requirement information.
Hence our objective is to design an efficient cross-layer based routing protocol for 802.16 WiMAX networks. In this paper, we develop a cross-layer based QoS outing protocol. In this protocol, using the physical and MAC layer, the minimum required power and link quality can be estimated and passed on to the routing layer. Then a combined cost value of the link quality and power along with delay can be determined and used in the routing protocol.

## II. RELATED WORKS

Chi Harold Liu et al [5], proposed Cross-Layer Design for QoS in Wireless Mesh Networks. They proposed a novel cross-layer framework that includes connection admission control together with QoS routing in the network layer and distributed opportunistic proportional fair scheduling in MAC layer. They defined a novel utility function that is exchanged between an efficient distributed opportunistic proportional fair scheduler and a multi-constrained QoS routing algorithm. Furthermore, a novel tightly-coupled design method for joint routing and admission control has been demonstrated, where a unified optimization criterion QoS performance index" that combines multiple QoS constraints to indicate the QoS experience of each route has been proposed.
Ali Al-Hemyari et al [6] proposed Cross Layer Design in 802.16d.The cross layer design discussed by them is dealing with the exchangeable information between MAC and NET layers to optimize the system performances. Two routing algorithms to find the scalable path to the BS for each node, and two CS algorithms for single and multi-channels single transceiver system have been proposed by

them. Some related issues pertaining to the system improvement are load balancing and fairness, slot reuse, concurrent transmission, and the relay models in the network also have been discussed. The system performances are further improved when a new design metric such as number of children per nodes is introduced.

Chun-Chuan Yang et al [7] proposed, Cross-Layer QoS Support in the IEEE 802.16 Mesh Network. Core mechanisms including mapping of IP QoS classes to 802.16 QoS types, admission control, minimal-delay-first route selection, tag-based fast routing, and delay-based scheduling were presented in the paper. This proposal can achieve the better performance in terms of delay, throughput, and signaling cost over the basic centralized and distributed scheduling scheme recommended in the standard.

Taimour Aldalgamouni et al [8], proposed a joint cross layer routing and resource allocation algorithm for multi-radio wireless mesh networks. The cooperation between the physical, MAC and network layers improved the performance of the network. The results showed that the proposed algorithm improved the average end to end delay and average end to end packet success rate compared to those of random routing and random resource allocation.

Fei Xie et al [9], proposed a cross-layer framework for video-on-demand service in multi-hop WiMax mesh networks. They aim at supporting true VoD service in residential or business networks with a WiMax based wireless backhaul. Their proposed routing algorithm makes use of the well-maintained scheduling tree and thus introduces less maintenance cost. The algorithm also minimizes the cost of joining a multicast tree. Based on the multicast routing algorithm, they applied the application layer patching technique which can offer true VoD service. They also extend the joint admission control and channel scheduling scheme to guarantee the data rate for Patching.

## III. Estimation of Routing Metrics

In this section, we briefly explain the routing metrics used in our cross layer based routing protocol. We use the following metrics:

- Power (P)
- Link Quality (LQ)
- End-to-End Delay (D)

### 3.1 Power

For utilizing the bandwidth efficiently, power control is very important. A Large number of hops are used in each route if the power allocated for each hop is minimum. Delay share of each hop can be decreased and thus it requires more time slots (bandwidth). On the other hand, in every route there are a minimum number of hops if maximum power is allocated. But the number of simultaneous transmissions is limited by the increase in the interference which leads to the inefficient wireless bandwidth utilization. In order to realize QoS provisioning with efficient resource allocation an optimal power allocation is required. *Pmin* is the minimum power required to transmit a signal on a link given the link distance and the sensibility of the receiver. *Pmax* is the maximum transmission power.

### 3.2 Link Quality

Links which are nearby with higher link quality can be allowed to transmit more packets, if links with poor quality is avoided by hopefully waiting for the link to improve. This probably improves the quality of the link. If the link behaves normally then the poor quality link could try to communicate.

We use the EETT (Exclusive Expected Transmission Time) metric to estimate the link quality [10].

EETT is a routing metric which is used to give a better evaluation of a multi-channel path. Consider a N-hop path with K channels. We have following definitions. For a given link l, its Interference Set (IS) is defined as the set of links that interference with it. A link's Interference Set also includes the link itself. Then the link l's EETT is defined as:

$$EETT_i = \sum_{link\, i \in IS(l)} ETT_i \quad \text{--- ---(1)}$$

where IS(l) is the Interference Set of link l.

### 3.3 End-to-End Delay

The delay associated with a network path is the sum of delays experienced by the links constituting the path and hence end-to-end delay is considered as an additive metric. The distance taken for a bit of data to travel across the network from one node to another is known as the delay and is usually calculated in multiples or fractions of seconds. Depending upon the location of the specific pair of communicating nodes, slight variations in the delay occurs. The maximum and average delay is necessary to perform exact measurements.

Each route *r* has a maximum end-to-end delay requirement to each of its packets. The end-to-end delay of a packet is the time it takes to travel from the source node to the destination node including intermediate links' transmission delays and nodes' queuing delays. Each link transmission delay equals the reciprocal of the link bandwidth (data transmission rate) which is constant. For the estimation of queuing delay, we use the average queuing delay at each node. Therefore the end-to-end delay D is given as,

$$D = \sum_{i=1}^{n} \frac{1}{LBW} + AQ_D \quad \text{--------} \quad (2)$$

where LBW is the link quality bandwidth and $AQ_D$ is the Average Queuing Delay.

## IV. CROSS LAYER BASED QOS ROUTING (CLBQR) PROTOCOL

### 4.1 AODV Protocol

Our cross layer based routing is a derivative of the well known AODV routing protocol. In this section, we briefly explain the working of the AODV protocol [11].

Ad-hoc On-demand distance vector (AODV) is a variant of classical distance vector routing algorithm. AODV uses a broadcast route discovery algorithm and then the unicast route reply massage. The following sections explain these mechanisms in more detail.

#### 4.1.1 Route Discovery

A route discovery process is initiated, when a node wants to send a packet to some destination node and does not locate a valid route in its routing table for that destination. Route request (RREQ) packet is broadcasted from source node to its neighbor, which then forwards the request to their neighbors and so on.

An expanding ring search technique is used by source node to control network-wide broadcasts of RREQ packets. By using time to live (TTL) value, the source node starts searching the destination in this technique. The TTL value will be incremented by an increment value if there is no reply within the discovery period. This process continues until threshold value is reached.

On forwarding the RREQ the intermediate node records the address of the neighbor from which first packet of the broadcast is received thus establishing a reverse path. The route reply (RREP) towards the source node is sent when the RREQ is received by a node that is either the destination node or an intermediate node with a fresh enough route to the destination. When the RREP is routed back along the reverse path, the intermediate nodes along this path set up a forward path entry to the destination in its routing table. A route from source to the destination established when the RREP reaches the source node.

#### 4.1.2 Route Maintenance

A route established between source and destination pair is maintained till it is required by the source. Route discovery is reinitiated to establish a new route to destination when the source node moves during an active session. When the destination node or the intermediate node moves, the routing entry is removed by the node upstream, and route error (RRER) message is sent to the affected active

upstream neighbors. To reach the source node, these nodes broadcast the RRER to their originator nodes and so on. By sending out a new RREQ message, the affected source node either stop sending data or reinitiate route discovery for that destination.

### 4.2 Combined Cost Value

In the cross layer based routing, we estimate a combined cost value of our routing metrics for routing. The combined cost (C) value is given as,

$$C = \frac{D}{P \times LQ} \quad \text{---- ---} \quad (3)$$

Where D is the end-to-end delay, P is the power and LQ is the link quality.
To compute *C,* a node conveys the information of the metrics in the RREQ packets along with the aggregate *C* value. Each node before forwarding a RREQ, first extracts this information. It then computes the new *C* value for each wireless interface operating channel. Finally, it updates the aggregate *C* and the information of the metrics in the RREQ packet.
All nodes maintain a minimum aggregate *C* (Cmin) value along with each routing entry in the routing table. An intermediate node sets the *C*min to the value received in the first RREQ. All subsequent copies of the RREQ are forwarded only if their aggregate *C* value is lower than the *C*min. If the value is lower, the current *C*min is replaced by the lower one. This ensures that the RREQ with the maximum channel diversity and least congestion is always forwarded and used for route creation.
In worst case scenarios, it is possible that multiple copies of the same RREQ with decreasing aggregate *C* values are received by a node. Thus we will have additional RREQs propagating in the network. However, the optimal RREQ with least aggregate *C* is generally received earlier than those with higher aggregate *C* values, since the optimal RREQ go across paths with maximum channel diversity and least loaded interface queues.

## V. SIMULATION RESULTS

### 5.1 Simulation Model and Parameters

To simulate the proposed scheme, network simulator (NS2) [13] is used. The proposed scheme has been implemented over IEEE 802.16 MAC protocol. In the simulation, clients (SS) and the base station (BS) are deployed in a 1000 meter x 1000 meter region for 100 seconds simulation time. All nodes have the same transmission range of 250 meters. In the simulation, CBR traffic is used.
The simulation settings and parameters are summarized in table 1.

Table 1: Simulation Settings

| | |
|---|---|
| Area Size | 1000 X 1000 |
| Mac | 802.16 |
| Nodes | 5,10,15,20 and 25 |
| No. of Flows | 1,2,3 and 4 |
| Radio Range | 250m |
| Simulation Time | 100 sec |
| Traffic Source | CBR |
| Physical Layer | OFDM |
| Packet Size | 1500 bytes |
| Frame Duration | 0.005 |

### 5.2 Performance Metrics

We compare our proposed CLBQR scheme with the CLQS scheme [7]. We mainly evaluate the performance according to the following metrics:
**Packet Delivery Ratio:** It is the ratio of the number of packets received successfully and the total number of packets sent.

**Energy Consumption:** It is the average energy consumption of all nodes in sending, receiving and forward operations

**Average end-to-end delay:** The end-to-end-delay is averaged over all surviving data packets from the sources to the destinations.

## 5.3 Results

### A. Based on Nodes

In our initial experiment, we vary the number of nodes as 5, 10, 15, 20 and 25.

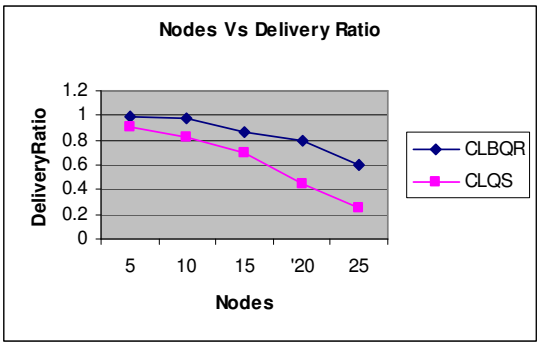


Fig: 2 Nodes Vs Delivery Ratio

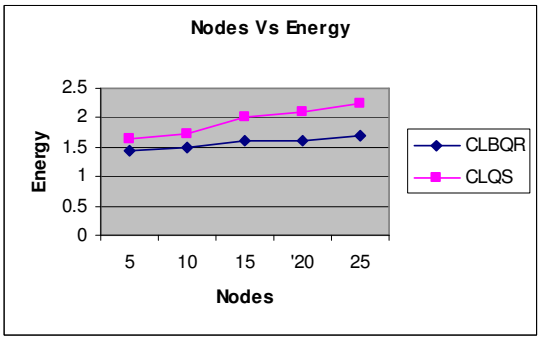


Fig: 3 Nodes Vs Energy

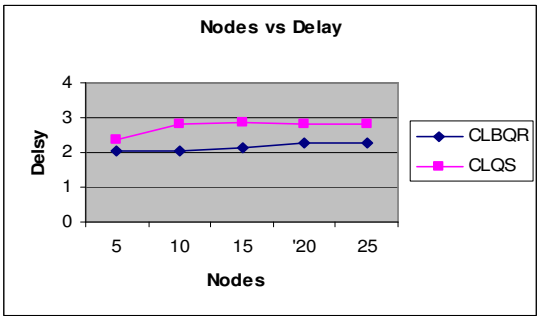


Fig: 4 Nodes Vs Delay

Figure 2 presents the packet delivery ratio when the number of nodes is increases. Since reliability is achieved using the dispersion technique, CLBQR achieves good delivery ratio, compared to CLQS. Figure 3 shows the results of energy consumption when the number of nodes is increased. From the results, we can see that CLBQR technique has less energy consumption when compared with CLQS. Figure 4 gives the average end-to-end delay when the number of nodes is increased. From the figure, it can be seen that the average end-to-end delay of the proposed CLBQR technique is less when compared with CLQS.

## VI. Conclusion

In this paper, we have developed a Cross-Layer Based QoS Routing (CLBQR) Protocol for 802.16 WiMAX Networks. In our protocol, the cross layer routing is based the routing metrics which includes power, link quality and end-to-end delay. In order to realize QoS provisioning with efficient resource allocation an optimal power allocation is required. We use the EETT (Exclusive Expected Transmission Time) metric to estimate the link quality where EETT is a routing metric which is used to give a better evaluation of a multi-channel path. The end-to-end delay of a packet is the time it takes to travel from the source node to the destination node including intermediate links' transmission delays and nodes' queuing delays. For the estimation of queuing delay, we use the average queuing delay at each node. Our protocol is the derivative of the AODV routing protocol which is the variant of classical distance vector routing algorithm. Then the routing is performed based on the routing metrics by estimating a combined cost value. By simulation results, we have shown that our proposed protocol achieves higher packet delivery ratio with reduced energy consumption and delay.

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# UNIT COSTS ESTIMATION IN SUGAR PLANT USING MULTIPLE REGRESSION LEAST SQUARES METHOD

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## *ABSTRACT*

*Co-generation is the concept of producing two forms of energy from one fuel. One of the forms of energy must always be heat and the other may be electricity or mechanical energy. In a co-generation plant a method for establishing unit costs of delivered steam and electrical energy is presented. This method employs the use of multiple regression least squares, based on a linear model of electrical energy generation and delivered steam as functions of generated boiler steam. The model is based on a plant design that allows steam to be extracted from between stages of the generating turbines at a reduced pressure to be used to serve heating loads. A discussion of the accuracy of the method is presented as well as an example of the use of the method using one year of Sonai sugar plant production.*

***KEYWORDS:*** *Cogeneration, multiple regression least squares methods, steam generation, steam turbines, surface fitting.*

## I. INTRODUCTION

Co-generation plants are extremely beneficial and cost effective for large institutions which require both heating and electrical power. This is particularly so when heating and electrical demands are well balanced and the demand for extracted steam and electrical power complement one another closely. The symbiotic nature of the simultaneous generation of steam and electricity carries with it the inherently elusive problem of assigning unit costs to each of the two types of utilities delivered.
In one way of thinking, the steam can be viewed as a by-product of electrical generation and therefore be considered essentially a "free" utility. Equally valid, or invalid, is the view that the electricity is just "skimmed off the top" of the steam delivery process, and is therefore of negligible cost. Whenever a plant has the optional capability of discharging steam from the turbines either at service pressure or at a vacuum, however, there is a definite unit value which can be assigned to both the electrical energy generated and the service steam delivered.
A mathematical model can be developed for cost as a function of both steam and electricity delivered, and the model can be fit to data from the boiler logs by the method of least squares. This provides a systematic method by which unit costs can be accurately calculated. The accurate calculation of unit costs for utilities generated from a plant are very important whenever consumption is metered and billed to differing accounts within an organization or between organizations. Multiple regression method of least square is used for calculating unit cost of steam in process and electricity. In this paper results obtained by this method are verified by analytical method of multiple regressions.

## II. SUGAR PLANT DESCRIPTION

The 16 MW capacity cogeneration project at M/s. Mula Sahakari Sakhar Karkhana Ltd (MSSKL) will integrate existing sugar mill operations with enhanced energy efficiency measures and optimum usage of bagasse. During season, generated mill bagasse will be transferred to the cogeneration plant which is to be installed in the campus of existing plant located at Sonai village in (M. S.) India. The

cogeneration plant will supply the heat and power requirements of the sugar mill and evacuate excess power to the state owned grid. During off-season, the power plant will use saved and procured bagasse from nearby mills for power generation. Technical detail of plant is as follows,

Plant Capacity = 17 MW
Voltage Generated = 11 K.V.
Boiler capacity = 80 tonne per hour.
Working pressure = 67 kg/cm2
Boiler temperature = 490 C
Type of boiler = water tube
Fuel = bagasse.

Power is stepped down to 433 V for supplying to sugar mill and cogeneration auxiliaries. Where as for export to the grid, it is stepped up to 132 KV. In normal mode, the STG operates in synchronisation with the Distribution Company (M.S.E.D.C.L.) grid. In event of any undesirable disturbance in the grid, the plant will island from the grid & continue supplying home load [1].

For Case study of Sonai plant in season 2007-2008 data has been taken into an account as shown in Table 1 Sonai plant delivers steam for heating, humidification, and absorption cooling of the facilities on the campus. The plant consists of one boiler/turbine units each capable of providing 67 kg exhaust steam to the campus steam distribution system. The capacity of unit is 17 M.W. Unit is capable of exhausting steam at the 67 kg /cm2extraction pressure only. In an ideally balanced situation, the amount of steam sent to the condensers is an absolute minimum and virtually all of the exhaust steam is sent to the campus heating distribution system. This type of an operating mode is the exception rather than the rule, however, as the steam and electrical loads are determined by campus demand .There exists a tradeoffs in determining the unit cost of each utility in that sending exhaust steam to the condensers, so as to generate more electricity, means forfeiting the value of the extraction steam which could have been sent to the campus distribution system. Likewise, the dispensation of steam to the campus distribution system means forfeiting electrical energy which could have been generated, had that steam been sent through the remaining stages of the turbine and been exhausted at a vacuum. The key in assigning the proper unit costs to these two utilities lies in equating their production to the common denominator of steam generated by the boilers, which we refer to as boiler steam [2].

**Table1 Plant output of Season 2007-08 (07 month)**

| Month | Delivered Steam(Sd) MT | Electrical Energy(E) KWH | Boiler Steam(Sb) MT |
|---|---|---|---|
| Nov.07 | 18924 | 4689267 | 28721 |
| Dec07 | 18012 | 4693324 | 28812 |
| Jan08 | 18253 | 4678132 | 28184 |
| Feb08 | 17528 | 4598764 | 29602 |
| Mar08 | 17382 | 4593925 | 27742 |
| Apr08 | 17154 | 4485606 | 27134 |
| May08 | 17103 | 3357982 | 27036 |
| **Total** | $\sum S_d$ **=124356** | $\sum E$ **= 1097000** | $\sum S_b$ **=197231** |

All steam generated in the plant is eventually condensed and returned to the boilers as feed water. This excludes leakage, of course, and a very small amount of steam used for such non conservative loads as humidifiers and autoclaves. Makeup water must be provided for these losses, as in any plant. Table1 shows the monthly values of steam delivered to the campus as well as the overall production of boiler steam. The value given for boiler steam includes the steam used in the production of electricity that is condensed at a vacuum, as well as the steam discharged at 67 kg/cm2 and sent to the campus distribution system. For example, during the first month of November 2007 shown in Table I,

28721 MT of boiler steam was generated and 18924 MT of that steam was extracted from the steam turbines and delivered to the campus at 67 kg/cm2 for heating purposes. The remainder was condensed at a vacuum, used exclusively in the electrical generation process. On an annual averaged basis, approximately 53% of boiler steam is extracted from the turbines at 67 kg/cm2 and sent to the campus distribution system. This leaves 47% which is used in the conventional generation of electricity only.

As can be seen from the percentages given above, the demand associated with the Sonai Plant is heavily weighted toward the electrical side of the spectrum. Occasionally, additional electrical power must be purchased from Consumer's Energy, the local utility, to meet peak electrical demand. This is particularly true when boilers may be out of service for maintenance. At no time is additional steam required to be purchased or generated to meet steam demand beyond that which is available by extraction from the electrical generation process. Steam demand is therefore handled automatically by making extraction steam available to the main distribution header at a constant pressure of 67 kg/cm2 and sending the remainder of the steam through the low pressure stages of the turbines to be used in electrical generation. Other sources of condensate are not measured, including that which condenses on the distribution lines and is periodically removed by traps placed at regular intervals along the distribution piping. The rate of heat loss, or condensate generation, therefore, is not measured or calculated for the system. This topic, however, could possibly be examined in another study, using various heat loss estimation techniques and possibly even some representative measurements taken in sample locations.

# III. UNIT COST ESTIMATION IN SONAI SUGAR PLANT

## 3.1 Modelling the plant output

In order to establish unit costs for the electrical and steam utilities, a mathematical model must be developed which accounts for the fuel consumed in terms of the utilities delivered .We know that there is a certain cost associated with operating the plant even if no utilities are generated whatsoever. The cost of salaries for the staff to operate and maintain the plant, the cost of service contracts for specialized maintenance, and any amortization costs associated with the original construction of the plant are incurred by the Plant administration whether or not the plant is even on line. These can all be lumped into a category considered as "fixed costs." The cost of the fuel for the plant is the largest single cost associated with plant operation, and a certain amount of this cost can also be attributed to the fixed cost category. A certain amount of fuel is consumed and "lost" in terms of heat losses from piping and equipment, power for lighting the plant, etc .These costs can be lumped into the fixed cost category since they also are incurred regardless of the level of plant output. Even though the fixed costs cannot be easily converted to unit costs for electrical and steam energy delivered, it is desirable to recoup these costs by charging customers unit costs for the utilities received. These costs can be easily absorbed in a unit cost for boiler steam generated and then attributed to electrical and steam unit costs from there. The overall boiler steam unit cost can be calculated by the sum of the overall plant costs per year divided by the total number of MT of boiler steam generated [3].

$$C_{bs} = \frac{A_{main} + A_{op} + A_{fuel} + .... + A_{cont}}{S_a} \quad (1)$$

Where,

$C_{bs}$ = Unit cost of boiler steam (Rs./Ton).

$A_{main}$ = Annual cost of plant maintenance staff

$A_{op}$ = Annual cost of plant operating staff.

$A_{fuel}$ = Annual cost of fuel consumed by the plant.

$A_{cont}$ = Annual cost of contracted supplies and services

$S_a$ = Annual amount of boiler steam generated (ton)

With a unit cost for boiler steam obtained, the unit costs of delivered steam and delivered electrical energy can then be calculated. In order to do this, the amount of boiler steam attributable to each of the two delivered utilities must be calculated. The mathematical model for making this conversion is as follows;

$$S_b = I + X_s S_d + X_e E \quad (2)$$

Where,

$S_b$ = boiler steam required (Ton),

$I$ = internal steam usage (Ton),

$X_s$ = delivered steam ratio (Ton boiler steam per Ton delivered steam).

$S_d$ = delivered steam (Ton).

$X_e$ = electrical steam ratio (Ton boiler steam per KWH delivered electricity).

$E$ = delivered electricity in KWH.

The known factors in this equation are $S_b$, $S_d$, and $E$. These are all obtainable from the monthly boiler logs. The time intervals typically used for this equation are of one month duration, since this provides a diverse range of operating conditions to average out any errors or anomalies in the records. These type of irregularities tend to have a more imbalanced effect when measured over shorter periods. Regardless of the time period used, it is important to be consistent in using the same time period for each term in the equation. The reason for this is that the parameter, internal steam usage, varies depending on the time period used; the others do not.

### 3.2 Multiple regression least square method.

Multiple regression estimates the outcomes (dependent variables) which may be affected by more than one control parameter (independent variables) or there may be more than one control parameter being changed at the same time. An example is the two independent variables x and y and one dependent variable z in the linear relationship case [4, 5].

$$z = a + bx + cy$$

For a given data set $(x_1, y_1, z_1),,(x_2, y_2, z_2),(x_n, y_n, z_n)$

Where $n \geq 3$, the best fitting curve f(x) has the least square error, i.e.,

$$z = \sum_{i=1}^{n} [z_i - f(x_i, y_i)]^2 = \sum_{i=1}^{n} [z_i - (a + bx_i + cy_i)]^2 = \min \quad (3)$$

Please note that $a$, $b$ and $c$ are unknown coefficients while all $x_i$, $y_i$, and $z_i$ are given. To obtain the least square error, the unknown co-efficient $a$, $b$ and $c$ must yield zero first derivatives.

$$\frac{\partial \prod}{\partial a} = 2\sum_{i=1}^{n} [z_i - (a + bx_i + cy_i)] = 0$$

$$\frac{\partial \prod}{\partial b} = 2\sum_{i=1}^{n} x_i [z_i - (a + bx_i + cy_i)] = 0 \quad (4)$$

$$\frac{\partial \prod}{\partial c} = 2\sum_{i=1}^{n} y_i [z_i - (a + bx_i + cy_i)] = 0$$

Expanding the above equations (4), we have

$$\sum_{i=1}^{n} z_i = a\sum_{i=1}^{n} 1 + b\sum_{i=1}^{n} x_i + c\sum_{i=1}^{n} y_i$$
$$\sum_{i=1}^{n} x_i z_i = a\sum_{i=1}^{n} x_i + b\sum_{i=1}^{n} x_i^2 + c\sum_{i=1}^{n} x_i y_i \quad (5)$$
$$\sum_{i=1}^{n} y_i z_i = a\sum_{i=1}^{n} y_i + b\sum_{i=1}^{n} x_i y_i + c\sum_{i=1}^{n} y_i^2$$

The unknown coefficients $a$, $b$ and $c$ can hence be obtained by solving the above linear equations.

### 3.3 Multiple regression method used for calculation.

Use of least square multiple regression method using equation 1

Equations are as follows,

$$\sum Sb = n\,I + X_s \sum S_d + X_e \sum E \quad (6a)$$

$$\sum S_d.S_b = I \sum S_d + X_s \sum S_d^2 + X_e \sum S_d.E \quad (6b)$$

$$\sum E.S_b = I \sum E + X_s \sum S_d.E + X_e \sum E^2 \quad (6c)$$

Where, n is number of months

**Table 2 Calculation Chart**

| $S_d.S_b$ | $S_d^2$ | $S_d.E$ | $E.S_b$ | $E^2$ |
|---|---|---|---|---|
| 543516204 | 358117776 | $8.87*10^{10}$ | $1.34*10^{11}$ | $2.19*10^{13}$ |
| 518961744 | 324432144 | $8.45*10^{10}$ | $1.35*10^{11}$ | $2.20*10^{13}$ |
| 514442552 | 333172009 | $8.53*10^{10}$ | $1.31*10^{11}$ | $2.18*10^{13}$ |
| 518863856 | 307230784 | $8.06*10^{10}$ | $1.36*10^{11}$ | $2.11*10^{13}$ |
| 482211444 | 302133924 | $7.98*10^{10}$ | $1.27*10^{11}$ | $2.11*10^{13}$ |
| 465456636 | 294259716 | $7.69*10^{10}$ | $1.21*10^{11}$ | $2.01*10^{13}$ |
| 462396708 | 292512609 | $5.74*10^{10}$ | $9.07*10^{11}$ | $1.12*10^{13}$ |
| **∑3505849144** | **∑2211858962** | **$\sum 5.71*10^{11}$** | **$\sum 9.04*10^{11}$** | **$\sum 1.47*10^{14}$** |

## IV. RESULT AND DISCUSSION

Employing the least squares method on the sample data given in Table 2, the resulting parameters areas follows,

$97231 = 7\,I + X_s\,124356 + X_e\,31097000$

$3505849144 = I\,124356 + X_s\,2211858962 + X_e\,5.71*10^{11}$

$9.04*10^{11} = I\,31097000 + X_s\,5.71*10^{11} + X_e\,1.47*10^{14}$

By using the values of above chart in multiple regression equations we get

$I$ =16985.84213

$X_s$ =0.415518312

$X_e$ =8.572502*$10^{-4}$

### 4.1 Calculation of unit costs estimation for steam and electrical demand

By using equation 1 we can calculate unit cost of steam and unit cost of electricity separately as follows

Unit Cost of Steam = $C_{bs} * X_s$

Unit Cost of Electricity = $C_{bs} * X_e$

$A_{fuel} = 93*10^7$ $A_{main} = 36*10^5$

$A_{op} = 72*10^5$ $A_{cont} = 132*10^5$

$A_{sta} = 10*10^5$ $A_{extr} = 20*10^5$

$A_{elect} = 12*10^5$ $A_{total} = 95.82*10^5$

Where,

$A_{sta}$ is count for stationary expenses of plant

$A_{elect}$ is count for electricity utilised by plant

$A_{extr}$ is cost for extra work other than above

$A_{total}$ is total cost of plant

$C_{bs} = A_{total} / S_a$

=95.82*107/197231

=4858.262646

**Unit Cost of Steam** = $C_{bs} * X_s$ = (4858.262646)*(0.428896036)

=2083.689591 Rs/Tonne

= $C_{bs} * X_s$ = 2.083 Rs/Kg

Now,

**Unit Cost of Electricity** = $C_{bs} * X_e$

= (4858.262646)*(8.23704271*10-4*103) = 4001.77 Rs/Wh

= 4.001 Rs/Kwh

### 4.2. Calculation of percentage relative error

Using values of $I$, $X_s$ and $X_e$ constants in equation 2 we can find percentage error monthly between calculated boiler steam production and actual boiler steam production using following formula.

$$\% \text{ error } = \{\frac{[s_b(measured) - s_b(calculated)]}{s_b(measured)}\} * 100$$

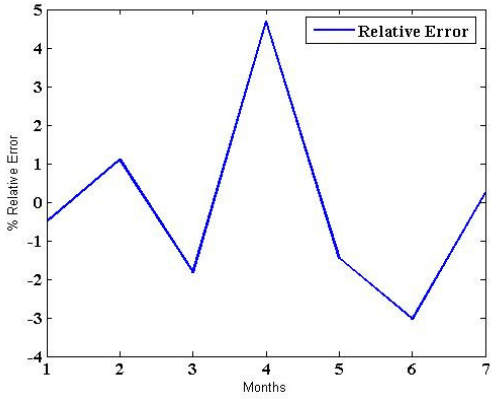


**Figure1. Represents % error month wise**

Figure1 shows the "residuals" from one year's (07 month) worth of data. This is the percent difference between measured boiler steam and calculated boiler steam, month by month. The errors appear to be well balanced on both sides of the axis with no characteristic signature, suggesting a good lit of the mathematical model. The standard deviation of these errors is 1.87% which is very good considering the numbers of variables which come in to power plant operation. By comparison, a trial and error procedure was used by University prior to the utilization the method of Least squares. The standard deviation of errors using this method was 4.69%. The method of least squares clearly provides more accurate solutions for the parameters which allow the mathematical model to more closely conform to the physical measurement.

## V. CONCLUSION

In Cogeneration plant there is simultaneous production of heat and electricity whatever steam is produced in boiler is used for sugar process and electricity generation. That means steam generated in boiler is a linear function of steam used in sugar process and for electricity. Multiple regression method of least square is used to calculate the unit cost of steam used in sugar process and electricity. Without a systematic method for evaluating the unit costs of steam and electricity delivered from a co-generation power plant, there figures can be very difficult to obtain.

When a mathematical model is developed and fitted to a data taken from boiler logs, the unit cost of each utility can be accurately computed. The method of least squares allows the errors to be minimized between calculated and measured boiler steam delivery rates. The accuracy of this comparison gives assurance that the model is appropriate and that the unit costs have been arrived at correctly. The accurate unit cost of steam delivered and unit cost of electricity calculation becomes very simple by use of multiple regression method.

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# ARTIFICIAL NEURAL NETWORK AND NUMERICAL ANALYSIS OF THE HEAT REGENERATIVE CYCLE IN POROUS MEDIUM ENGINE

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## *ABSTRACT*

*Homogeneous Charge Compression Ignition (HCCI) Engines offers lot of advantages over the conventional Internal Combustion Engines. The disadvantages of HCCI such as high HC and CO emissions can be reduced significantly by applying the concept of porous medium combustion. Porous Medium (PM) Engines are the revolutionary concept that is proposed to overcome the disadvantages of HCCI Engines. In this paper numerical analysis of Thermodynamic model of heat regenerative cycle of PM Engine is performed and the effect of various parameters like expansion ratio, initial temperature and maximum temperature are analyzed in efficiency. Artificial Neural Network (ANN) is used topredict the performance of PM Engine and the results are compared with the corresponding values of outputs obtained by Numerical analysis.*

***KEYWORDS:*** *HCCI Engine, Porous Medium Engine,Heat regenerative cycle, Artificial Neural Network.*

## I. INTRODUCTION

Research in the field of internal combustion (IC) engines has been motivated by the desire to preserve a clean environment and to reduce energy consumption. Reducing exhaust emissions of internal combustion engines are of global importance. Presently,homogenous charge compression ignition (HCCI) engines are being actively investigated worldwide as they can achieve efficiencies close to that of diesel engines while producing low levels of oxides of nitrogen (NOx) and particulate matter emissions. But the disadvantages associated withHCCI Engines are higher hydrocarbon (HC) and carbon-monoxide(CO) emissions[1], the control of ignition timing and combustionrate over the complete operating range. Porous medium (PM) engine, basedon the regenerative or super-adiabatic combustion in porous medium, can reduce the HC and CO emissions to a larger extent[2].Recently, the PM engine has received more and more attention fromnumerousresearchers because of its potential for producing homogeneous mixtures and reducing NOx and soot emissions [3,4].

Premixed combustion within porous mediahas been studied widely and applied to steady combustionwith great successes over the past decades [5,6,7].Consequently,the technique has been then extended from gaseous to liquid fuelsand from steady to unsteady combustion.On this basis, the new concept ofcontrollable combustion in porous media for internal combustionengine was suggested and developed. Durst and Weclas[8] proposed two designs of the PM engine, in one of which a porous mediumcombustion chamber is mounted in the engine cylinder head,fuel is injected into the porous medium chamber, and consequently, all combustion events, i.e. fuel vaporization, fuel–air mixture formation and homogenization, internal heatrecuperation,aswellascombustionreaction occur inside the porous medium. In orderto prove the feasibility of PM engine, they modified a single-cylinder,air cooled diesel engine to incorporate a porous medium reactorin the cylinder head and operated it as a PM engine.

Hanamura[9] designed a reciprocating heat engine, which is similar to a Stir ling engine with super-adiabatic combustion in porousmedia. One-dimensional numerical simulations shows that thethermal efficiency of the engine reached to 57.5% under even verylow compression ratios between 2 and 3, which are much lowerthan those of conventional Otto and Diesel cycles. Weclas[10] proposed a strategy for development of intelligent combustion systems for IC engines, whose essenceis a new concept for mixture formation andhomogeneouscombustionbased on the Porous Medium technology. Macek[11] analyzed the possibilities of homogeneous combustionachieved by porous medium with limited temperature, and foundthermodynamic limits of a new cycle with PM combustion usinghigh flame stability and fast burning at comparatively low temperaturesand the potential of internal heat regeneration. Here we have analyzed the PM heat regenerativecycle in a PM engine and evaluate its thermodynamic performance numerically as well as using ANN. This work is basically the extension of the work done by Hongsheng Liu[3].The engine is derived from one of the designs of Durst[8] and the analysis is based on general idealized cycle model.An ideal thermodynamic model for the cycle of PM engine is presentedto evaluate effects of various working parameters on theperformance of the PM engine.The PM engine is here defined as an internal combustion enginewith a highly porous medium chamber mounted on the cylinderhead (Fig. 1). The PM chamber is thermally isolated from the headwalls and equipped with a valve permitting a periodic contact betweenthe PM-chamber and the cylinder volume.Fig.1shows the complete working cycle of the PM engine advancedby Durst [8].

## II. POROUS MEDIUM ENGINE CYCLE

To conduct an ideal cycle analysis of the PM engine, three essential assumptions were adopted in this study:
(1) The heat capacity of porous medium is much larger than that of gas, thus the temperature of porous medium can be regarded as constant and not affected by the heat exchange between the porous medium and the working gas.
(2) Heat losses via the piston, cylinder wall and PM-chamber are neglected. The compression and expansion processes realized were considered as adiabatic.
(3) Instantaneous thermal coupling between the PM-chamber volume and the cylinder. This means that no time elapses during heat transfer between porous medium and the working gas.
Under these assumptions, an idealized thermodynamic cycle with PM heat regeneration in the PM engine can be described with Fig. 2.

The heat added per unit mass of working fluid for the PM heat regenerative cycle is

$$Q_{in} = Q_{2-3} + Q_{3-3'} = C_v(T_3 - T_2) + RT_3 \ln\left(\frac{v_3'}{v_3}\right)$$

Net Work output per cycle is

$$\begin{aligned} W &= W_{2-3} + W_{3-3'} + W_{4-1} \\ &= C_v(T_3 - T_2) + RT_3 \ln(V_{3'}/V_3) + C_v(T_1 - T_4) \end{aligned}$$

The cycle efficiency for the PM heat regenerative cycle 1–2–3–3’–4–1 is

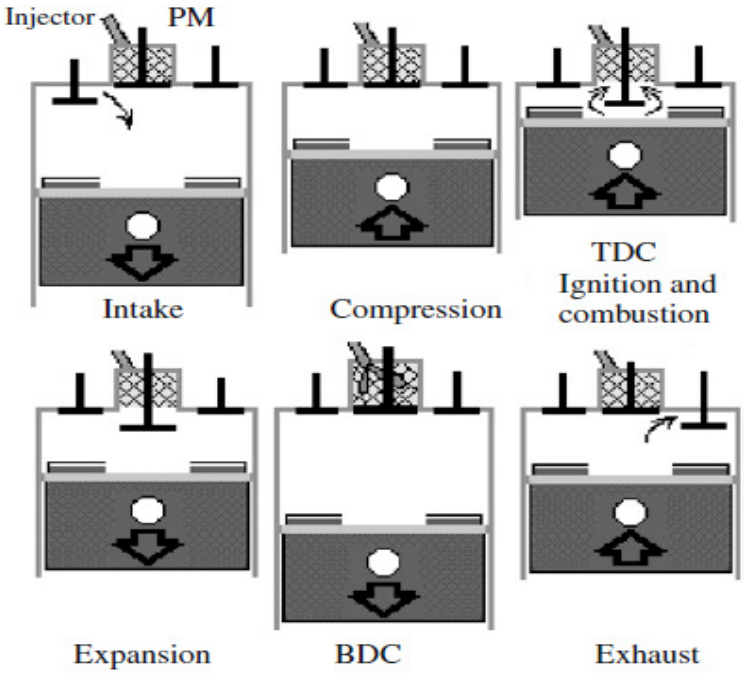


Fig.1.Principle of the PM engine proposed by Durst [8].

$$\eta = 1 - \frac{T_3(\rho/\varepsilon)^{k-1} - T_1}{T_3 - T_1\varepsilon^{k-1} + (k-1)T_3 \ln \rho}$$

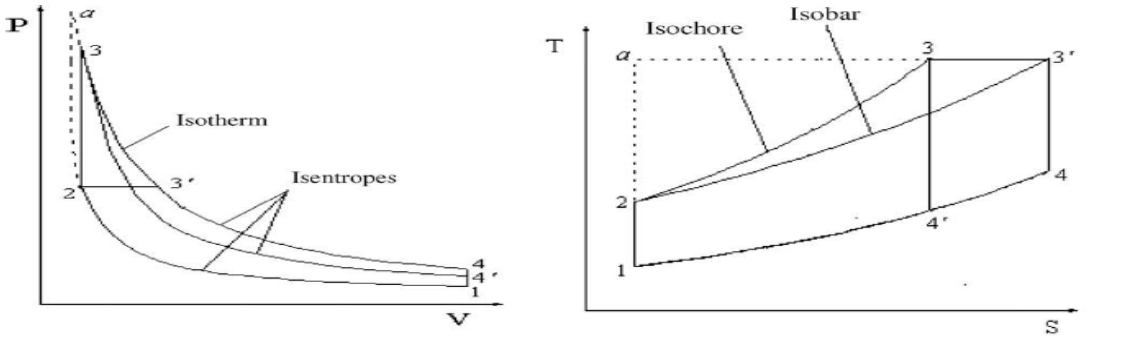


Fig.2.Comparison of Otto, Diesel and PM heat regeneration cycle[3].

## III. NUMERICAL RESULTS

A parametric study was conducted to analyze effects of ρ, T1 and T3on the characteristics of the net-work output versus efficiency forPM heat regenerative cycle with ideal thermodynamic model.Range of the various parameters is shown in Table 1. Results of the calculationsfor above parameters ranges are shown in the Fig.3 and Fig.4.

**Table1. Range of various parameters**

| Parameters | Range |
|---|---|
| Initial Temperature,T1 | 300K to 350K |
| Expansion Ratio, ρ | 1 to 2.5 |
| Maximum Temperature, T3 | 1600K to 2000K |
| Ratio of Specific Heats, k | 1.4 |
| Constant volume Specific Heat, Cv | 0.7165 KJ/Kg.K |

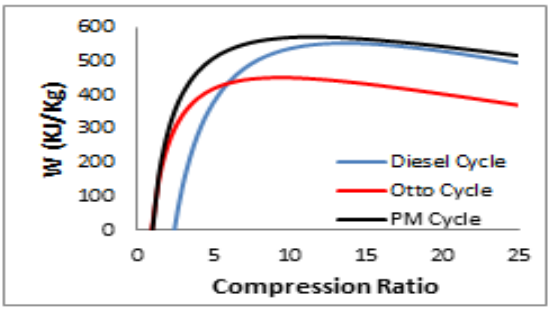


Fig.3. Comparison of the Net Work output for Otto, Diesel and PM heat regeneration cycle.

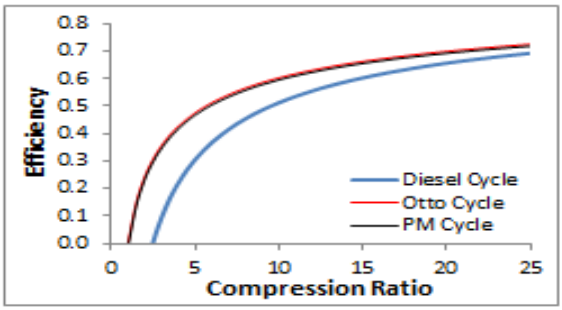


Fig.4. Comparison of efficiency for Otto, Diesel and PM heat regeneration cycle.

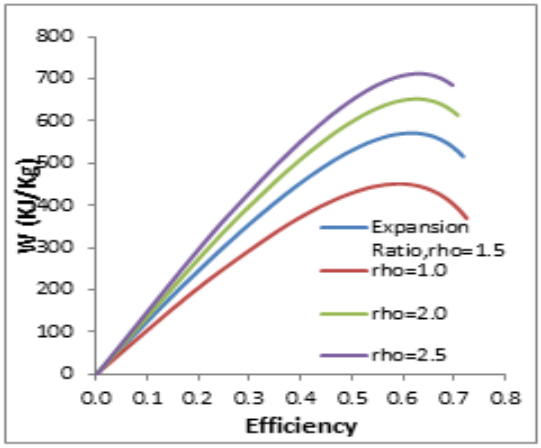


Fig.5. Influence of ρ on the Net Work output versus Efficiency characteristic

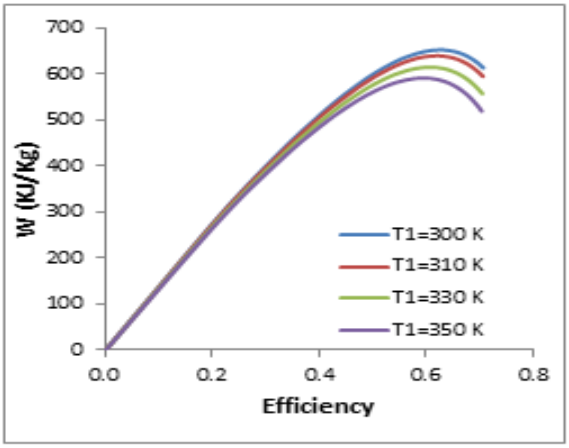


Fig.6. Influence of T1 on the Net Work output versus Efficiency characteristic

For an actual engine, the compression ratio must exceeds certainvalue to ensure the realization of the actual cycle, therefore, the net-work output of the PM heat regenerative cycle must be largerthan that of actual Otto and Diesel cycle. That means the PM heat regeneration cycle can provide significantly more net-work outputat little expense of thermal efficiency.

Fig. 5shows the influences of the expansion ratio (ρ) on the net-work output versus the efficiency for the PM heat regenerative cycleat a condition of T1 = 300 K and T3 = 1800 K. It is shown that there exists a maximum net-work output for constant expansionratio, with the increase of the expansion ratio, the maximum net-work output increases greatly and the thermal efficiency corresponding to the maximum net-work output increases also. Whenthe expansion ratio equals 1 the cycle becomes an Otto cycle, whose net-work curve is much lower than others.

Fig. 6 shows the effects of the initial temperature T1 on the network output versus the thermal efficiency for the PM heat regenerative cycle at a condition of ρ = 2.0 and T3 = 1800 K. The maximum net-work output decrease with the increase of the initial temperature, however, the change is not very evident.
Fig. 7 shows the effects of the maximum temperature T3 on the net-work output versus the thermal efficiency for the PM heat regenerative cycle at a condition of ρ = 2.0 and T1 = 300 K. It shows that there exists a maximum net-work output for constant maximum temperature.With the increase of the maximum temperature, the maximum net-work output increases evidently and the thermal efficiency corresponding to the maximum net-work output also increases.
These results are in good agreement with the results obtained by Hongsheng Liu, MaozhaoXie, Dan Wu [3] as shown in Fig.8 and Fig.9.

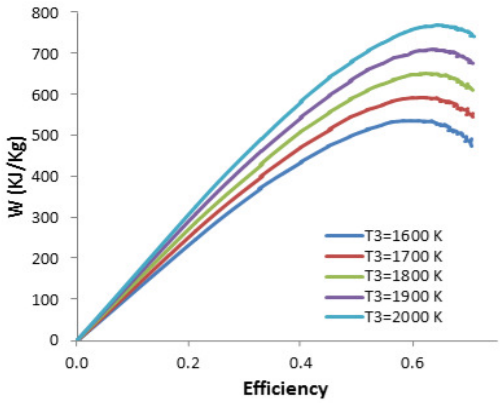


Fig.7. Influence of T3 on the Net Work output versus Efficiency characteristic

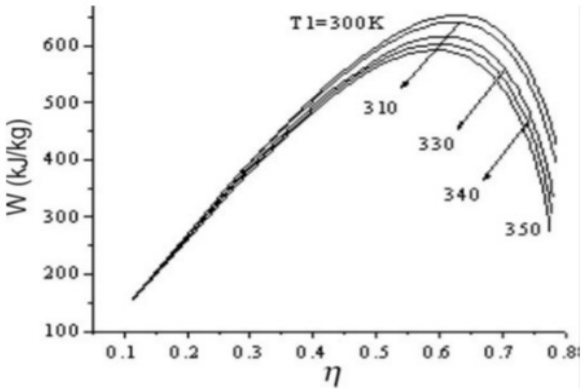


Fig.8. Influence of T1 on the Net Work output versus efficiency Characteristic (Hongsheng Liu, MaozhaoXie, Dan Wu)

## IV. ANN ANALYSIS

An artificial neural network (ANN) is an information processing paradigm that is inspired by the way biological nervous system.In a simplified mathematical model of the neuron, the effects of synapses are represented by connection weights that modulate the effect of the associated input signals, and nonlinear characteristics exhibited by neurons is represented by a transfer function. The neuron impulse is then computed as the weighted sum of the input signals, transformed by the transfer function. The learning capability of an artificial neuron is achieved by adjusting the weights in accordance to the chosen learning algorithm.
A typical artificial neuron and the modeling of a single layered neural network is shown below. The signal flow from inputs $x_1$ , ... ... ... $x_n$ is considered to be unidirectional, which are indicated by arrows, as is aneuron's output signal flow (O). The neuron output signal O isgiven by the following relationship:

$$O = f(net) = f \sum_{j=1}^{n} w\, x_j$$

Where, $x_j$the weight vector and the function f (net) is referred to as an activation (transfer) function. The variable net is defined as a scalar product of the weight and input vectors,

$$net = w^T x = w_1 x_1 + \cdots + w_n x_n$$

Where, T is the transpose of a matrix and in the simplest case, the output value O is computed as

$$O = f\,(net) = \{1\ if\ w^T \geq \theta\ and\ 0\ otherwise\}$$

Where, θ is called the threshold level and this type of node is called a linear threshold unit.

The ANN approach has been applied to predict the performance of various thermal systems. The useofANNsfor modeling theoperationofinternalcombustion engines is a more recent progress. This approach was used to predict the performance and exhaust emissions of diesel engines [12]and the specific fuel consumption and fuel air equivalence ratio of a diesel engine [13]. The effects of valve-timing in a spark ignition engine on the engine performance and fuel economy was also investigated using ANNs [14].

The output of the network is compared with desired output at each presentation and errors were computed. These errors were then back propagated to the ANN for adjusting the weight such that the errors decrease with each iteration and ANN model approximated the desired output. The network is trained till the chosen error goal of $10^{-6}$ is achieved. The schematic of a feed forward network is shown in Fig.10.

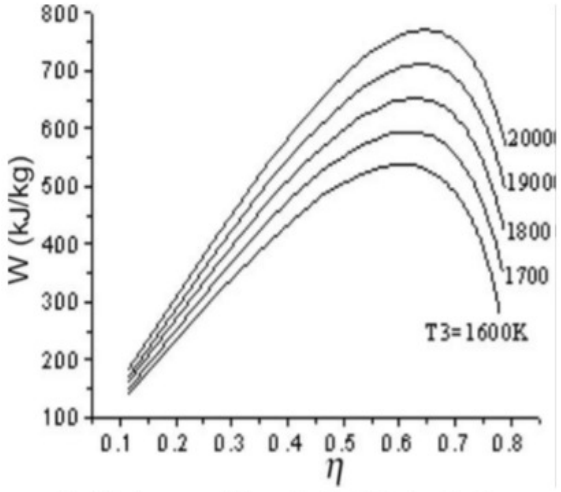


Fig.9. Influence of T3 on the Net Work output versus efficiency characteristic.(Hongsheng Liu, MaozhaoXie, Dan Wu)

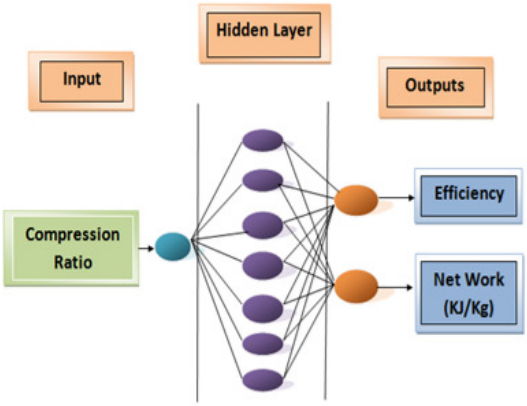


Fig.10. Representation of feed forward network for single hidden layer

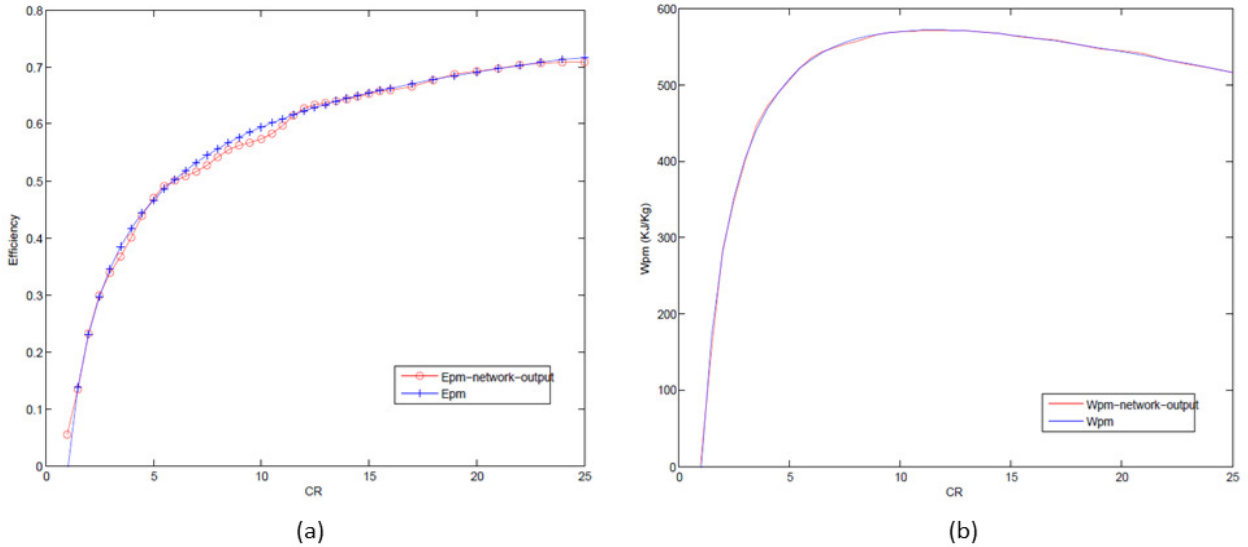


Fig.11. Comparison of ANN predicted results with numerical results

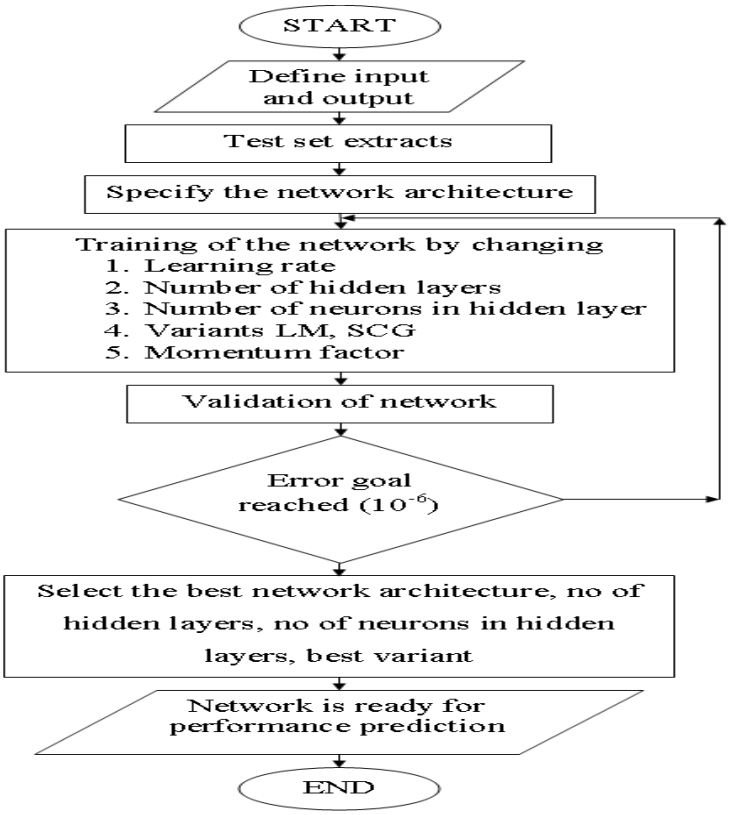


Fig.12. Flow chart of the ANN used for performance prediction.

In the present study, back propagation algorithm with variant LM is used. Finally the ANN predicted results are compared with numerical results for measuring the performance of thenet-work(Fig.11.).The flow chart for the development and training of the ANN networkmodel for performance prediction of a dual-fuel engine is given inFig. 12. ANN used forperformance prediction was made in MATLAB(version 7.0) environment using neural network tool box. Basedon the performance results of the network, the best network architecture was selected. It is chosen for performance prediction of a porous medium engine.

# V. CONCLUSION

This study demonstrates an ideal model of the PM heat regenerative cycle in a new type of PM engine. The novel feature of the PM heat regenerative cycle is the heat feedback and an isothermal heat addition process are realized by using the porous medium as a heat recuperator. Numerical computations shows that the PM heat regenerative cycle can provide much larger net-work output than that of an Otto cycle at a little expense of thermal efficiency, and the effects of expansion ratio and limited temperature on the net-work output are evident. The results obtained could provide significant guidance for the performance evaluation and improvement of practical PM engines. A simulation model is developed using ANN to predict PM engine performance which is very reliable.

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# HYBRID TRANSACTION MANAGEMENT IN DISTRIBUTED REAL-TIME DATABASE SYSTEM

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***ABSTRACT***

*Managing the transactions in real time distributed computing system is not easy, as it has heterogeneously networked computers to solve a single problem. If a transaction runs across some different sites, it may commit at some sites and may failure at another site, leading to an inconsistent transaction. The complexity is increase in real time applications by placing deadlines on the response time of the database system and transactions processing. Such a system needs to process transactions before these deadlines expired. A series of simulation study have been performed to analyze the performance under different transaction management under conditions such as different workloads, distribution methods, execution mode-distribution and parallel etc. The scheduling of data accesses are done in order to meet their deadlines and to minimize the number of transactions that missed deadlines. A new concept is introduced to manage the transactions in "hybrid transaction management" rather than static and dynamic ways setting computing parameters. This will keep the track of the status of mix transaction static as well as dynamic so that we can improve the performance of the system with the advantages of static as well as dynamic.*

***KEYWORDS:*** *Real time system, hybrid transaction management, missed deadlines, database size.*

## I. INTRODUCTION

As the world become smarter and more informatics, demands on IT will grow. Many converging technologies are coming up like rising IT delivery model-cloud computing. Demands of the real time distributed database are also increasing. Many transaction complexities are there in handling concurrency control and database recovery in distributed database systems. Two-phase commit protocol is most widely used to solve these problems [1] and commit protocols are implemented in distributed system. A uniform commitment is guarantee by a commit protocol in such system to ensure that all the participating sites agree on a final outcome. Result may be either a commit or an abort condition.

Many real time database applications in areas of communication system and military systems are distributed in nature. In a real time database system the transaction processing system that is designed to handle workloads where transactions have deadlines. A series of simulation study have been performed to analyze the performance of the system under different transaction management condition such as different workloads, distribution methods, execution mode-Distribution and Parallel, impact of dynamic slack factors to throughput etc. The section 2 describes the concept of a real time database system. The section 3 describes the transaction details. In section 4, proposed model and their parameters are given. The detail of anticipation of result and analysis are given in section 5. The overall conclusions are discussed in section 6.

## II. REVIEW OF LITERATURE

Many database researchers have proposed varieties of commit protocols like two phase commit and Nested two phase commit [2, 3], Presumed commit [4] and Presume abort [3], Broadcast two phase commit , Three phase commit [5,6] etc. These require exchanges of multiple messages, in multiple

phases, between the participating sites where the distributed transaction executed. Several log records are generated to make permanent changed to the data disk, demanding some more transaction execution time [4, 7, 8]. Proper scheduling of transactions and management of its execution time are important factors in designing such systems.

Transactions processing in any database systems can have real time constraints. The scheduling transactions with deadlines on a single processor memory resident database system have been developed and evaluated the scheduling through simulation [9]. A real time database system is a Transaction processing system that designed to handle workloads where transactions have complete deadlines. In case of faults, it is not possible to provide such guarantee. Real actions such as firing a weapon or dispensing cash may not be compensatable at all [10]. Proper scheduling of transactions and management of its execution time are the important factors in designing such systems. In such a database, the performance of the commit protocol is usually measured in terms of number of transactions that complete before their deadlines. The transaction that miss their deadlines before the completion of processing are just killed or aborted and discarded from the system without being executed to completion [11].

# III. TRANSACTION DETAILS

This study is in continuation of [12, 13] work in the same domain [14, 15]. The study follows the real time processing model [16, 17, 18] and transaction processing addressing timeliness [19]. This model has six components: (i) a source (ii) a transaction manager (iii) a concurrency control manager (iv) a resource manager (v) a recovery manager (vi) a sink to collects statistics on the completed transactions. A network manager models the behaviour of the communications network. The definitions of the components of the model are given below.

### 3.1 The source:

This component is responsible for generating the workloads for a site. The workloads are characterized in terms of files that they access and number of pages that they access and also update of a file.

### 3.2 The transaction manager:

The transaction manager is responsible for accepting transaction from the source and modelling their execution. This deals with the execution behaviour of the transaction. Each transaction in the workload has a general structure consist of a master process and a number of cohorts. The master resides at the sites where the transaction was submitted. Each cohort makes a sequence of read and writes requests to files that are stored at its sites. A transaction has one cohort at each site where it needs to access data. To choose the execution sites for a transaction's cohorts, the decision rule is: if a file is present at the originating site, use the copy there; otherwise, choose uniformly from among the sites that have remote copies of the files. The transaction manager also models the details of the commit and abort protocols.

### 3.3 The concurrency control manager:

It deals with the implementation of the concurrency control algorithms. In this study, this module is not fully implemented. The effect of this is dependent on algorithm that chooses during designing the system.

### 3.4 The resource manager:

The resource manager models the physical resources like CPU, Disk, and files etc for writing to or accessing data or messages from them.

### 3.5 The sink:

The sink deals for collection of statistics on the completed transactions.

### 3.6 The Network Manager:

The network manager encapsulates the model of the communications network. It is assuming a local area network system, where the actual time on the wire for messages is negligible.

## IV. TRANSACTION MODEL AND THEIR PARAMETER

The proposed model is discussed below. A common model of a distributed transaction is that there is one process, called as Master, which is executed at the site where the transaction is submitted, and a set of processes, called Cohorts, which executes on behalf of the transaction at these various sites that are accessed by the transaction. In other words, each transaction has a master process that runs at its site of origination. The master process in turn sets up a collection of cohort's processes to perform the actual processing involved in running the transaction. When cohort finishes executing its portion of a query, it sends an execution complete message to the master. When the master received such a message from each cohort, it starts its execution process.

When a transaction is initiated, the set of files and data items that, it will access are chosen by the source. The master is then loaded at its originating site and initiates the first phase of the protocol by sending PREPARE (to commit) messages in parallel to all the cohorts. Each cohort that is ready to commit, first force-writes a prepared log record to its local stable storage and then sends a YES vote to the master. At this stage, the cohort has entered a prepared state wherein it cannot unilaterally commit or abort the transaction but has to wait for final decision from the master. On other hand, each cohort that decides to abort force-writes an abort log record and sends a NO vote to the master. Since a NO vote acts like a veto, cohort is permitted unilaterally abort the transaction without waiting for a response from the master.

After the master receives the votes from all the cohorts, it initiates the second phase of the protocol. If all the votes are YES, it moves to a committing state by force-writing a commit log record and sending COMMIT messages to all the cohorts. Each cohort after receiving a COMMIT message moves to the committing state, force-writes a commit log record, and sends an acknowledgement (ACK) message to the master. If the master receives even one NO vote, it moves to the aborting state by force writing an abort log record and sends ABORT messages to those cohorts that are in the prepared state. These cohorts, after receiving the ABORT message, move to aborting state, force-write an abort log record and send an ACK message to the master. Finally, the master, after receiving acknowledgement from all the prepared cohorts, writes an end log record and then forgets and made free the transaction. The statistics are collected in the Sink [11, 16, 17, 26]. The database is modeled as a collection of DBsize pages that are uniformly distributed across all the NumSites sites. At each site, transactions arrive under Poisson stream with rate Arrival Rate and each transaction has an associated firm deadline. The deadline is assigned using the formula

$$DT=AT+SF*RT \quad (1)$$

Here DT, AT, SF and RT are the deadline, arrival rate, Slack factor and resource time respectively, of transaction T. The Resource time is the total service time at the resources that the transaction requires for its execution. The Slack factor is a constant that provides control over the tightness or slackness of the transaction deadlines.

In this model, each of the transaction in the supplied workload has the structure of the single master and multiple cohorts. The number of sites at which each transaction executes is specifying by the File selection time (DistDegree) parameter. At each of the execution sites, the number of pages accessed by the transaction's cohort varies uniformly between 0.5 and 1.5 times Cohort Size. These pages are chosen randomly from among the database pages located at that site. A page that is read is updated with probability of WriteProb. Summary of the simulation parameter is given in table I.

**Parameter Settings**

The values of the parameter set in the simulation are given in table II. The CPU time to process a page is 10 milliseconds while disk access times are 20 milliseconds.

Table I. Proposed model parameters

| Parameters | Description |
|---|---|
| NumSites or Selectfile | Number of sites in the Database |
| Dbsize_generating_site | Number of pages in the database at same location. |
| Dbsize_remote_site | Number of pages in the database at remote location. |
| ArrivalRate | Transaction arrival rate/site |
| Slackfactor | Slack factor in Deadline formula |
| FileSelection Time | Degree of Freedom (DistDegree) |
| WriteProb | Page update probability |
| PageCPU | CPU page processing time |
| PageDisk | Disk page access time |
| TerminalThink | Time between completion of transaction & submission of another |
| Numwrite | Number of Write Transactions |
| NumberReadT | Number of Read Transactions |

Table II. Assumed values of proposed model parameters

| Parameters | Set Values | Parameters | Set Values |
|---|---|---|---|
| NumSites | 8 | FileSelection Time | 3 |
| Dbsizevary | Max. 200 for generating site and 2200 for remote site | PageCPU | 10ms |
| ArrivalRate | 6 to 8 job/sec | PageDisk | 20ms |
| Slackfactor | 4 | TerminalThink | 0 to 0.5 sec |
| WriteProb | 0.5 | Numwrite/Number Read T | vary |

## V. ANTICIPATION OF RESULTS

The experiment has to be perform using different simulation language like C++Sim, DeNet etc. For this study, GPSS World can be use as a simulator [20]. Literatures are also collected from several recent studies [21, 22, 23, 24, 25, and 26]. The study for performance evaluation starts by first developing a base model. Further experiments were constructed around the base model experiments by varying a few parameters and process of execution at a time.

The performance metric of the experiments is Miss Percent that is the percentage of input transaction that the system is unable to complete before their deadline. A study can be analyzing the performance of the system under different workload with varying the arrival rate of the transaction, dynamic slack factors, execution mode etc. A study can be analyzed the performance using this new concept of transaction to manage the transactions in "hybrid transaction management" rather than static and dynamic ways setting computing parameters technique along with varying database size for generating site and remote site technique. The anticipated experimental results are discussed below.

### 5.1. Comparison of Centralized and Distributed systems

This anticipated experiment compares the performance of the system under centralized and distributed [13]. The distributed systems have higher percentage of miss Transactions than centralized system. This higher miss percentage is due to distance between cohorts. This leads to design of a new perfect distributed commit processing protocol to have a real-time committing performance.

### 5.2. Impact of distribution methods

This anticipated experiment is to be conducted to know the impact of difference between distribution methods to the performance of the system [13]. As an example, we take Exponential distribution and Poisson distribution. The assignment and committing of transactions to cohorts are passed under scheduler using Exponential distribution and Poisson distribution and the statistics of the simulation outputs are to be noted. The Exponential might give more uniform assignment and committing of transactions than Poisson. Poisson might throws higher numbers of transactions giving more collisions of transactions and large number miss percentage of transactions than Exponential. So on many experiments of such similar types might be conducted by using more different distribution rules.

### 5.3. Impact execution mode: Distribution and Parallel

This anticipated experiment compares the output of the system putting the cohorts in parallel with that of distribution execution [13]. From this we might conclude following points. Parallel execution of the cohorts might reduce the transaction response time. The time might require for the commit processing is partially reduced. This is because the queuing time is shorted in parallel and so there are much fewer chances of a cohort aborting during waiting phase.

### 5.4. Impact of slack to Throughput

In this set of experiments, the impact of slack factor to observed on the throughput of the system [13]. The throughput initially might decreases with increase in slack factor due to constraint of distributed real time database. Still there are lots more to study required about other parameters to improve the throughput of the overall system.

### 5.5. Transaction Management

The transactions can be managed in many different ways. In most of the earlier work done simply static or dynamic ways with only database size computing [13,26]. A new concept is introduced to manage the hybrid transactions management with database size for originating site and remote site rather than database size computing parameters, where the values of the parameters are changes or adjust automatically depending on the requirements during the execution the experiment.

## VI. CONCLUSIONS

A series of simulation study have been performed to analyze the performance under different transaction management situation such as different workloads, distribution methods, execution mode-Distribution and Parallel, impact of dynamic slack factors to throughput. The scheduling of data accesses are done in order to meet their deadlines and to minimize the number of transactions that missed deadlines.

Parallel execution of the cohorts reduces the transaction response time than that of serial or distributed execution. The time required for the commit processing is partially reduced, because the queuing time is shorted in parallel and so there are much fewer chances of a cohort aborting during waiting phase. The throughput initially increases with increase in slack factor. But it drops rapidly at very high work loads. The slack factors can be providing by static or dynamics ways.

A new concept is introduced to manage the hybrid transactions in database size for originating site and remote site rather than database size computing parameters. With this approach, the system gives a significant improvement in performance. This approach will keep tracks of timing of the transactions to help them from aborts. This approach will give advance information about the remaining execution time of the transactions. This will help the system to inject extra time to such transactions with the merit of static as well as dynamic ways with the track and does recording of the status of the status of failing transaction so that we can provide an extra slack time to improve the performance of the system. In all the conditions the arrival rate of transaction plays a major role in reducing number of miss percentage and improved performance.

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# A FAST PARTIAL IMAGE ENCRYPTION SCHEME WITH WAVELET TRANSFORM AND RC4

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***ABSTRACT***

*Encryption is used to securely transmit data in open networks. Each type of data has its own features; therefore different techniques should be used to protect confidential image data from unauthorized access. In this paper, a fast partial image encryption scheme using Discrete Wavelet Transform with RC4 Stream Cipher is done. In this method, the approximation matrix (lowest frequency band) is encrypted using the stream cipher as it holds most of the image's information. The encryption time is reduced by encrypting only the part of the image and maintains a high level of security by shuffling the rest of the image using the shuffling algorithm. Selective encryption is a recent approach to reduce the computational requirements for huge volumes of images.*

***KEYWORDS:*** *DWT, Stream Cipher, Shuffling Algorithm, Selective Encryption*

## I. INTRODUCTION

The field of encryption is becoming very important in the present era in which information security is of utmost concern. Security is an important issue in communication and storage of images, and encryption is one of the ways to ensure security. Image encryption has applications in internet communication, multimedia systems, medical imaging, telemedicine, military communication, etc. Information security is becoming more important in data storage and transmission. Images are widely used in several processes. Therefore, the protection of image data from unauthorized access is important. Image encryption plays a significant role in the field of information hiding [1].

There are two basic ways to encrypt digital images: in the spatial domain or in the transform domain [2]. Since wavelet based compression appeared and was adopted in the JPEG2000 standard, suggestions for image encryption techniques based in the wavelet domain have been abundant. However, many of these are not secure as they are based exclusively on random permutations making them vulnerable to known or chosen-plaintext attacks [2]–[4]. The encryption scheme presented here is based on the DWT and RC4 Stream Cipher. The scheme aims at reducing encryption time by only encrypting part of the image, yet maintaining a high level of security by shuffling the rest of the image using the Shuffling Algorithm.

The idea here is to encrypt the approximation matrix (*ca*) with the stream cipher as it holds most of the image's information**. S**tream ciphers typically encrypt one byte at a time. To generate a stream cipher a key is input into a random number generator. The generator produces a keystream consisting of random numbers, each 8 bits long. For a high level of security, the keystream should be unpredictable without knowledge of the input key. The keystream is combined with the plaintext using the bitwise exclusive**-**OR (XOR). In symmetric encryption, the same key is used for encryption and decryption [5], [6]. While encrypting this matrix alone will provide complete perceptual encryption, it would be possible for an attacker to gain information about the image from the other matrices, especially in images that have a lot of edges. Therefore, the horizontal (*ch*), vertical (*cv*), and diagonal (*cd*) matrices will be shuffled using the Shuffling Algorithm.

# II. DISCRETE WAVELET TRANSFORM

Wavelets are mathematical functions that cut up data into different frequency components. Wavelet algorithms process data at different scales or resolutions. The wavelet transform carries out a special form of analysis by shifting the original signal from the time domain into the time–frequency, or, in this context, time–scale domain. It is illustrated in Figure 1. The idea behind the wavelet transform is the definition of a set of basis functions that allow an efficient, informative and useful representation of signals.

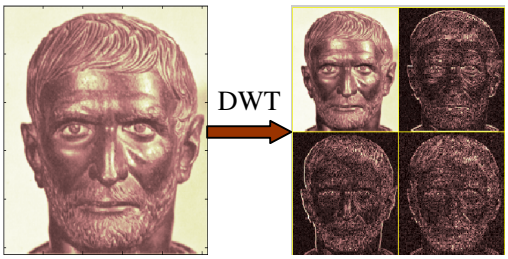



Figure 1. DWT Illustration

A wavelet is a function $\psi \varepsilon L_2$ (R) which meets the admissibility condition is written in equation

$$0 < C_\psi := 2\pi \int_R \frac{\varphi(w)2}{w} \, d\omega < \infty \qquad (1)$$

where, $\psi$ denotes the Fourier transform of the wavelet $\psi$.
The constant $C_\psi$ designates the admissibility constant $\omega$ denotes the signal to be transformed. Approaching $\omega \longrightarrow 0$ gets critical. To guarantee that the above equation (1) is accomplished, we must ensure that $\psi(0) = 0$.
Since $\psi \varepsilon L_2$ (R), also is its Fourier transform $\psi \varepsilon L_2$ (R): $\int_R \varphi(\omega)2 \; d\omega < \infty$.
Therefore, $\varphi(\omega)$ declines sufficiently fast for $\omega >> 0$. In practical considerations, it is sufficient that the majority of the wavelet's energy is restricted to a finite interval. This means that a wavelet has strong localization in the time domain.

## 2.1 Daubechies Wavelet

The family of Daubechies wavelets is most often used for multimedia implementations. They are a specific occurrence of the conjugate-quadrature filters. The Daubechies wavelets (see Figure 2) are obtained by iteration; no closed representation exists. The Daubechies wavelets are the shortest compactly supported orthogonal wavelets for a given number of vanishing moments. The degree $n_0$ of vanishing moments determines the amount of filter bank coefficients to $2n_0$. After embedding, the stego-image will be inverse transformed to the spatial domain. The inverse transforms (IDWT) takes the values of the frequency domain and transfers them back into the time domain.

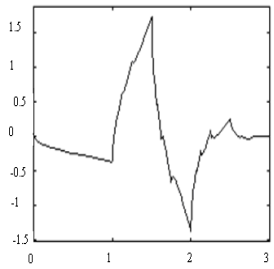



Figure 2. Daubechies Wavelet

# III. STREAM CIPHER

RC4 is a stream cipher, symmetric key algorithm. The same algorithm is used for both encryption and decryption as the data stream is simply XORed with the generated key sequence. The keystream is completely independent of the plaintext used. It uses a variable length key from 1 to 256 bit to initialize a 256-bit state table. The state table is used for subsequent generation of pseudo-random bits and then to generate a pseudo-random stream which is XORed with the plaintext to give the ciphertext.

The algorithm can be broken into two stages: initialization, and operation. In the initialization stage the 256-bit state table, **S** is populated, using the key, K as a seed. Once the state table is setup, it continues to be modified in a regular pattern as data is encrypted.

The initialization process can be summarized by the pseudo-code:

```
j = 0;
for i = 0 to 255:
S[i] = i;
for i = 0 to 255:
j = (j + S[i] + K[i]) mod 256;
swap S[i] and S[j];
```

It is important to notice here the swapping of the locations of the numbers 0 to 255 (each of which occurs only once) in the state table. The values of the state table are provided. Once the initialization process is completed, the operation process may be summarized as shown by the pseudo code below;

```
i = j = 0;
for (k = 0 to N-1) {
i = (i + 1) mod 256;
j = (j + S[i]) mod 256;
swap S[i] and S[j];
pr = S[ (S[i] + S[j]) mod 256]
output M[k] XOR pr
}
```

where, M[0..N−1] is the input message consisting of N bits.

This algorithm produces a stream of pseudo-random values. The input stream is XORed with these values, bit by bit. The encryption and decryption process is the same as the data stream is simply XORed with the generated key sequence.

Some of the RC4 algorithm features can be summarized as:

1. Symmetric stream cipher
2. Variable key length
3. Very quick in software
4. Used for secured communications as in the encryption of traffic to and from secure web sites using the SSL protocol.

# IV. PROPOSED METHOD

In the DWT method, the image first goes through the single-level DWT resulting in four coefficient matrices; the approximation (*ca*), horizontal (*ch*), vertical (*cv*), and diagonal (*cd*) matrices. The lowest frequency sub-band is expressed in the matrix *ca*. The *ca* matrix will be encrypted as it holds most of the image's information using the RC4 Stream Cipher. For encryption, the RC4 keystream will be combined with the *ca* coefficients using the XOR operation. While encrypting this matrix alone will provide complete perceptual encryption, it would be possible for an attacker to gain information about the image from the other matrices. Therefore, the horizontal (*ch*), vertical (*cv*), and diagonal (*cd*) matrices will be shuffled. The Shuffling Algorithm used in the DCT [7] [8] method is used here. The encrypted *ca* matrix and the shuffled *ch*, *cv* and *cd* matrices then undergo the Inverse Discrete Wavelet Transform (IDWT) to produce the encrypted image. This method aims at reducing encryption time by only encrypting part of the image, yet maintaining a high level of security by shuffling the rest of the image. Figure 3 shows the block diagram of the proposed system.

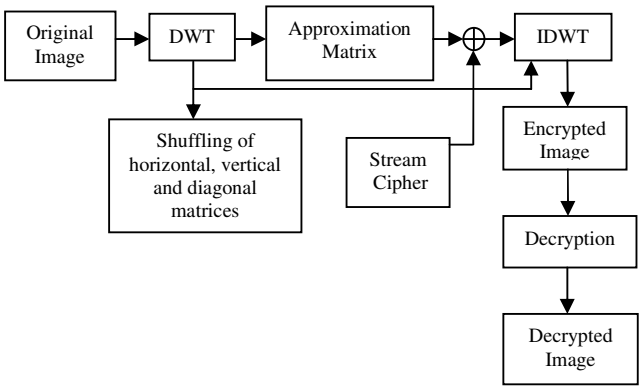



Figure 3. Block Diagram of the Proposed System

In the following, the encryption, decryption and shuffling of the images are illustrated.

## Algorithm to Encrypt Image

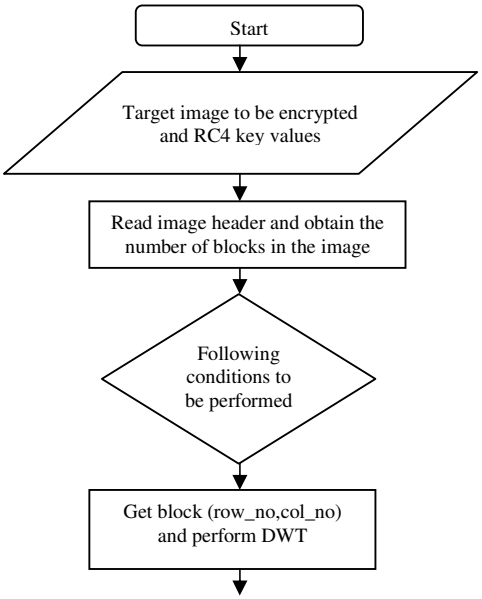
**Input** : Target Image to be encrypted and the stream RC4 Key values.
**Output** : Encrypted Image
**Begin**
Step 1: Read the image header, save the height of the image in variable height & the width in variable width and save the body image in an array imagebody.
Step 2: Obtain how many blocks exist in an image row and how many ones in the column, by dividing the width and height of the image by N, where N is equal to 8 (the required block size).

- NoRowB = Image Height / N;
- NoColB = Image Width / N;

Step 3: For all blocks in the image perform the following:

- Get_block (row_no, col_no)
- Perform a DWT on the block and save the resulted coefficients in an array.
- Round the selected coefficients, convert the selected coefficients to 11 bits.
- Encrypt the selected coefficients by XORing the generated bit stream from the RC4 + Key with the coefficient bits, the sign bit of the selected coefficients will not be encrypted.
- Perform an Inverse Discrete Wavelet Transform (IDWT) and get the new block values and the resulted values could be positive or negative values due to the encryption step.

Step 4: Apply the proposed shuffling algorithm on the resulted blocks to obtain the encrypted image.
**End**
Various steps for encrypting the image is shown in figure 4.



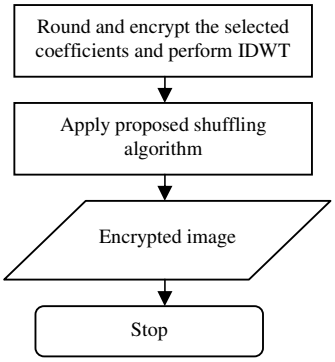



Figure 4. Flowchart for encrypting the image

## Algorithm to Decrypt Image

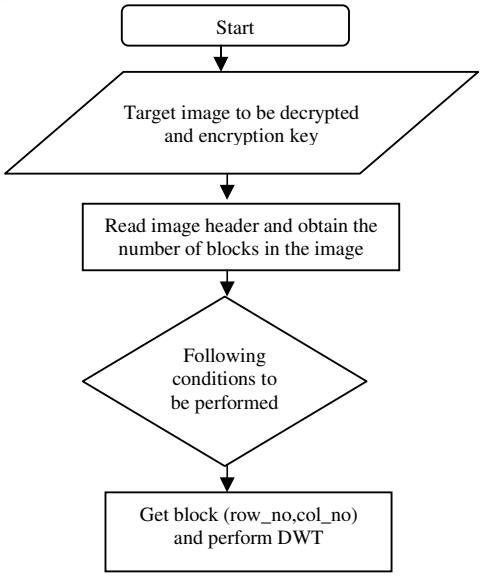
**Input** : Target Image to be decrypted and the Encryption Key
**Output** : Original Image
**Begin**
Step 1: Read the image header, save the height of the image in variable height & the width in variable width and save the body image in an array imagebody.
Step 2: Obtain how many blocks exist in an image row and how many ones in the column, by dividing the width and height of the image by N, where N is equal to 8 (the required block size).

- NoRowB = Image Height / N;
- NoColB = Image Width / N;

Step 3: For all blocks in the image perform the following:

- Get_block (row_no, col_no)
- Perform a DWT on the block and save the resulted values in an array.
- Round the selected coefficients, convert the selected coefficients to 11 bits.
- Decrypt the resulted bits by using the generated bit stream from the RC4 + Key, by performing an XOR operation, the sign bit of the selected coefficients will remain.
- Convert the resulted bits into integer values, and join the sign (from the step above) with each integer, if the coefficient is negative multiply it by −1.
- Perform an Inverse Discrete Wavelet Transform (IDWT) and get the new blocks.

Step 4: Reshuffle the block, since the shuffling algorithm generates the same row and column numbers to return the shuffled blocks into their original locations.
Step 5: Reconstruct the image to get the original Image.
**End**
Various steps for decrypting the image is shown in figure 5.



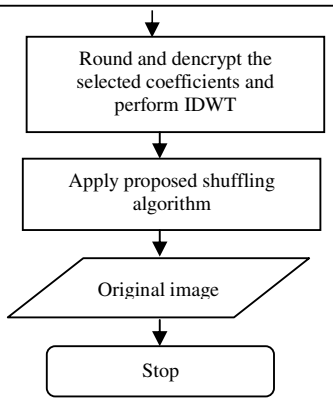



Figure 5. Flowchart for decrypting the image

## Shuffling Algorithm

**Input** : Key, number of blocks in the row (**NoRows**), number of blocks in the column (**NoCols**) and the resulted encrypted image saved in an array.
**Output**: A new shuffled image
**Begin**

```
for i = 0 to (NoRows×NoCols)
NewVal[i]=(K×i)mod(NoRows×NoCols)
endfor
K= 0
for i = 0 to (NoRows×NoCols)
MoveBlock(ImageBlk(NewVal[I]), ImageBlk [K])
K++
endfor
```

**End**
Various steps of shuffling is shown in figure 6.

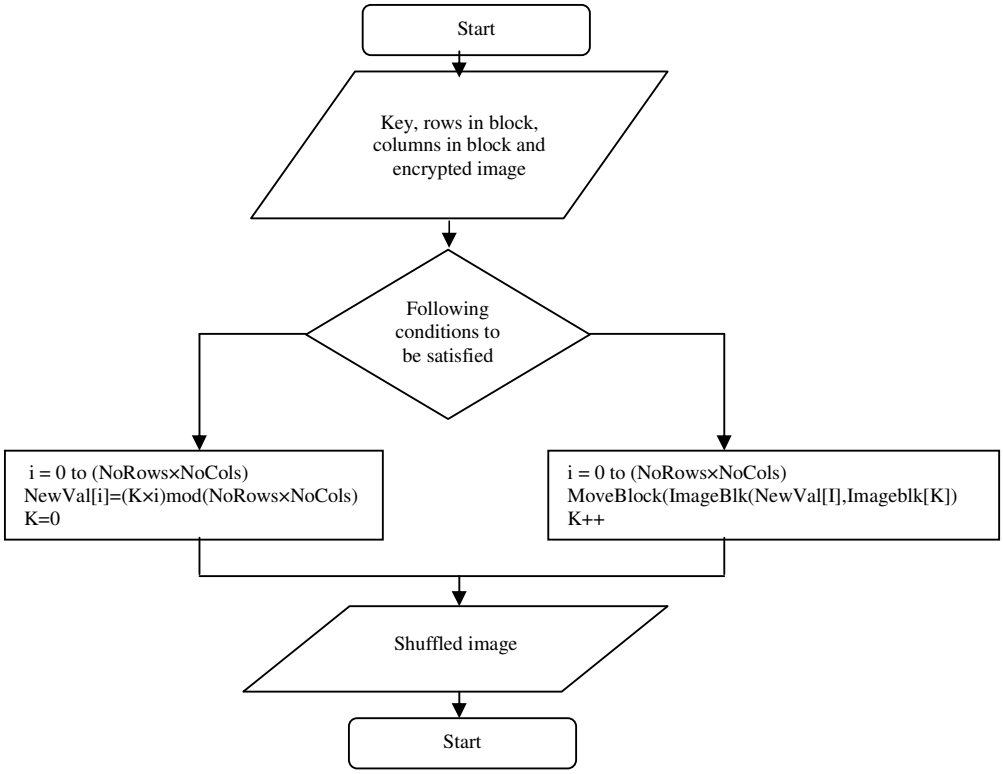



Figure 6. Flowchart of shuffling algorithm

# V. EXPERIMENTAL RESULTS

The performance analysis of selective image encryption DWT with Stream Cipher is measured using the Peak Signal to Noise Ratio (PSNR), Histogram Analysis and Entropy. Figure 7 shows the Original Image used in the DWT method [9] [10]. Figure 8 shows the Selective Encryption of the original image. The Encrypted Image after applying the shuffling algorithm is shown in Figure 9 and in Figure 10, the Decrypted Image is shown.

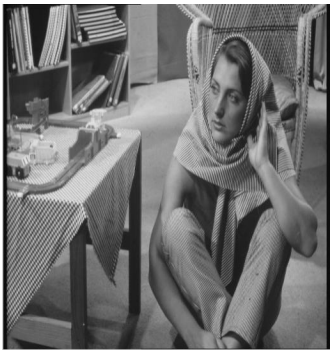


Figure 7. Original Image

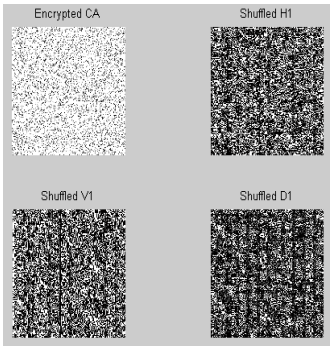



Figure 8. Selective Encryption

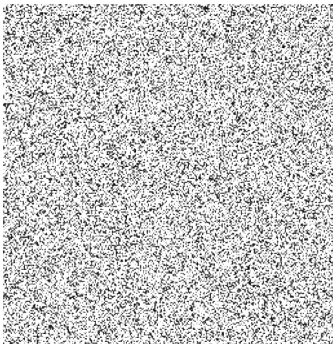


Figure 9. Encrypted Image

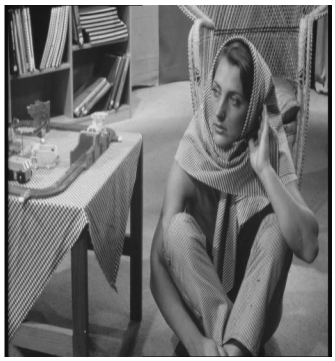


Figure 10. Decrypted Image

Table 1 shows the Performance Analysis of the encrypted and decrypted images in terms of PSNR when tested with different test images of size 512×512. A lower PSNR is obtained in the case of Encrypted Image and a higher PSNR is obtained in the case of Decrypted Image. Higher PSNR value shows a better quality of the image.

Table 1. Performance Analysis of DWT Method

| **Test Images** | **PSNR of Encrypted Image** | **PSNR of Decrypted Image** |
|---|---|---|
| Barbara | 20.5784 | 85.6641 |
| House | 20.7056 | 85.4996 |
| Lena | 20.8768 | 85.5393 |
| Airplane | 20.6219 | 85.4215 |
| Baboon | 20.7354 | 85.3072 |

To demonstrate that our proposed algorithm has strong resistance to statistical attacks, test is carried out on the histogram of enciphered image. Several gray-scale images of size 512×512 are selected for this purpose and their histograms are compared with their corresponding ciphered image. One typical example is shown below. The histogram of the original image contains large spikes as shown in Figure 11 but the histogram of the cipher image as shown in Figure 12, is more uniform. It is clear that the histogram of the encrypted image is, significantly different from the respective histogram of the original image and bears no statistical resemblance to the plain image. Hence statistical attack on the proposed image encryption procedure is difficult.

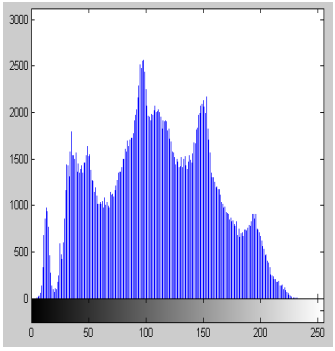



Figure 11. Histogram of Original Image

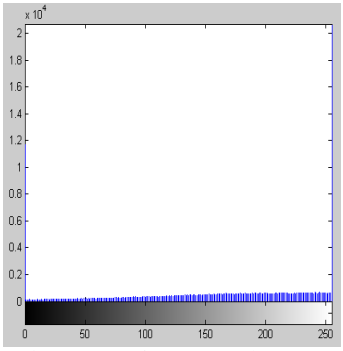



Figure 12. Histogram of Encrypted Image (after shuffling)

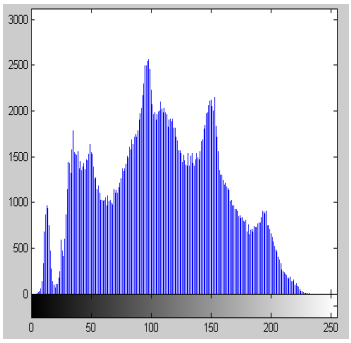



Figure 13. Histogram of Decrypted Image

Entropy is a statistical measure of randomness. Table 2 shows the entropy of different test images of size 512×512.

Table 2. Entropy of different test images

| **Test Images** | **Entropy of Encrypted Image** |
|---|---|
| Barbara | 4.7879 |
| House | 4.7888 |
| Lena | 4.7807 |
| Airplane | 4.7899 |
| Baboon | 4.7916 |

# VI. CONCLUSION

A fast partial image encryption scheme for images using DWT with RC4 Stream Cipher has been presented in this paper. The system only encrypts the lowest frequency band of the image, however it is highly secure as the rest of the other bands are all shuffled using the Shuffling Algorithm. The algorithm is considered as a fast image encryption algorithm, due to the selective encryption of certain portion of the image (lowest frequency band). PSNR values of the encrypted images are low and are resistant to statistical attacks. Hence, better security has been provided.

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# IMPROVE SIX-SIGMA MANAGEMENT BY FORECASTING PRODUCTION QUANTITY USING IMAGE VERIFICATION QUALITY TOOL

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***ABSTRACT***

*With the emergence of a business era that embraces changes as one of its major characteristics, manufacturing success and survival are becoming more and more difficult to ensure. The emphasis is on adaptability to changes in the business environment and on addressing market and customer needs proactively. Changes in the business environment due to varying needs of the customers lead to uncertainty in the decision for requirements from supplier. Flexibility is needed in the value stream map (VSM) to counter the uncertainty in the decision for requirements from supplier. VSM adapts the changes if it is flexible and agile in nature. In this paper a model is presented, which encapsulates the market sensitiveness, process integration, information driver and flexibility measures of VSM demands from supplier and grantee customer requirements. The model was addressed validation to preventive and verification to corrective (VPVC) that is a concept within six-sigma definition. (VPVC) depends on the systematic investigation of discrepancies (failures / deviations) which must be applied in lean six-sigma environment that adopt one piece flow layout. The model is consists of two phases, the first phase is a mathematical model explores the relationship among customer demand, quality, and service level and the leanness and agility of VSM in fast moving consumer goods. The second phase is a quality assurance process of establishing evidence that provides a high degree of preventive that a product involves acceptance of fitness for purpose with customers'. The paper concludes with the justifications of the system input, which depends on the effect of the jerky demand of the market with high quality specification.*

***KEYWORDS:*** *Six-Sigma, VSM management, Simulation Steps.*

## I. INTRODUCTION

The concept of quality is first emerged out of the industrial revolution. Previously products had been made from start to finish by the same team, with handcrafting and tweaking the product to meet 'quality criteria'. In the late 1800s pioneers such as Frederick Winslow Taylor and Henry Ford recognized the limitations of the methods being used in mass production at the time and the subsequent varying quality of output. Taylor established Quality Departments to oversee the quality of production and rectifying of errors, and Ford emphasized standardization of design and component standards to ensure a standard product was produced. Quality was the responsibility of the Quality department and was implemented by Inspection of product output to 'catch' defects.

The Lean Six-Sigma aims to establish a continuous improvement system using a value stream thinking that can be one of the key sources of competitive advantages [1], [2], This work is based on determine economic quantity that was conducted at the company and customer needs. The work examines the operations of the specific company and analyzes the opportunities for the application of Value Stream principles [4]. This work will also audit current material flows and scheduling practices using Value Stream Mapping and Profitability Mapping to identify potential improvements. Based on this information, and the supplemental research, a future state of operations will be recommended as a mathematical model. These objectives postulates in [1], [3],[5]. Total Quality Management is a guide to implement logistics management to control task direction [7]. The Human Equation-Building Profits by Putting People First [8] indicate the simple think about profits but without simulation model

predict future state situation quantity and price. The main objectives are set the economic quantity after known duration to determine VSM orders [10, 12].

Verification of machinery and equipment usually consists of Design Qualification - DQ [13], Installation Qualification - IQ [14], Operational Qualification - OQ [15] and Performance Qualification - PQ [16]. DQ is usually a customer's job by confirming through review and testing that the equipment meets the written acquisition specification. Otherwise, the process of IQ, OQ and PQ is the task of validation.

In such a situation, the specifications of the parts and restructuring proposals should be appended to the qualification document whether the parts are genuine or not. Torres and Hyman have discussed the suitability of non genuine parts use and provided guidelines for equipment users to select appropriate substitutes which are capable to avoid adverse effects [17]. When machinery/equipment qualification is conducted by a standard endorsed third party such as by an ISO standard accredited company for a particular division, the process is called certification [18], [19]. Prospective validation - the missions conducted before new items are released to make sure the characteristics of the interests which are functional properly and which meet the safety standards [20], [21]. Some examples could be legislative rules, guidelines or proposals [22], [23], [24], methods [25], theories/hypothesis/models [26[, [27].

The other function is retrospective validation - a process for items that are already in use and distribution or production. The validation is performed against the written specifications or predetermined expectations, based upon their historical data/evidences that are recorded. If any critical data is missing, then the work can't be processed or can only be completed partially [20], [26].

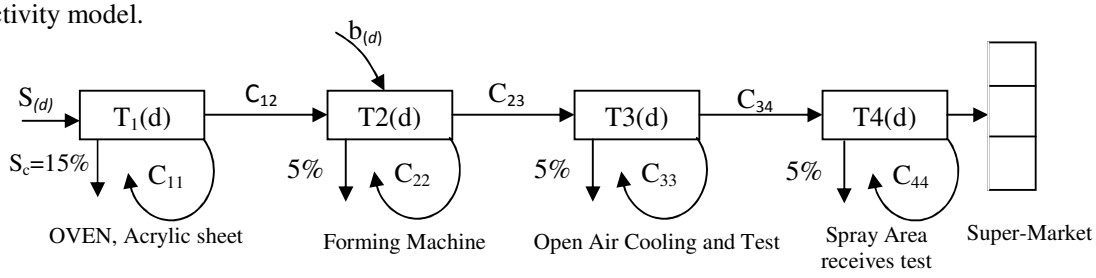
Verification can be expressed by the query "Are you building the thing right?" and validation by "Are you building the right thing?" "Building the right thing" refers back to the user's needs, while "building it right" checks that the specifications be correctly implemented by the system.

# II.PRODUCTION MODEL ( PHASE I )

Mat-lab and C# software used to formulate a two phases code that present an economic order quantity after known days (future state), also used to determine best quantity with respect to profits taking into account marketing and inventory costs that appeared if company produce extra product. The unit price is exchange if customer demands difference about company productivity. The ideal situation when customer demand is equal to company productivity with acceptance requirements.

The next sections are divided to two parts, the first section (Company production model) determines the forecasting quantity based on rework and scrap, the second section (Economic Production Quantity) determines the economic quantity based on customer needs and company profits.

Sketch-1 consider the following company's productivity model is analyze the effect of supplier provide quantity retention rate on the company productivity's form so that it can predict the future need for number of machines, labors and resources. Assume that the company has estimates of the percentages of parts reworking or scraping before day off, this estimation represent current state of productivity model.




$S_{(d)}$ : Quantity provided by Supplier
$b_{(d)}$ : beside parts fed Machine $T_2$ ,
$T_i(d)$: Task series in day (d),
$C_{ji}$ : No. of work piece transferred from j to i.
Sc: Scrap percentage

Sketch-1: Sequencing machine and its

In this work develops a matrix equation helps in this analysis to control quantities and its direction weather feed or feedback. The next values used in model to illustrate the model working, these values may change to match different company model. The first phase illustrates in (Figure 1).
Suppose that the current order is 500 parts, and the company managers decide to increase productivity to 1000 per day from now on. The company estimates that [10%] of the $T_1(d)$ will reworking. The number of $T_1(d+1)$ in the following day will be 0.1(500) +1000=1050, then it will be 0.1(1050)+1000=1105, and so on. Let $T_1$ (d) be the number of oven acrylic sheet in day d, where d=1, 2, 3, ... then in day d+1, the number of oven acrylic sheet is given by: $T_1(d+1)$=10% of previous oven acrylic sheet repeating in the same day + 1000 new oven acrylic sheet, [0.1 x $T_1(d)$+1000]. The number of $T_1(d)$ is known in the first day of analysis (which is 500); the previous equation will solve step by step to predict the number of $T_1(d+1)$ in the future that shared in feeding super-market in the final station in the production line. If 15% of parts in $T_1(d)$ are scraping, then $T_1(d)$feed $T_2(d)$by $C_{12}$ = [100% of parts ] – [ 10% reworked in previous step + 15% scraped from previous step]= 75% of parts returns as $T_2(d)$, also $C_{22}$ = 5% of $T_2(d)$rework its operation. And 200 extra parts fed from $T_1(d)$ from besides production line. Then in day (d+1) the number of forming acrylic sheets is given by: $T_2(d+1) = 0.75\ T_1(d) + 0.05\ T_2(d) + 200$

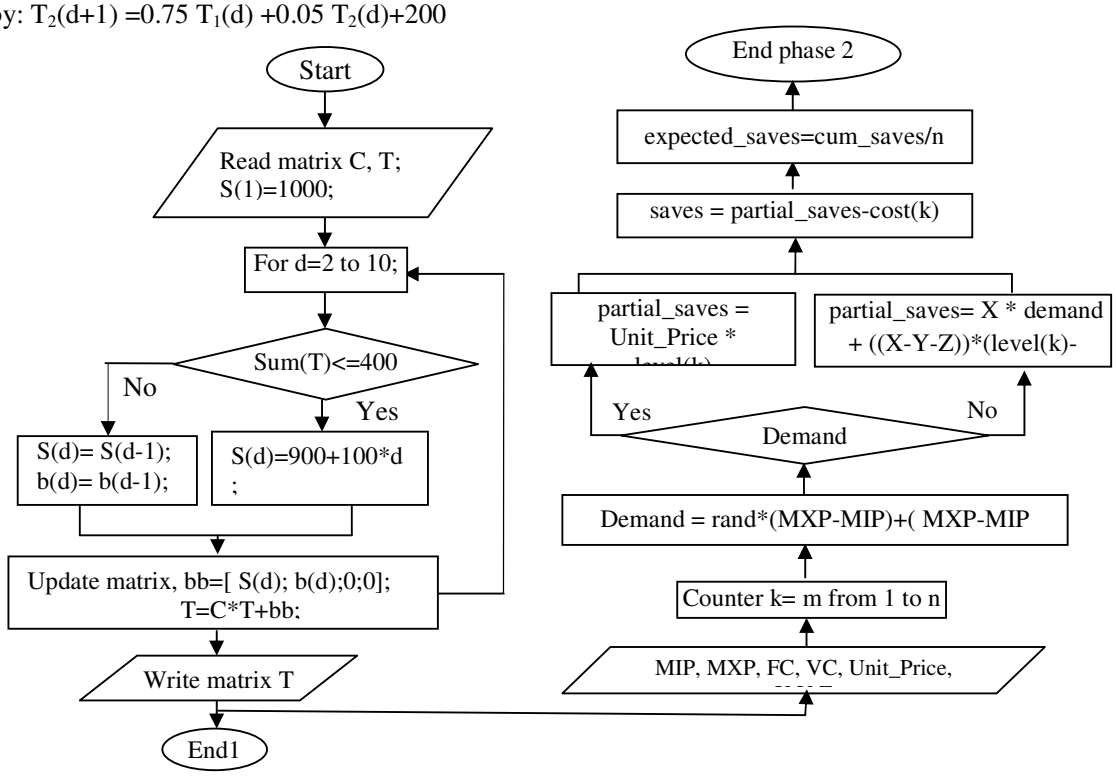



Figure 1. Flow-Chart of phase I of simulation program.

Suppose that [5%] of the $T_2(d)$ and $T_3(d)$ scraped. And $C_{22}, C_{33}, C_{44}$ = 5% of the $T_2(d)$, $T_3(d)$ and $T_4(d)$ reworked. $C_{23}$, $C_{34}$ = [100% - 5% reworked on previous station – 5% scraped from previous station ] =90% of the forming machine operation and open air cooling test return to increase its quality.

$T_3(d+1) = 0.9\ T_2(d) + 0.05\ T_3(d)$
$T_4(d+1) = 0.9\ T_2(d) + 0.05\ T_3(d)$
The next matrix formulate the previous situation, it may take different values with respect to any company situation. The suitable matrix will form as next:

$$\begin{bmatrix} \mathbf{T_1(d+1)} \\ \mathbf{T_2(d+1)} \\ \mathbf{T_3(d+1)} \\ \mathbf{T_4(d+1)} \end{bmatrix} = \begin{bmatrix} 0.1 & 0 & 0 & 0 \\ 0.75 & 0.05 & 0 & 0 \\ 0 & 0.9 & 0.05 & 0 \\ 0 & 0 & 0.9 & 0.05 \end{bmatrix} \begin{bmatrix} \mathbf{T_1(d)} \\ \mathbf{T_2(d)} \\ \mathbf{T_3(d)} \\ \mathbf{T_4(d)} \end{bmatrix} + \begin{bmatrix} \mathbf{1000} \\ \mathbf{200} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix}$$

To study the effects of supplier provide quantity and thermoforming sheets that fed from other oven, the model must be generalized to be:

$T_1(d+1)=C_{11}\ T_1(d)+ S(d)$
$T_2(d+1)=C_{12}\ T_1(d)+ C_{22}\ T_2(d)+b(d)$
$T_3(d+1)=C_{23}\ T_2(d)+ C_{33}\ T_3(d)$
$T_4(d+1)=C_{34}\ T_3(d)+ C_{44}\ T_4(d)$

$$\begin{bmatrix} T_1(d+1) \\ T_2(d+1) \\ T_3(d+1) \\ T_4(d+1) \end{bmatrix} = \begin{bmatrix} C_{11} & C_{21} & 0 & 0 \\ C_{12} & C_{22} & 0 & 0 \\ 0 & C_{23} & C_{33} & 0 \\ 0 & 0 & C_{34} & C_{44} \end{bmatrix} \begin{bmatrix} T_1(d) \\ T_2(d) \\ T_3(d) \\ T_4(d) \end{bmatrix} + \begin{bmatrix} S(d) \\ b(d) \\ 0 \\ 0 \end{bmatrix}$$

Suppose that the initial total productivity order is 1512 consists of 500 parts at $T_1(d)$ station, 375 parts at $T_2(d)$, 337 parts at $T_3(d)$, 304 parts at $T_4(d)$. The company wants to study the over 10 days the effects of increasing supplier provides 100 each day and fed from other oven by 50 per day until the total productivity orders reaches 2554 product, then the customer orders fluctuation between the productivity after 10 days and 2500 parts.

S(d)=900+100*d
b(d)=150+50*d  where d: 1, 2, 3, 4, . . . 10

The model is simulated by MATLAB; a Matlab script file to predict the future state productivity to feed super market for the next 10 days appears in the next table:

```
% model's coefficients
      C =[0.1,0,0,0;0.75,0.05,0,0;0,0.9,0.05,0;0,0,0.9,0.05];
% initial vector of current state values
       T =[500;375;337;304];
% initial supplier provide and fed from beside production line
      S(1)=1000;
      b(1)=200;
% E is 4x10 matrix
      E(:,1)=T;
% Counter over days from 2 to 10
      for d=2:10;
        %maximum WIP
        if sum(T)<=2554;%maximum WIP
        %increase supplier provided and fed from other production line by 100
          S(d)=900+100*d;
        %increase supplier provided and fed from other production line by 50
          b(d)=150+50*d;
        else
        %hold status quo quantity
        S(d)= S(d-1);
        b(d)= b(d-1);
      end
```

```
        %Update matrix
                bb=[ S(d); b(d);0;0];
                T=C*T+bb;
                E(:,d)=T;
        end
%plot the results
plot(E'),hold,plot(E(1,:),'O'), plot(E(2,:),'+'), plot(E(3,:),'*'),...
plot(E(4,:),'x'),xlabel('days'),ylabel('Number of orders'),...
gtext('OVEN'), gtext('Forming Machine'), gtext('Open air test'), gtext('Spray area
received'),title('Economic order quantity')
```

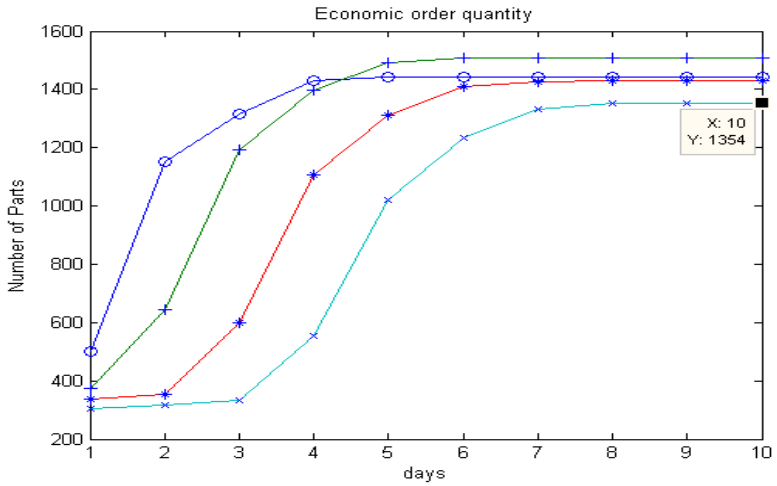



Figure 2. # Of products estimated from a certain production line

(Figure 2) illustrates the predicted quantity that follow the previous speculates about specific company. The quantity is 1345 parts appears after 8 days. The customer requirements are fluctuated between **1000** and **2500** parts in determined days.

# III. OPTIMAL ECONOMIC ORDER QUANTITY

The optimum production level handling between different tasks station, the transportation cost will be large if line produce too many units without market form, if there is any units not handled weather transportation system become in position will increase transportation cost and that is a worst case. The fixed cost of the transportation system is $4 part/day; the cost of producing forming bathtubs during these four steps is $35 above the fixed cost. The historical file illustrates that there is a fluctuation between 1000 and 2500 parts are produced, if the parts handled in its time will save $160/day (unit price) but else if not handled in time (over production)will cost company $60 for transportation and $45 for inventory, this mean part will sell by $55.
The simulated model to estimate the optimum quantity to produced and transported to design a suitable super market:

```
        %number of simulation runs
                n=10000;
        % 1354 parts exists + 1000+200 provided from besides =2554
                Min_Productivity = MIP;
                Max_Productivity = MXP;
                Fixed_Cost = FC;
                Variable_Cost = VC;
                level=[ MIP: MXP ]; %(1200)+1
```

```
cost = FC + VC * level;  %fixed cost + production cost*# of products
    for k=1:1201 %1201 = (2554 – 1354) +1
        cum_saves=0;
        for m=1:n
            demand = floor(rand*( MXP - MIP)+ (MXP-MIP)+1);
            if demand >= level(k)
%unit price - transportation cost = $160 net profit
                partial_saves = Unit_Price * level(k);
            else
%extra product have transportation cost and inventory cost
        bulimic_Unit_Price = X;
        transportation cost= Y;
        Inventory cost= Z;
            partial_saves= X * demand +((X-Y-Z))*(level(k)-demand);
    end
        saves = partial_saves-cost(k);
        cum_saves = cum_saves+saves;
    end
        expected_saves=cum_saves/n;  % y axis
        p(k,1)=level(k);
        p(k,2)=expected_saves;
    end
plot(p(:,1),p(:,2),'+',p(:,1),p(:,2),'-'),xlabel('NO. of bathtubs'),ylabel('Transportation saves $')
```

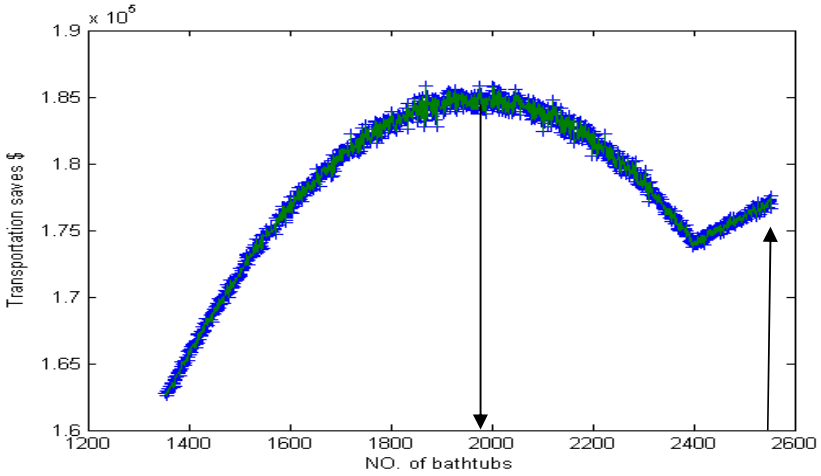



Figure 3. Optimum order quantity

(Figure 3) illustrates the optimum quantity saves the handling cost and increase profit is 1990 parts/day that represents pacemaker quantity. Also (Figure 3) illustrates unobserved behavior after producing 2400 parts, this behavior set domain for productivity as follow:

$$\#\text{of products} \begin{cases} P = 1990 \text{ / day} \\ P > 2400 \text{ / day} \end{cases}$$

# IV. QUALITY MODEL VPVC (PHASE II)

Lean Six-sigma tools must be integrated by the factory to reduce defects and achieves customer requirements. (Figure 4) illustrates the VPVC flowchart, VPVC is a program need a digital cam which

fixed to prevent scrap via pick sequence of pictures related with time to stop machine when process cycle time completed. The program applies the same code among processes to reduce inspection time (NNVA) from 1.25 *min* to 0.28 *sec*.

(Figure 4) consists of two steps, the first step is the validation code and the second step is the verification code. The main objective is produce customer demand meet with his specification.

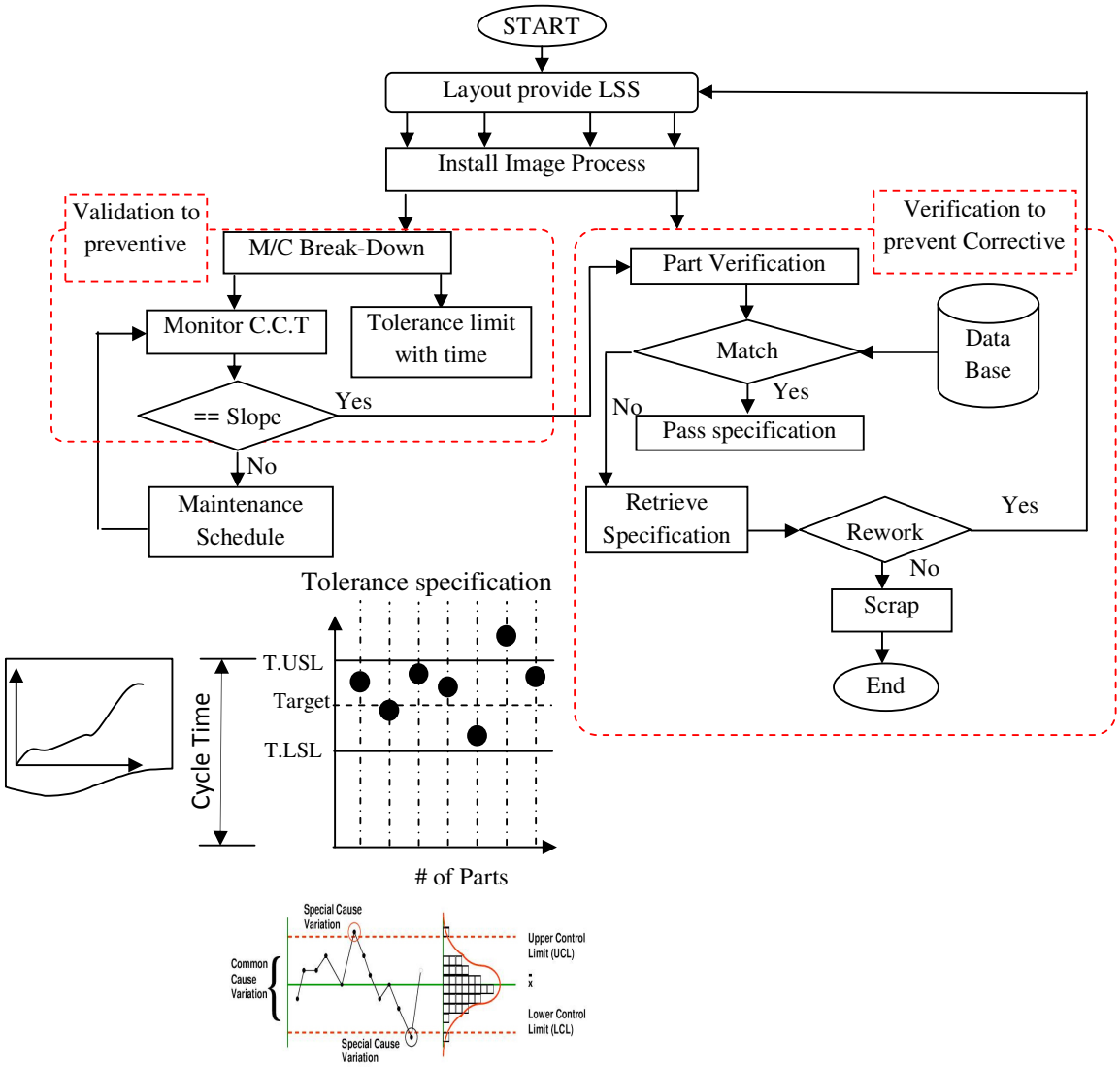



Figure 4. The VPVC flowchart.

### 4.1. Validation Code ( Step I ):

Validation to preventive is executed on machines by monitor cumulative cycle time of the sequence activities in VSM to build a standard reference time line for every part. If there is any deviation far this reference the validation will diagnosis the fault. The reference line will thrown preventive attention.

1. READING Labor _ID.
2. READING Job_ID and stamp the $Clock_{(start)}$
3. Reading VSM data (Supplier serial, R.M serial, loaded M/c, $Clock_{(end)}$)

```
t=[0:1:12]';
y=[Comulative Clock picked up for start and end of every product]';
```

```
yy=[Clock without any follow up for the labors]';
n=3
P=Polyfit (t, y, n), PP=Polyfit (t, yy, n);
Plot (t, y, 'r.-', t, yy, 'g.-'); hold on; h = plot (t, y, 'r', t, yy, 'r'); hold off; ylim([0 200])
hold, grid on, type fitfun
start = [1;0]; options = optimset('TolX',2);
estimated_lambda = fminsearch (@(x) fitfun(x, t, y, h), start, options)
xlabel ('The Scanning steps for assembly Line'),...
   ylabel ('The Expected time monitoring with Validation System in (Sec)'),...
   gtext ('The Standard Scanning time with I.Verification')
   title ('Using Time Line to control IdealStandard lines')
```

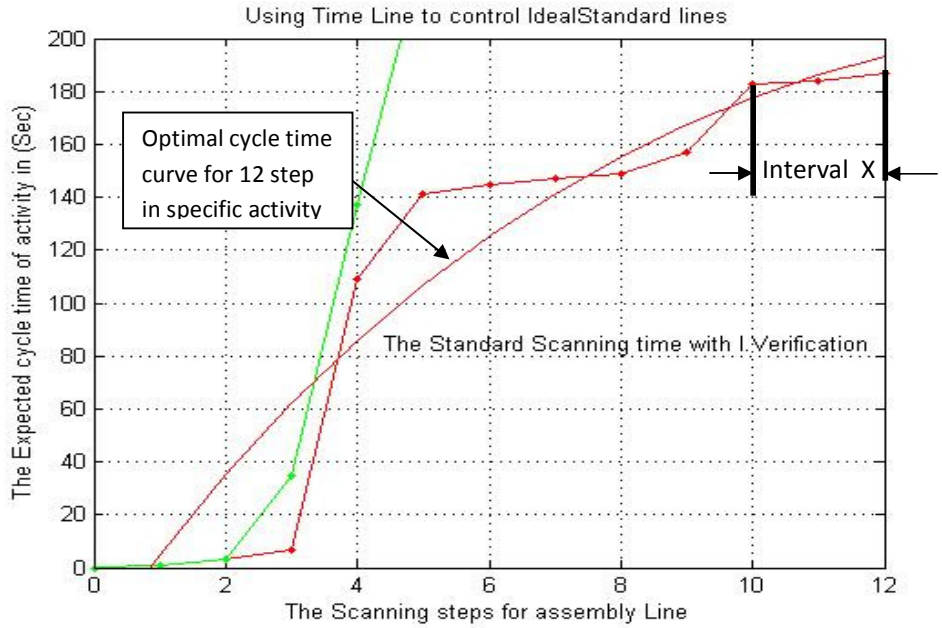



Figure 5. The optimal time curve for the steps executed in specific activity

(Figure 5) illustrates the interval X that match with clock monitor; the machine is stopped automatically by the control system to prevent scrap parts. The next phase applies code between processes to reduce NNVA time.

### 4.2. Verification code (Step II)

Verification to corrective is the second section in the proposed flowchart, the verification executed by picked sequential images in fixed time domain to decide verification level of the product.

```
using System;
using System.Drawing;
using System.Drawing.Imaging;
using System.Security.Cryptography;

namespace ZagazigUniversity
{
        public class Verification
        {
                public enum Check
                {       Part_Pass,Points_Defect,Size_Defect              };
```

```
        public static Check Compare(Bitmap fileNameBase, Bitmap Produced)
                {
                        Check cr = Check.Part_Pass;
                        if (fileNameBase.Size != Produced.Size)
                                { cr = Check.Size_Defect; }
                        else
                        {
System.Drawing.ImageConverter ic = new System.Drawing.ImageConverter( );
                                byte[ ] baseImage1 = new byte[1];
btImage1 = (byte[ ])ic.ConvertTo(fileNameBase, baseImage1.GetType( ));
                                byte[ ] producedimage2 = new byte[1];
btImage2 = (byte[ ])ic.ConvertTo(produced, producedimage2.GetType( ));

                SHA256Managed shaM = new SHA256Managed( );
                byte[ ] hash1 = shaM.ComputeHash(baseImage1);
                byte[ ] hash2 = shaM.ComputeHash(producedimage2);
                for (int i=0; i<hash1.Length && i<hash2.Length && cr==Check.Part_Pass; i++)
                                {
                                  if (hash1[i] != hash2[i])
                                  cr = Check.Points_Defect;
                                }
                        }
                        return cr;
                }
        }
}
```

Figure 6. The comparison product process result.

(Figure 6) illustrates the result of comparison among picture which stored in database and every part produced. This result determine the rework percentage the used in mathematical model (phase I).

## V. CONCLUSION

The proposed steps is divided into two phases, every phase have two steps that formulate a code that present a future quantity after known days (future state), the first phase based on percentage of reworking and scraping parts during the same tasks of different operations. The starting production point is 1354 parts as shown in (Figure 2) and the best productivity is 1990 or 2500 parts as shown in (Figure 3). The model used to determine best quantity with respect to profits taking into account marketing and inventory costs that appeared if company produce extra product. The unit price is exchange if customer demands difference about company productivity in overproduction case. The ideal situation when customer demand is equal to company productivity.

The second phase illustrates a preventive and corrective system for rapid modeling and manufacturing of objects with contact dimension. The system needs the 2D optical digitizing system and the dimension reconstruction software. The optical digitizer utilized a white-light source for image acquisition that makes this technology cost-effective, fast in image acquisition and portable for various applications. The inspection time (NNVA) was reduced from 1.25 *min* to 0.28 *sec.*

## ACKNOWLEDGEMENTS

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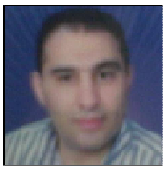

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# OPTIMAL PATH FOR MOBILE AD-HOC NETWORKS USING REACTIVE ROUTING PROTOCOL

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## *ABSTRACT*

*Reactive protocols don't maintain routing information or routing activity at the network nodes if there is no communication. Reactive protocols determine a route to some destination only when somebody wants to send a packet to that destination. The route discovery usually occurs by flooding the route request packets throughout the mobile ad-hoc networks. Our approach is using reverse route calculation in RRQ packets and reverse route calculation in RRP packets to obtain optimal path communication between sender nodes to destination node for mobile ad-hoc networks.*

***KEYWORDS:*** *MOBILE AD-HOC NETWORKS, REACTIVE ROUTING PROTOCOL*

## I.INTRODUCTION

### 1.1 Mobile ad-hoc network

Mobile ad-hoc networks are self organizing and self configuring multi hop wireless networks where the structure of the network changes dynamically because of mobility of nodes [1]. A MANET can be a standalone network or it can be connected to external networks (Internet).The main two characteristics of MANET are mobility and multi hop and hence multi hop operation requires a routing mechanism designed for mobile nodes. In mobile ad-hoc networks where there is no infrastructure support as is the case with wireless networks, and since a destination node might be out of range of a source node transmitting packets; a routing procedure is always needed to find a path so as to forward the packets appropriately between the source and the destination [1]. Within a cell, a base station can reach all mobile nodes without routing via broadcast in common Wireless networks. In the case of ad-hoc networks, each node must be able to forward data for other nodes.Therefore the requirements of the protocol for MANET are loop free paths, optimal path, dynamic topology maintenance etc.

### 1.2 Reactive Routing Protocol

Reactive routing protocol is an on-demand routing protocol for mobile ad-hoc networks. The protocol comprises of two main functions of route discovery and route maintenance. Route discovery function is responsible for the discovery of new route, when one is needed and route maintenance function is responsible for the detection of link breaks and repair of an existing route. Reactive routing protocols, such as the AODV [4], the DSR [5], do not need to send hello packet to its neighbor nodes frequently to maintain the coherent between nodes. Another important feature of reactive routing protocol is that it does not need to distribute routing information and to maintain the routing information which indicates about broken links [3]. Both the neighbor table and routing information would be created when a message

needed to be forwarded and nodes maintain this information just for certain lifetime. When communication between two nodes completes, nodes discard all these routing and neighbor information. If another message needs to be forwarded, same procedure continues.

# II. OUR APPROACH TO FIND THE OPTIMAL PATH

We calculate optimal path between source node and destination node by two steps, which are executed both in forwarding RRQ (route request) packets and RRP (route reply) packets.

## 2.1 Reverse route calculation in RRQ

Each node will create a route table called reverse route table when it receive a RRQ. This reverse route table is different from other route tables. It records and indicates the route to the source node, not the destination node. Furthermore, node will calculate the distance every time, and most importantly, this distance is the key fact to choose the shortest path to the source node [2]. First of all, when a node receives RRQ, it will create a route entry which indicates the next hop (the node forwarding the RRQ) to the source node and calculate the distance between this next hop node and the source node. Second, this node will also make the similar decision when it receives RRQ, update route table or discard RRQ [3]. For convenience, we use two variables (*First* and *new*) to indicate how to make reverse route calculation in RRQ. The *first* is distance the node calculates at the first time when it receives RRQ or the distance at current time. The *new* is distance the node calculates when it receives RRQ again. Once an intermediate node receives a RRQ, the node sets up a reverse route entry for the source node in its route table. Reverse route entry consists of <Source IP address, Source seq. number, number of hops to source node, IP address of node from which RRQ was received>. Using the reverse route a node can send a RRP to the source. Reverse route entry also contains life time field. RRQ reaches destination, In order to respond to RRQ a node should have in its route table unexpired entry for the destination and sequence number of destination at least as great as in RRQ (for loop prevention). If both conditions are met & the IP address of the destination matches with that in RRQ the node responds to RRQ by sending a RRP. If conditions are not satisfied, then node increments the hop count in RRQ and broadcasts to its neighbours. Ultimately the RRQ will make to the destination. Let us consider the temporary topology of mobile ad-hoc network as shown below in Fig. 1.

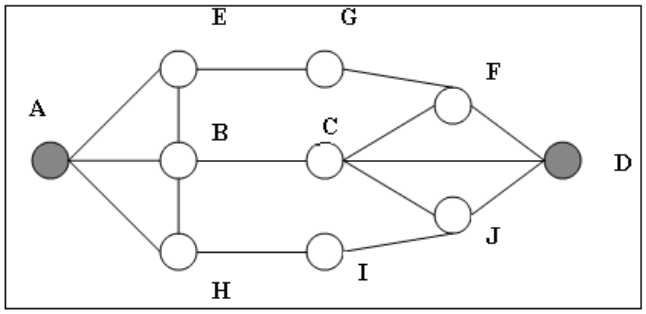


Fig.1 Temporary topology of mobile ad-hoc network

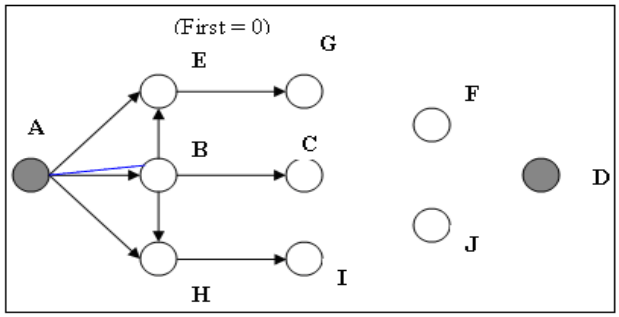


Fig.2 Node creates reverse route entry and calculates distance in RRQ

[*Note: ——— new
⟶ RRQ]

In Fig. 2, when node A broadcasts RRQ to node B and E, node B and E will create a reverse route entry which indicates the next hop to the source node when packet arrives at node B and E. Besides, node B and E would calculate the distance between forwarding node and source node. In this situation, the next hop to source node for node B and E is node A and the *first* for node B and E is 0, because node A is both the forwarding node and source node. And then, when node B forwards the RRQ to node E, node E will calculate the *new* which is the distance between forwarding node (node B) and the source node ( A). Then, node E will compare the *new* with *first* (the first distance when node E receives RRQ from node A). Since *new* > *first*, the node discard this RRQ.

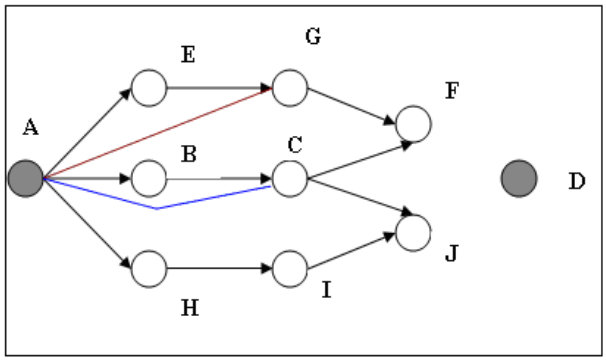


Fig.3a) Update route table in RRQ

[* Note: ——— new
——— first
⟶ RRQ]

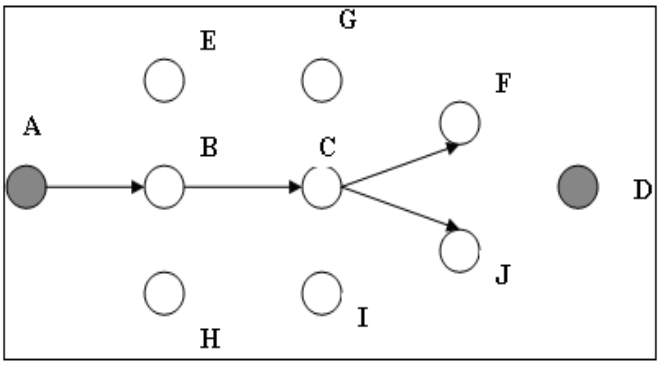


Fig.3b) The result of updating route table in RRQ

[ * Note: ⟶RRQ]

As shown in Fig. 3(a), node F creates reverse route entry when it receives RRQ from node G and select node G as the next hop to the source node (A). The same process happen when node F receives the same RRQ again from node C. Node F calculates the *new* between the forwarding node (node C) and the source node (A). Since *new* < *first*, node F updates the route table and select node C as the next hop to the source node. Fig. 3(b) is the finally route after node C broadcasts RRQ.

## 2.2 Reverse route calculation in RRP

We use similar calculation mechanism to get the optimal path in forwarding RRP. The only difference is that the distance we calculate in RRP is from the node forwarding RRP to the destination node.

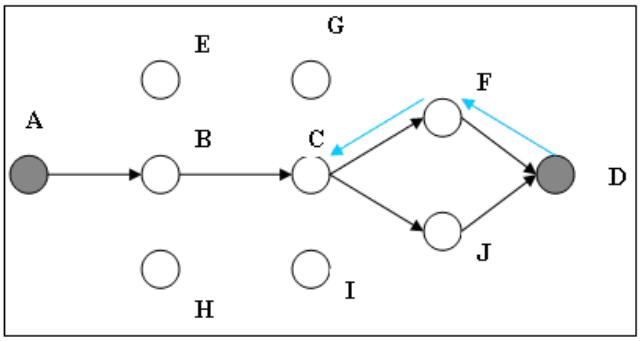


Fig.4 Node creates reverse route entry and calculates distance in RRP

[*Note: ⟶ RRQ
⟶ RRP]

As shown in Fig. 4, the destination node (node D) receives the RRQ from node F and then creates the RRP and unicasts it to node F. Node F forwards this RRP to node C according to the route table created by forwarding the RRQ.

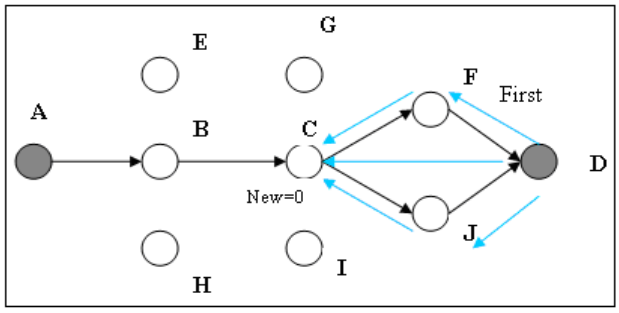


Fig .5a) update route table in RRP

[ *Note: RRQ
RRP]

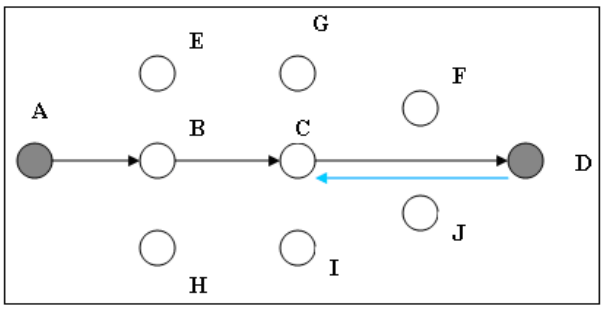


Fig.5b) Optimal path communication between A to D

When node C receives the RRP from node F, it creates the route entry and calculates the fir***st***, which indicates the next hop is node F when the message whose destination node is node D arrives at node C. And then, when node C receives RRP from node D, it will calculates the *new* and finds that *new* < *first*, as shown in Fig. 5(a) and (b), node C updates the route table, and then finally optimal path is found.

## III. CONCLUSION AND FUTURE WORK

In this paper, we propose a reactive routing protocol, consists of two steps to find the optimal path: first, we calculate the shortest path to the source node and create reverse route table, second, we filter these paths to obtain optimal path communication for mobile ad-hoc networks by calculating distance to the destination node.

As future work, we will make some measurement to increase the reliability of the reactive routing protocol, especially on how to fix the link when new node joints in the mobile ad-hoc network or when a node dies in the mobile ad-hoc network.

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# POWER QUALITY RELATED APPROACH IN SPACE VECTOR CONVERTER

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***ABSTRACT***

*A cycloconverter is a power electronics device used to convert constant frequency AC power to adjustable voltage adjustable frequency AC power without any DC link. Cycloconverter inject significant harmonics and non-standard frequency components like inter harmonics (i.e., non integer multiples of power frequency) into power systems. The impact of cycloconverter on power quality is studied, and the relation between power quality indices and cycloconverter control strategies are developed. Control strategies based on the switching sequence SVPWM (i.e., space vector pulse width modulation). Control strategies are proposed to minimize the power quality impact of the converters. An innovative wavelet filter concepts are illustrated with the help of wavelet transform tool to recognize the power quality.*

***KEYWORDS:*** *Cycloconverter, power electronics, power quality, harmonics, wavelet.*

## I. INTRODUCTION

Cycloconverters are static frequency changers (SFCs) designed to convert constant voltage, constant frequency AC power to adjustable frequency AC power without any intermediate DC link. The basic principle of a cycloconverter was proposed and patented by Hazeltine in 1926[1]. However, practical and commercial cycloconverters were not available until thyristors were developed in the 1960s. With the invent of large rating thyristors and the development of microprocessors and microcontrollers feed gate driver circuits, cycloconverters are widely used in heavy industries like rolling mills, cement industries, ship propellers. Basic cycloconverter is naturally commutated converter capable of flowing power in either direction. The sizes of the converter depend upon the rating of the thyristors. Compared with rotary frequency changers, its losses are considerably low. Cycloconverters can deliver a nearly sinusoidal waveform resulting in minimum torque pulsations for the case of rotating loads [8]. However it produces highly distorted input currents. Highly distorted input currents can significantly decrease electrical power quality [11]. The cycloconverter input currents and output voltages contain harmonics as well as inter harmonics. In this paper a soft-switching technique is adapted to reduce these power harmonics and the power quality impact of thyristor-controlled cycloconverters is studied. Power quality impact includes; total harmonic distortion (THD), impact on distribution transformers, and impact on communication lines [14].Basic theory of cycloconverter: A cycloconverter consists of one or more back to back connected controlled rectifiers. The delay angles of those rectifiers are modulated so as to provide AC output voltage at desired frequency and amplitude. The three phase cycloconverter consists of 18 thyristors but higher pulse order systems are large and complicated and tend to be applicable for large rating load. Based on the structure of the rectifiers used in cycloconverters are classified into half wave and bridge cycloconverter. The AC-AC matrix converter, an alternative to an AC-DC-AC converter for voltage and frequency transformation,

has two major advantages, i.e., it requires no DC-link reactive component and it allows bi-direction power flow. Since its description [2], the matrix converter has been of intensive ongoing research [3-6] and an aspect which attracts much of the research effort is the pulse-width modulation control. For matrix converters used in variable-speed drive applications the ideal PWM algorithm should have;

* Provide independent control of the magnitude and frequency of the generated output voltages.
* Give sinusoidal input current with adjustable phase shift,
* Achieve the maximum possible range of output to input voltage ratio,

Satisfy the conflicting requirements of minimum low-order harmonics and minimum switching losses. Hitherto two control schemes, the Venturini method and the space vector modulation, have been used to meet the above listed requirements. However, owing to completely different design approaches, the two PWM algorithms give distinctly different performances with regard to operation in unbalanced or distorted supply voltages. The brief circuit diagram of matrix converter is given in the Fig.1. Nine bidirectional switches are so arranged that any of the three input phases can be connected to any output phase. Each of the bidirectional switches employed is constructed by connecting a pair of power devices back to back. One power diode is provided in series to protect the IGBTs from reverse voltage blocking. The switching control obeys a rule that only one of the three switches connected to an output phase can and must be ON at any one time. It provides short circuit protection as well as uninterrupted load current flow.

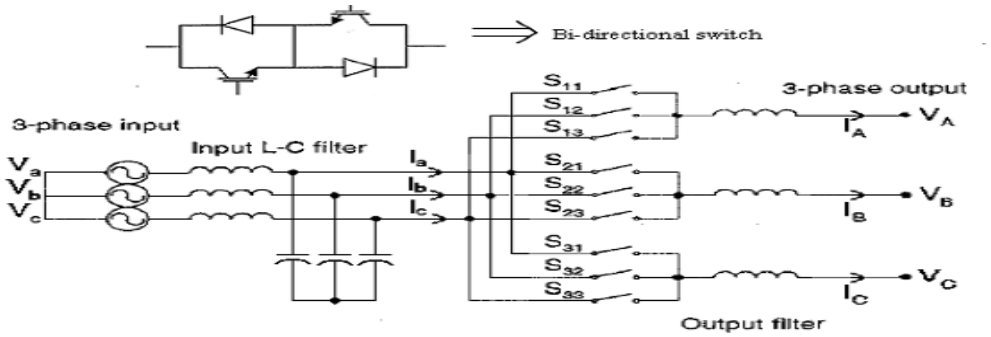


Figure 1. Matrix converter topology

## II. SVM METHOD

The SVM methods represent the three-phase input currents and output line to line voltages as space vectors. It is based on the concept of approximating a rotating reference vector with those voltages physically realizable on a matrix converter. For nine bi-direction switches there are 27 possible combination of switching status, which is also divided into five groups. The first group consists of six vectors whose angular positions vary with change of the input voltages. These groups are invalid for SVM technique. The next three groups of switch combinations have two common features; namely each of them formulates a six-sextant hexagon as shown in Fig.2. These, so named 'stationary vectors', are used to synthesis the desire output voltage vector. The remaining group comprising three zero vectors is also used in this method. The modulation process selection can be done in two ways one is vector selection and another vector on time duration calculation. At a given time instant Ts, the SVM selects four stationary vectors to approximate a desired reference voltage with the constraint of unity input power factor.

### 2.1. Switching technique of SVM

To calculate the on time duration of the chosen vectors, the four vectors selected are combined into two sets leading to two new vectors adjacent to the reference voltage vector. According to space vector modulation theory, the integral value of the reference vector over one sample time interval can be approximated by the sum of the products of the two adjacent vectors on time intervals. General formulae derived for estimating the vector on time intervals have been given as,

_____ (1)

_____ (2)

_____ (3)

_____ (4)

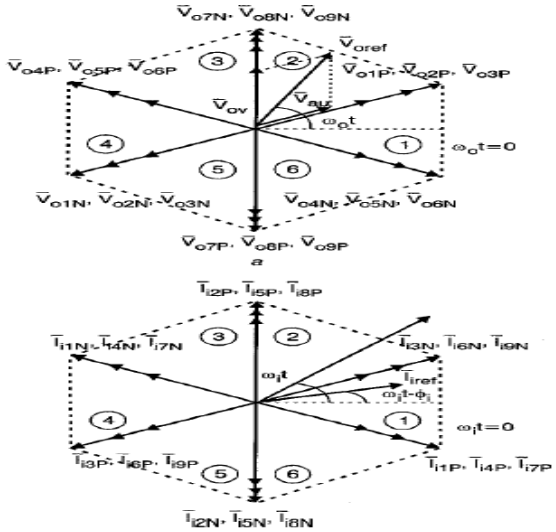


Figure 2. Output voltage and input current hexagon

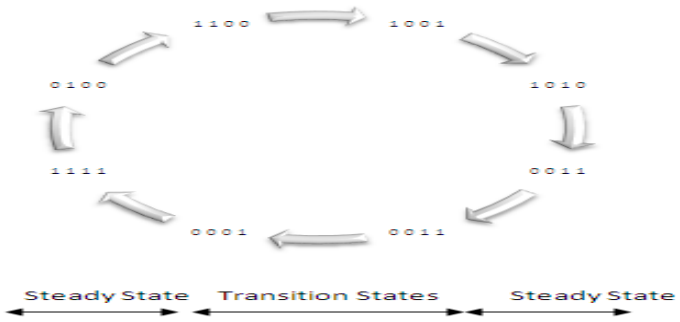


Figure 3. Switching states

Where — the voltage transfer ratio, $\theta_{0 \text{ and}}$ $\theta_i$ are the phase angles of the output voltage and input current vectors respectively. These values are limited within 0 to $60^0$ ranges. The zero vector on-time is given by,

(5)

The above procedure is performed at every sampling interval.

## 2.2. Circuit description

Matlab simulink has been applied here to simulate the matrix converter from three phase to single phase conversion. Fig.4 shows the schematic of vector converter. Reference voltage of the space vector converter can be adjusted to control the output frequency of the converter.

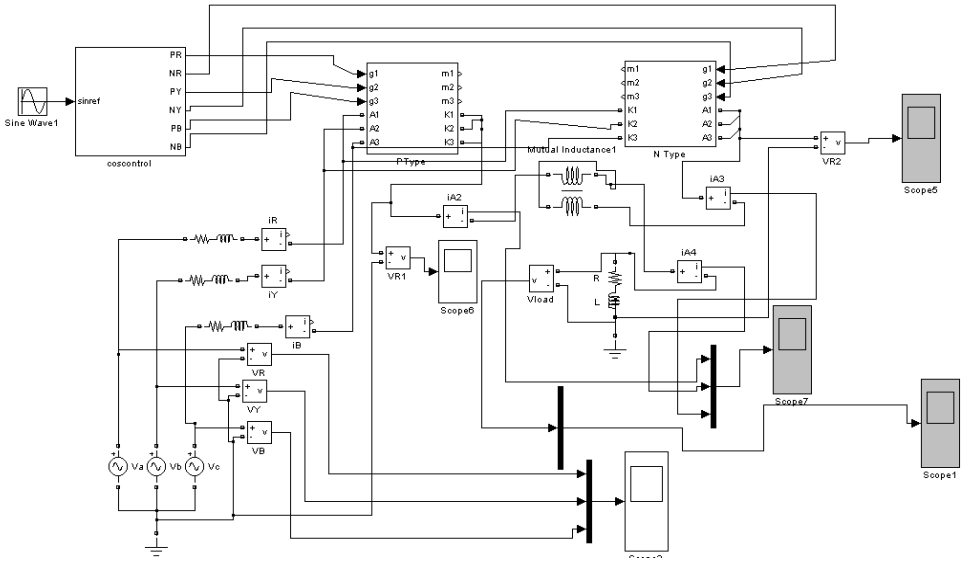


Figure 4. Space vector cycloconverter technique

## 2.3. Results

Three phase single phase vector simulation Fig.5 and power quality of that output phase has been measured through Matlab. Three phase 230V supply voltage, applied to the converter and the output voltage power quality is measured through power GUI tool. Total harmonic distortions for different angles have been studied and compared with the conventional converter. Total control strategy has been performed with the help of field programming gate array embedded system.

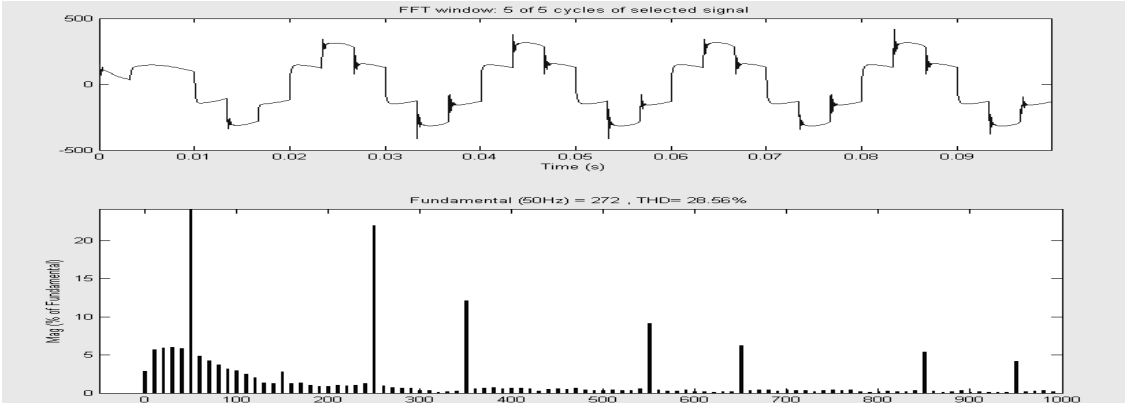


Figure 5. Spectrum analysis

**Sampling time = 3.25521e-005 sec, samples per cycle = 614.4, fundamental = 272 peak (192.4 RMS), Total Harmonic Distortion (THD) = 28.56%**

**Table 1 Harmonic order**

| Harmonics Hz | Order | Amplitude Volt |
|---|---|---|
| 0 | | 7.86 |
| 10 | | 15.47 |
| 20 | | 16.19 |
| 30 | | 16.31 |
| 40 | | 15.95 |
| 50 | Fundamental | 272.05 |
| 60 | | 13.14 |
| 70 | | 11.43 |
| 80 | | 10.08 |
| 90 | | 8.54 |
| 100 | H2 | 7.98 |
| 110 | | 6.78 |
| 120 | | 5.48 |
| 130 | | 3.73 |
| 140 | | 3.35 |
| 150 | H3 | 7.49 |
| 160 | | 3.47 |
| 170 | | 3.56 |
| 180 | | 2.78 |
| 190 | | 2.47 |
| 200 | H4 | 2.47 |
| 220 | | 2.55 |
| 230 | | 2.78 |
| 240 | | 3.42 |
| 250 | H5 | 59.70 |
| 260 | | 2.70 |
| 270 | | 2.01 |
| 280 | | 1.70 |
| 290 | | 1.82 |
| 300 | H6 | 0.87 |
| 310 | | 0.84 |
| 320 | | 0.32 |
| 330 | | 0.59 |
| 340 | | 0.69 |
| 350 | H7 | 32.93 |
| 360 | | 1.55 |
| 370 | | 1.77 |
| 380 | | 2.00 |
| 390 | | 1.49 |
| 400 | H8 | 1.86 |

$10^{th}$ harmonics of this system has been studied through GUI system and voltage vs. magnitude data has been generated and shown in table 1.

# III. CONCLUSION

In this article a new ride-through module for a matrix converter has been proposed. The ride through capability has been achieved by the minimal addition of hardware and software into the matrix converter. A method for harmonic analysis of the converter waveforms is presented which can accurately predict the harmonic performances of either control method. Modelling of matrix converter losses is described, resulting in a meaningful tool for power circuit design and device optimization. The main advantage of the SVM method lies in lowering switching losses compared to the Venturini method, however, exhibits superior performance in terms of input current and output voltage harmonics. Natural sampling avoids baseband distortion, where PWM requires more computational effort than UPWM because of calculation of the crossing times.

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# SEARCH RESULT CLUSTERING FOR WEB PERSONALIZATION

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## *ABSTRACT*

*The main problem faced by the users of web search today is the quality and the amount of the results they get back. The results frustrate a user and consume his precious time. Existing search engines perform keyword based searches without taking into account the user intent and semantics of the user query. Hence to improve searching in the WWW, a new personalized search index provides a conceptual relation between the search keywords and the pages, which matches the user's information need. The proposed approach aims to mine a reduced set of effective search result for enhancing the searching experience. In this project, we propose and build a personalized 2D web search model. We store and maintain user's long-term dynamic profile based on user search and use it to personalize. We use ontology at client side to solve the cold start problem and expand the query and generate clusters of similar results. We store client's profile as a weighted ontology tree. We use web search results from an existing search engine and re-rank them based on client's profile.*

***KEYWORD***: clustering, web personalization, ontology, web mining

## I. INTRODUCTION

Web search is difficult because it is hard for users to construct queries that are both sufficiently descriptive and sufficiently discriminating to find just the web pages that are relevant to the user's search goal. Ambiguous queries lead to search result sets containing distinct page groups that meet different user search goals. To filter out irrelevant results the users must refine their search by modifying the query .Users must understand the result set to refine queries effectively; but this is time consuming, if the result set is unorganized. Web personalization using web search result clustering is one approach for assisting users to both comprehend the result set and to refine the query. According to Eirinaki and Vazirgiannis [3] personalization is defined as follows: Web site personalization can be defined as the process of customizing the content and structure of a Web site to the specific and individual needs of each user taking advantage of the user's navigational behaviour.Web page clustering identifies semantically meaningful groups of web pages and presents these to the user as clusters. The clusters provide an overview of the contents of the result set and when a cluster is selected the result set is refined to just the relevant pages in that cluster. An ontology is a model of the world, represented as a tangled tree of linked concepts. Concepts are language-independent abstract entities. They are expressed in this ontology using English words and phrases only as a simplifying convention. Semantic ontology is to improve automated text processing by providing language-independent, meaning-based representations of concepts in the world. The ontology shows how concepts are related and their properties.The objective of a web personalization system is to provide users with the information they want or need, without expecting from them to ask for it explicitly.
Search personalization is based on the fact that individual users tend to have different preferences and that knowing the user's preference can be used to improve the relevance of the results the search engine returns. There have been many attempts to personalize web search. These attempts usually differ in

1. How to infer the user preference, whether explicitly by requiring the user to indicate information about herself or implicitly from the user's interactions,
2. What kind of information is used to infer the user's preference.
3. Where this information is collected or stored, whether on the client side or the server side, and
4. How this user preference is used to improve the results' retrieval accuracy.

Any system providing personalization services will need to store some information about the user in order to achieve its goal. The simplest way to construct a profile is to collect users' preferences explicitly, by asking them to submit the necessary information manually before any personalization can be provided. However, studies like [6] show that users are generally not willing to spend extra time and effort on specifying their intentions especially when the benefits may not be immediately obvious. There are also often concerns about privacy, and users might not be very comfortable supplying personal information to search servers.

Section I indicates the work done in the field of search personalization. Section II describes the proposed search personalization system. Section III describes the proposed OntoPersonalization Ranking algorithm. The experimental results and conclusion are explained in later sections

## II. RELATED WORK

Hearst and Pedersen [2] showed that relevant documents tend to be more similar to each other, thus the clustering of similar search results helps users find relevant results. Several previous works [8][9][2][5][4] are conducted to develop effective and efficient clustering technology for search result organization. In addition, Vivisimo [7] is a real demonstration of this technique. Lee and Bordin defines a class of personalized search algorithms called "local-cluster" algorithms that compute each page's ranking with respect to each cluster containing the page rather than with respect to every cluster. In particular, they propose a specific local-cluster algorithm by extending the approach taken by Achlioptas et al. [10]. They proposed local-cluster algorithm considers linkage structure and content generation of cluster structures to produce a ranking of the underlying clusters with respect to a user's given search query and preference. The rank of each document is then obtained through the relation of the given document with respect to its relevant clusters and the respective preference of these clusters. Zamir and Etzioni [8][9] presented a Suffix Tree Clustering (STC) which first identifies sets of documents that share common phrases, and then create clusters according to these phrases. Our candidate phrase extraction process is similar to STC but we further calculate several important properties to identify salient phrases, and utilize learning methods to rank these salient phrases. Some topic finding [1][3] or text trend analysis [9] works are also related to our method. The difference is that we are given titles and short snippets rather than whole documents.

Motivated by Lee and Bordin's local cluster algorithm we propose a cluster based probability algorithm. Our algorithm considers cluster probability, user choice obtained through local webcluster database and defined ontology to produce a ranking of the underlying clusters with respect to a user's given search query and preference. The rank of each document is then obtained through the relation of the given document with respect to its relevant clusters and the respective preference of these clusters.

## III. PROPOSED SYSTEM

In any Information Retrieval model the important challenge is to present the results which the user is expecting for his query. Efficiency is a challenge in this that has been addressed very well so far. Current web search engines serve all users, independent of the special needs of any individual user. Personalization of web search is intended to carry out retrieval for each user incorporating his/her interests. Even though there exist some personalization models that facilitate personalization to some extent they fail in cases where the results are totally biased towards a dominant keyword in the search query. Generally, the user doesn't want to go beyond two pages of results. And in most cases the results relevant to the dominant keywords fill up the first few pages making the user unsatisfied.

We propose a client side personalization model that would effectively overcome the above stated problems. The system uses a middleware approach. We build entity search capabilities on top of an existing search-engine such as Goggle by "wrapping" the original engine. The middleware would take

a user query, use the search engine API to retrieve top K web pages most relevant to the user query, and then cluster those web pages based on their associations to real people. The architecture is a pipeline that receives the input query, obtains search results from a search engine, filters the results applying a clustering algorithm and then gets the clusters. The steps of overall approach are illustrated in Fig 1

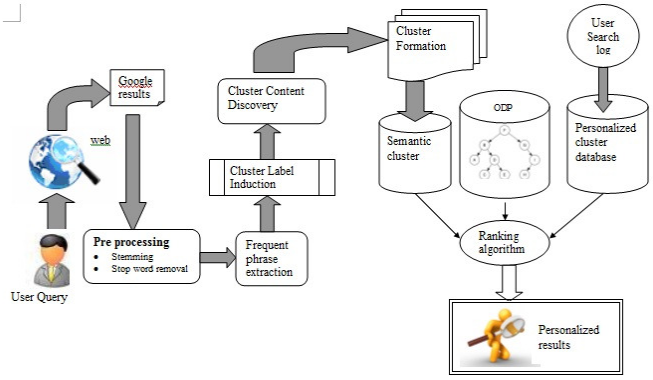


Fig 1: System Diagram

The system is divided into three major sections

### 1. Search Result Fetching

We first get the WebPages of search result lists returned by a web search engine. We have extracted results from yahoo, google and msn. So the first search is the conventional meta-search based on these keywords. These WebPages are analysed by an HTML parser and the result items are extracted. Generally, there are only titles and query-dependent snippets available in each result item. We assume these contents are informative enough because most search engines are well designed to facilitate users' relevance judgment only by the title and snippet, thus it is able to present the most relevant contents for a given query. Each extracted phrase is in fact the name of a candidate cluster, which corresponds to a set of documents that contain the phrase.

**2. Cluster formation:**

The system first identifies meaningful cluster labels and only then assigns search results to these labels to build proper clusters. The algorithm consists of five phases. Phase one is pre-processing of the input snippets, which includes tokenization, stemming and stop-word marking. Phase two identifies words and sequences of words frequently appearing in the input snippets. In phase three, a matrix factorization is used to induce cluster labels. Phase four snippets are assigned to each of these labels to form proper clusters. The assignment is based on the Vector Space Model (VSM) and the cosine similarity between vectors representing the label and the snippets. Finally, phase five is post processing, which includes cluster merging and pruning. The algorithm is as follows:

```
/** Phase 1: Pre processing */
for each document
{
do text filtering;
identify the document's language;
apply stemming;
mark stop words;
}
/** Phase 2: Feature extraction */
discover frequent terms and phrases;
/** Phase 3: Cluster label induction */
use LSI to discover abstract concepts;
for each abstract concept
```

```
{
find best-matching phrase;
}
prune similar cluster labels;
/** Phase 3: Cluster label induction */
use LSI to discover abstract concepts;
for each abstract concept
{
find best-matching phrase;
}
prune similar cluster labels;
/** Phase 4: Cluster content discovery */
for each cluster label
{
use VSM to determine the cluster contents;
}
/** Phase 5: Final cluster formation */
calculate cluster scores;
apply cluster merging;
```

**3. Cluster ranking:**

Finally, clusters are sorted for display based on their score, calculated using the following simple formula: $C_{score}$ = label score × ||C||, where ||C|| is the number of documents assigned to cluster C. The scoring function, although simple, prefers well-described and relatively large groups over smaller, possibly noisy ones.

As we retrieved the original ranked list of search result $R=\{r(di|q)\}$, where $q$ is current query, $di$ is a document, and $r$ is some (unknown) function which calculates the probability that $di$ is relevant to $q$. Traditional clustering techniques attempt to find a set of topic-coherent clusters $C$ according to query $q$. Each cluster is associated with a new document list, according to the probability that $di$ is relevant to both $q$ and current cluster:

$C = \{Rj\}$, where $Rj = \{r(di|q, Rj)\}$ (1)

In contrast, our method seeks to find a *ranked* list of clusters $C'$, with each cluster associated with a cluster name as well as a new ranked list of documents:

$C' = \{r'(ck, Rk|q)\}$, where $Rk = \{r(di|q, ck)\}$ (2)

As shown in Eq. 1 and Eq. 2, we modify the definition of clusters by adding cluster names $ck$, and emphasize the ranking of them by function $r'$.

The OntoPersonalization algorithm for ranking clusters is the direct analogy of the SP algorithm where now clusters play the role of pages. That is, we will be interested in the aggregation of links between clusters and the term content of clusters. In order to incorporate the user relevant query-independent web page importance, personalized result ranks, ontology and original web ranks (as an approximation for the real page rank) are aggregated to form the final result ranking. Thereby each result item is assigned a score (indicating probability) corresponding to the number of results ranked below it. Then the total score of a result is a weighted sum of its scores with respect to each ranking, i.e.,

score = (w*0.7)_score1 +(0.3 * w)_score2 +C_score (3)

where score is the final score of the result item, based on which the results are finally re-ranked before being submitted to the user, score1 is the score of the result item within the personalized result set, score2 is the score of the result item within the given ontology result set, and such that the

combination threshold w serves as a personalization control parameter. C_score is the score obtained by Lingo algorithm. By adjusting the value of w, the user controls the personalization level. We have considered a 70-30 ratio for personalization and Ontology tree. The threshold can be set by the user. For instance, setting w to 0 would mean that the user would be presented with the original result ranked on the basis of defined ontology tree, and on the other hand setting w to 1 would mean that the new result set is the same as the personalized set. Our web search personalization system provides a control over threshold value w, thus enabling the user to cancel the personalization at any point of time. The figure 2 indicates the overall ranking process.

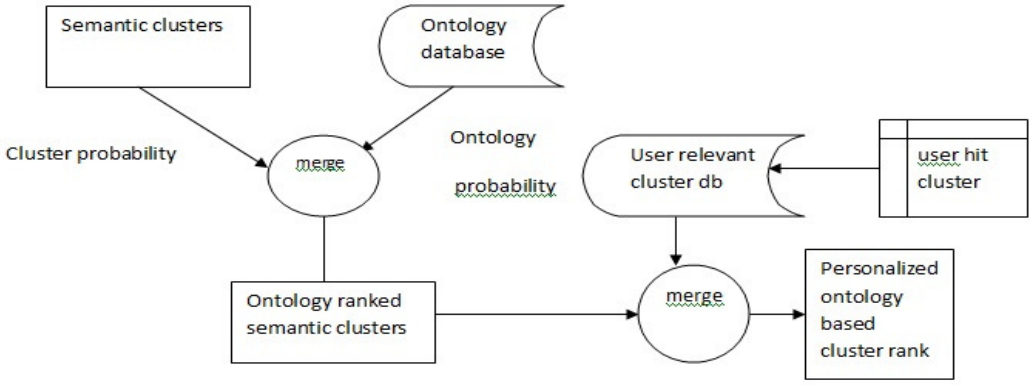


Fig 2: The Cluster Merging Diagram

# IV. THE ONTO PERSONALIZATION RANKING ALGORITHM

Our goal is to utilize the user context to personalize search results by re-ranking the results returned from a search engine for a given query Assuming an ontological user profile with interest scores exists and we have a set of search results, Algorithm is utilized to re-rank the search results based on the interest Scores, user choice score and the semantic cluster score. The proposed algorithm is capable of presenting results according to the user desired level of personalization.

The Onto Personalization algorithm works in three steps

1. Ontology Ranking
2. Pure personalization Ranking
3. Final Ranking

The algorithm uses previous clicked cluster data, stored in webcluster database,to create task oriented dynamic profile of user. The ontology for the given keyword is identified and extracted from the ontology database. Thus appropriate weights are added to the cluster depending on given personalization level. Thus using dynamic user profile and ontology cluster list we finally obtain a ranked cluster list which satisfies the user intent is obtained.

**Algorithm: Onto Personalization Ranking**

**Input:** Cluster List, Ontology Database, Webcluster Database,User Query

**Output:** Ranked Output: Ranked Personalized List

**Steps:**

1. Get the user query.
2. Retrieve the ontology tree node, on, matching the query.
   /*this node acts as parent node*/
3. Get all child nodes, add weight to them.
4. Get user query
5. Retrieve all records where query matches the webcluster database keyword.
6. Add weights to those clusters
7. Get user personalization –Ontology ranking ratio.
8. Multiply the ontology list with the ontology ratio.
9. Multiply personalized list personalization ratio.
10. Merge the ontology and personalization list

11. Match the list with the semantic cluster list obtained from Lingo algorithm.
12. Discard non matching clusters.
13. Re rank the final list.

## V. EXPERIMENTAL RESULTS

The figure 3 shows the system interface of our proposed system for the query "computer mouse".

Fig 3: System Interface

The figure 4 shows how the cluster score increases as the user searches the same term repeatedly. Figure 5 indicates the user satisfaction percentage with the offered results. The graph shows the increase in cluster ranking as the system learns more about the intent of user.

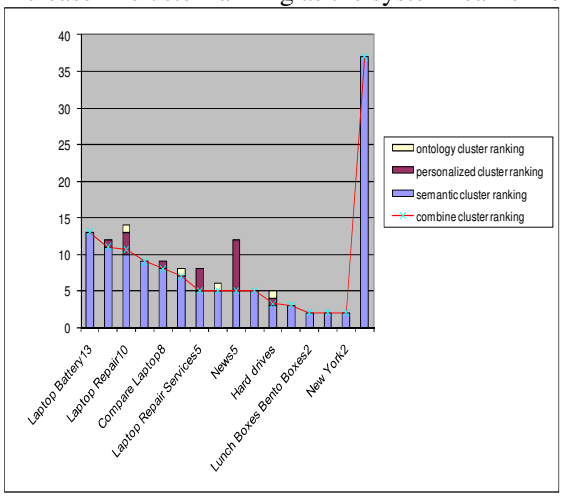


Fig 4: Results showing increasing in cluster ranking depending on user choice

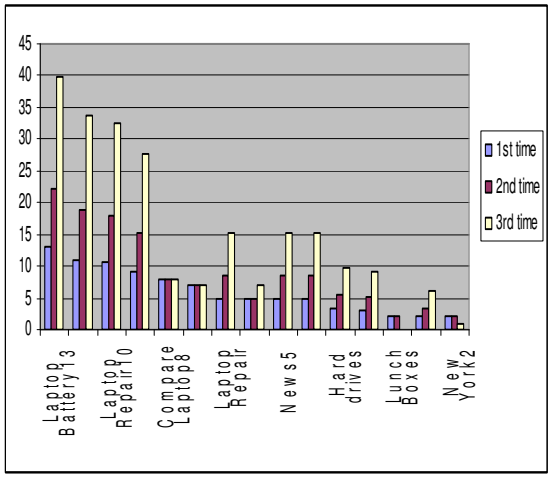


Fig 5:Growth of personalization

## VI. CONCLUSION

We have introduced a web mining tool, a personalized, knowledge-driven cluster based search system that helps the user to find web information based on individual preferences. Analysing the currently

available algorithms, we observed that little emphasis was being placed on the quality of thematic groups' description. The aim of this work is to perform personalized search by recording user profile for users from their browsing pattern and to retrieve more relevant and related documents clusters that are semantically related to the given search query. To achieve this, it is essential to know the meaning and domain of the search query. To understand the semantics of the search query, Ontology is developed. Along with the semantic clusters ranking probability, the ontology ranking and personalized cluster probability is taken into account to decide the final ranking of clusters for a given search query. Personalization using such ontologies and semantic can produce better results as compared to the keyword-based searching.

Our system also shows that, while it is possible to improve the efficiency of search through each of the personalization methods discussed above, they infact work best when operated in conjunction with one another, acting as a checks and balances mechanism. When used in conjunction, the inferences truly become more probable, and lead to dramatically better search results.Effecient information gathering without disturbing the privacy of user can still prove a good way to personalize the search results.

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# HIGH PERFORMANCE COMPUTING AND VIRTUAL NETWORKING IN THE AREA OF BIOMETRICS

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## *ABSTRACT*

*Virtual networking is an important step in the evolution of data networks. The key idea of network virtualization is to build a diversified Internet to support a variety of network services and architectures through a shared substrate. Pattern Recognition is the process of establishing a close match between some new stimulus and previously stored stimulus patterns. This Paper describes the necessity of biometric systems for Network Data and Information Security, Role of virtual LAN's in supporting the error free security system. An Attempt is made to use the finger print of an individual for accessing the secured network. On an experimental basis, a biometric attendance system of staff and students of college is done to test and validate the working of the designed algorithm using Cellular Neural Network. Designing of algorithm using Cellular Neural Network to carry out the front end software, Backend software to implement in the Virtual network and implemented on digital Signal Processor (DSP). Ideal finger implemented on Digital Signal Processor (DSP). Ideal finger print data was considered for analysis without any error.*

**KEYWORDS:** *Biometric, Cellular Neural Network, Digital Signal Processor, Virtual LAN.*

## I. INTRODUCTION

Human finger prints are unique to each person and can be regarded as a sort of signature, certifying the person's identity. Because no two finger-prints are exactly alive, the process of identifying a fingerprint involves comparing the ridges and impressions on one fingerprint to those another. This first involves capturing the likeness of the fingerprint, either through use of a fingerprint scanner (Biometric Reader) which takes the digital picture of a live fingerprint. A virtual LAN is used to connect different Biometric Readers and the Server.

A Practical approach is taken to connect Biometric Reader and Server for the Students and Staff Attendance, The matching of fingerprints is accomplished by using Neural Networks(NN), Cellular Neural Networks(CNN) and the NN and CNN paradigms use repetitive multiplication and Addition (MAC), the Digital Signal Processor Architecture Super Harvard Architecture(SHARK) is ideal for MAC operations.

A High Performance Computing HN36 Biometric machine is taken and It is connected to the Virtual Local Area Network of Internet Protocol Address as Server, we taken Microsoft SQL Server to activate the biometric at the Back End Access to the reports from one computer to another computer in the network that increases performance, security, and the resources required Biometric Devices, Captures the Finger Print and Image will be processed using Cellular Neural Network and Pattern Matching Algorithm with the help of Hash Functions. The analysis of fingerprints for matching purposes generally requires the comparison of several features of the print pattern. In this network, here set of finger prints are captured as training data set in the files. Once the finger print is captured it automatically monitors the files. Where the training data set is stored. These stored files are having large bulk of training data sets. So we are using pattern matching. The pixel value equivalent of the finger prints and these files are stored. Pattern matching is carried out to find out the convergence of the fingerprint.

## II. BIOMETRIC READER

A Biometric Reader HN36 is taken which is portable and having high capacity of 3000 data storage capacity and 80000 transaction storage capacity, This finger print reader can interact with external devices and this readers have all the necessary communication standards which includes RS232, RSS485, TCP/IP and USB.

Further, A real time clock and a graphical LCD of 128/64 assist this Reader to perform more efficiently. It works best in an operating temperature range of 0 to 45 degrees and can withstand humidity levels from 20% to 80%, it equipped with a rechargeable battery which provides un interrupted power back up of about 2 hours, Their high matching speed ensures that they can match 1000 fingerprints in less than 2 seconds which effectively means that they have an identification time of less than 1 second. It is a Standalone connecter but at this practical approach we connected it to the Virtual Local Area Network which is connected with 12 Biometric Readers to the Server. It supports both the finger prints and password for the attendance, it having high speed scratch proof sensor 500 DPI (Digital Processing Image)

A sensor is a device that measures or detects a real-world condition, such as motion, heat or light and converts the condition into an analog or digital representation.

Fig 2.1 HN-36 Biometric Machine

Fig2.2 Fingerprint

## III. VIRTUAL LOCAL AREA NETWORK

The actual or physical LAN may be considered as a group or combination of computers connected by some network device such as hub or switch. It forms a single broadcast domain, that is, if a machine wants to broadcast a message then the message is received by all other machines in the LAN. Now-a-days

LAN can be configured logically with the help of networking device software. With this, k number of machines physically connected to a switch may be grouped into ‘n’ number of logical LANs. This is known as Virtual Local Area Network (VLAN).

As the Strength of students and staff is more in the college and the requirement of the Biometric Readers will be increase year by year, and the computer systems which are in the college will be increased by year by year going for virtual LAN is much better than the LAN. Sometimes it is required to reflect the organizational structure of a college rather than its physical layout, Physical LAN reflects only the physical layout of a college, rather than its logical layout. VLAN only can do this Job. VLAN reduces the migration cost of moving a station from one LAN to another, In a Physical LAN if a station is to move from one place or another keeping it in the same previous LAN, then the System Administrator has to physically reconfigure the wiring of the switch but this is done very easily in VLAN. The network Administrator will have to configure the switch with software without any physical labour. VLAN gives the facility of creating virtual workgroup without affecting the physical layout of the LAN. The members of a workgroup can exchange there views very easily as VLAN creates logical workgroup, broad caste in a group means distribution of message with in a single logical LAN rather than physical LAN. So VLAN provides n number of logical broadcast domain this provides security to the system.

**3.1 Basic VLAN Architecture** VLAN can be implemented in VLAN cable switch, no other special device is required at all. The switch contains built in software which the network administrator has to configure to form the VLAN. He has to form the workgroups give membership to them monitor them, if required reconfigure them.

**3.2 Membership** Different characteristics of Network are used for Including a station in a VLAN.

**3.2.1 Port Number** Port Number of the switch may be used as a membership parameter for example stations attached to port number **1,4,5,8 and 10** are in VLAN 1 stations attached to port number **2, 3,9,16** are in VLAN 2 and so on.., here VLAN 1 Station is of the Clients (Computers ) and VLAN 2 Station is of the DSP(Biometric Readers).

**3.2.2 MAC ADDRESS:** 48 bit MAC address may also be used as a Membership parameter for example stations with MAC Address **AC23-E234 : BC10** And **FEA1 : CC43 : 100 C** may be included in VLAN1 and so on.

**3.2.3 IP ADDRESS:** 32-bit IP Address may also be used for Configuring VLAN for Example stations with IP Address **192.168.1.10** and **192.168.1.14** may be included in VLAN 1, Stations with IP Address **192.168.1.100** and **192.168.1.12** may be included in VLAN2.

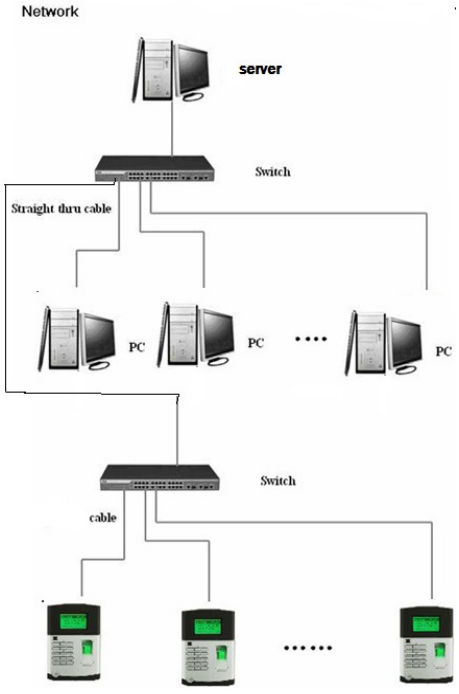


Fig 3.1 Virtual Local Area Network

# IV. SOFTWARE FOR BIOMETRIC READER

Time Tracking Software is a category of computer software that allows its users to record time spent on tasks. It is accounting software used to maintain timesheets. Fingerprint biometric time attendance system and a perfect add-on to current human resource management helping to automate data collection and process timesheets. The Software helps to prepare attendance reports faster for organizations of any size, Improve overall workforce punctuality. Queue up faster with one touch login. By using this system the students and staff of the college can give the attendance 99.9% accurately, No password to remember, no cards to hold, no buddy-punching, just by using users own finger. By using this method we found the management of human resource is improved, and it gives a full overview of workforce time attendance in seconds. This software can generate the reports according to the user's requirements and the reports can also export to MS-Excel.

# V. MICROSOFT SQL SERVER

Microsoft SQL Server is used to activate the biometric at the Back End Access to the reports from one computer to another computer in the network. It is used to Secure information so nobody can manipulate the data except

Appropriate person that is System Administrator and user can export data at LAN or Virtual LAN or can create custom reports or applications (like a web report). In all these scenarios, the best way to perform the installation is in two separate machines: One holding the database (Server), and the other one holding the Punch Clock (Client).

# VI. BLOCK DIAGRAM OF A BIOMETRIC SYSTEM

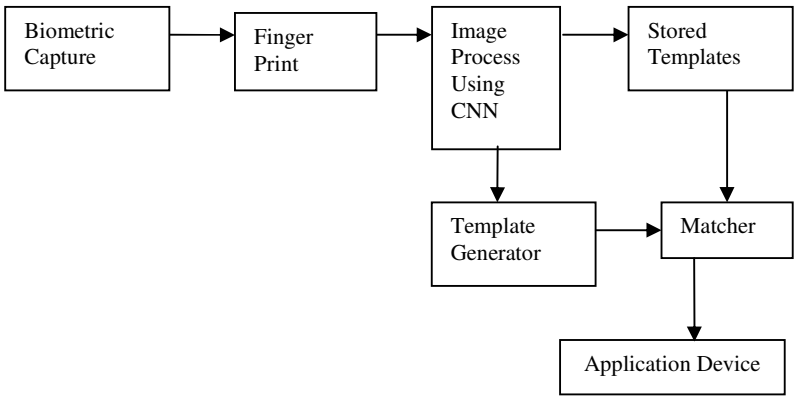


Fig 6.1 Block Diagram of a Biometric System

Biometric Devices, Captures the Finger Print and Image will be processed using Cellular Neural Network, the above block diagram shows the extraction and identification process and it checks the present template matches with the stored template or not.

# VII. CONCEPT OF FINGERPRINT SDK

A fingerprint SDK is a software toolkit that allows the integration of biometric fingerprint recognition into various applications. Typically a Windows-based SDK will utilize either a DLL or ActiveX (COM) control to interface with the integrated application. By referencing these DLL or COM objects, developers are able to utilize the fingerprint functionality from within a desired application.

# VIII. ALGORITHM APPROACH

### 8.1. Methodology

Cellular Neural Network (CNN) is a Data to Information processing paradigm which is inspired by the way of human brain system. Here in our mathematical models for CNN are in differential equations form as a data for information processing has variables which can be represented in differential equation form and this $n^{th}$ order differential equations, which makes processing the proposal MAC method Ideal.

**8.1.1. Algorithm** A standard CNN differential equation is shown in a equation 1, which is a simplify and standard differential equations

$$x_{ij} = -x_{ij} + \sum_{k=-r}^{r} \sum_{l=-r}^{r} a_{kl}\, y_{i+k,j+l} + \sum_{k=-r}^{r} \sum_{l=-r}^{r} b_{kl} u_{i+k,\,j+l} + z$$

Where

$X_{ij}$ is the first derivative of $X_{ij,}$ a and b are the elements of the space invariant template matrices. Solving the standard differential equations, x= (h : w)

Where x = x(t)

$X(0) = x_0$

This can be solved by Standard Numerical Integration Methods. The simplest one is the forward Eulu Formula, which calculates the value of x (t + Δt) from x(t) ,Δt be the time step.

$x(t + \Delta t) = x(t) + \Delta t x(t) = x(t) + \Delta t h(x(t):(w))$

This equation used for calculating the time of CNN dynamics range. So we are finding the group of finger print by using Eulurs Formula of above equation. Every time step is calculated to find the pattern of finger print.

Fig 8.1 Finger Print

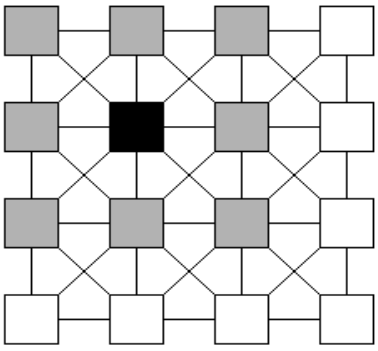

Fig 8.2 Cellular Neural Networks

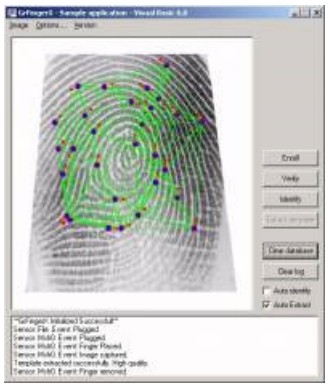

Fig 8.3 Finger Print in Time Track Software

In this figure we have used two dimensionally fully connected CNN with competitive learning method for training. In competitive learning we have used both feed-forward neural network and feedback neural network. so that once finger print is going to find in training dataset.

It will take some synaptic weights which were given in training data set and match with old weights which were given by user new weights. This weights and inputs are calculated in MAC form(matrices multiplication and addition).so that this were calculated by pixels form such as address bus and data bus and it will act as row and column. It is associated by the form of cell of pixels C(6,8),C(4,9) so on. These are the sample training data sets. Every cell is interconnected between cellular neural networks and their neighbor cells are also connected. Actually it is necessary to capture the cells of the training data sets, so if it is required the cell is connected to each other on demanded process. Because if all cells are connected then there is a problem of CNN dynamics range. Then there is only one winner neuron. In the above figure consider an MXN cells arranged in M rows and N columns. We denote the cell on the ith and the jth column as C(i,j),as in figure. Generic processors use von Neumann architecture, where in the data bus and address bus are multiplexed. This hampers the

processing speed for repetitive processes like the one represented in equation 1. However, this type of architecture gives the advantage of storing the program and data on the same memory. But these types of processors fail for MAC type of processing. DSPs are implemented using SHARK where in the data bus and address bus are separate and the stored program and stored data are separate but interlinked. This type of architecture is highly advanced as the prior architecture lacked the facility of interlinking of stored program and stored data on different memory hence making processing relatively slow, when compared to SHARK architecture , but fast when compared to von Neumann architecture as it had different buses for address bus and data bus. Hence SHARK architecture is ideal for repetitive tasks like MAC. The DSP used here for processing i.e.., computing the distances or weights after repetitive feed forward training is of fixed point origin, the software developed for DSP was written in high level language and later converted to assembly level language and finally to machine level language.

## IX. ANALYSIS AND USABILITY

The analysis of fingerprints for matching purposes generally requires the comparison of several features of the print pattern. These include patterns, which are aggregate characteristics of ridges, and minutia points, which are unique features found within the patterns. It is also necessary to know the structure and properties of human skin in order to successfully employ some of the imaging technologies.

In figure 9.1 we show the biometric finger print implemented in capturing the finger of human being. A set of finger prints are captured, which are given access

The fingerprint is composed of various “ridges” and “valleys” which form the basis for the loops, arches, and swirls that one can easily see on his/her fingertip. The ridges and valleys contain different kinds of breaks and discontinuities. These are called “minutiae”, and it is from these “minutiae” that the unique features are located and determined. There are two types of “minutiae”:

- Ridge endings (the location where the ridge actually ends)
- Bifurcations (the location where a single ridge becomes two ridges)

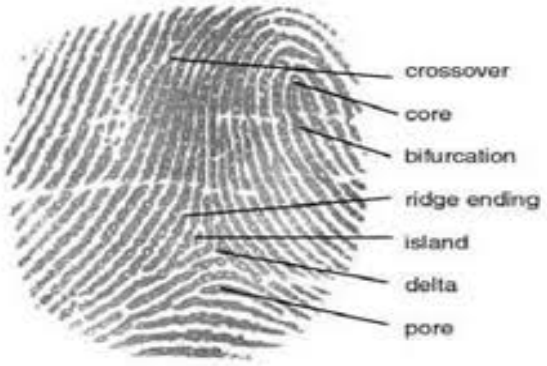


Fig : 9.1 Basic patterns of fingerprint

**Template Creation** Based upon the unique features found in the “minutiae”. The location, position, as well as the type and quality of the “minutiae” are factors taken into consideration in the template creation stage. Each type of fingerprint recognition technology has its own set of algorithms for template creation and matching.

**Template Matching** The system will either attempt to verify or identify a individual, by comparing the enrolled template against the verification template.

**Biometrics growth and advantages** The biometrics is experiencing fast development across the world because

1. Evolutions and rapid expansion of Information technology and web which claims for secure access control and secure data transfer.
2. Terrorism has put a lot of threat to Governments, which has raised the demand for accurate identification of individuals.

The three basic patterns of fingerprint ridges are the arch, loop, and whorl. An arch is a pattern where the ridges enter from one side of the finger, rise in the center forming an arc, and then exit the other side of the finger. The loop is a pattern where the ridges enter from one side of a finger, form a curve, and tend to exit from the same side they enter. In the whorl pattern, ridges form circularly around a central point on the finger. Scientists have found that family members often share the same general fingerprint patterns, leading to the belief that these patterns are inherited.

Table :1 Figure print data by Class

| period | Finger Print Type | | |
|---|---|---|---|
| | Arch | Loop | Whorl |
| 1 | 6 | 9 | 8 |
| 2 | 6 | 7 | 6 |
| 3 | 5 | 6 | 7 |
| 4 | 10 | 5 | 10 |
| 5 | 9 | 6 | 7 |

## X. COMPUTATIONAL BASIS

In this network, here set of finger prints are captured as training data set in the files. Once the finger print is captured it automatically monitors the files. Where the training data set is stored.

These stored files are having large bulk of training data sets. So we are using pattern matching. The pixel value equivalent of the finger prints and these files are stored. Pattern matching is carried out to find out the convergence of the fingerprint. Maximum convergence will occur for a non pattern matching algorithm. During pattern matching after training of CNN, changes in the trained CNN.Pixel value equivalent of the pattern when compared yield minor changes in the actual value which is trained in CNN. Higher number of learning epochs in training process also leads to redundancy in trained CNN. Comparison of pixel data, which is repetitive in nature, can increase the speed of processing as MAC(matrices of multiplication and addition) architecture specializes in increasing the speed of identical data types. Pixel values, if exceeding a certain limit, can be averaged using pixel averaging technique to remove the redundancy in values. The repetition of pixel values calculation is absolute as it decreases the speed of recognition. Hence, pixel averaging technique processing is improved in terms of speed of convergence and improvement in processing ability. Equivalent pixel values are stored and processed with freedom of analysis for testing after the training process is complete, inherent noise addition is possible during storage and retrieval of data. To overcome this problem, reduction algorithms can be used. However, in this work, data without any noise (i.e.. ideal data) is considered for evaluation of results. Trials can be carried out for noise inclusion by changing the pixel values in the stored file. These will, however, be unpredictable noise inclusion and cannot be incorporated to any actual noise. Actual noise data can be a cut in the thumb, peeling of skin etc…, of the authentic user. In pattern matching the trained data is stored in form of patterns. So in this paper we propose “finger printing” to preprocess the input string. So we are taking three basic patterns of finger print ridges are the archs, loops, and whorl. Suppose we are trying to find a pattern string ‘p’ in a long document D. hash the pattern ‘p’ into say a 16bit value. Now run through the file, hashing each set of |p| consecutive characters into a 16bit value. If we ever get a match for a pattern, we can check to see if it corresponds an actual pattern match (in the case we want to double check and not report any false matches!) otherwise we can just move on. We can use more than 16-bits, too; we would like to use enough bits so, that we will obtain few false matches.this scheme is efficient as long as hashing is efficient. Of course hashing can be very expensive operation, so in order for this approach to work, we need to be able to hash quickly on average. In fact, a simple hashing technique allows us to do so in constant time for operation! The easiest way to picture the process is to think of the file as a sequence of digits, and the pattern as a number. Then we move a pointer in the file one character at a time, seeing if the next |P| digits give us a number equal to the

number corresponding to the pattern. Each time we read a character in the file, the number we are looking at changes is a natural way; the left most digit 'a' is removed and the new right most bit 'b' is inserted. Hence ,we update an old number 'N' and obtain a new number N□ by computing

$$N□ = 10.( N – 10^{|P|-1}.a)+b$$

When dealing with a string, we will be reading characters (bytes) instead of numbers. Also, we will not want to keep the whole pattern as a number. If the pattern is large then the corresponding number may be too large to do effective comparison. Instead, we hash all the numbers down into say 16 bits, by reducing they modulo some appropriate time p. We then do all the mathematics (multiplication, addition) |P|

$$N□= [10.( N – 10^{|P|-1}.a)+b] \bmod P$$

All operations mod P can be made quite efficient, so, each new hash value takes only constant time to compute! The idea is that the hash of the pattern creates an almost unique identifier of the pattern-like a finger print. If we ever find two fingers prints that match, we have a good reason to expect that they must come in the same pattern. Ofcourse, unlike real finger prints, hashing based finger prints do not actually uniquely identify a pattern, we will need to check for false matches, but since false matches should be rare, the algorithm is very efficient.

A natural approach is to choose the prime p randomly. This way, nobody can set up a bad pattern and document in advance, since they are not sure what prime we will choose.

P=17935

P=251

**P mod p =114**

**6386179357342…….**

**63861 mod p = 107**

**38617 mod p = 214**

**86179 mod p = 86**

**61793 mod p = 47**

**17935 mod p = 114**

**79357 mod p = 41**

**93573 mod p = 201**

**35734 mod p = 92**

**57342 mod p = 114**

This pattern P is a five digit number. Note successive calculations take constant time:

38617|P|=(63861 mod p) - (60000 mod p)).10+7 mod p. also note that a false matches are possible (but unlikely): 57432=17935 mod p.

Let us make this a bit more rigorous Π(x) represents the number of primes that are less than or equal to x. it will be helpful to use the following fact.

**Fact:** $\frac{x}{\ln x} \le \prod(x) \le 1.26\frac{x}{\ln x}$

Consider any point in the algorithm, where the pattern and document do not match. if our pattern has length |P|, then at that point we are comparing two numbers that are each less than 10^|P|.what is the probability that a random prime divides this difference? That is, what is the probability that for random prime we choose, the two numbers corresponding to the pattern and the current |P| digits in the document are equal modulo P.

First note that there are at most ---------- distinct primes that divide the differences, since the difference is at most 10^|P|(in absolute value),an each distant prime divisor is at least 2.hence,if we choose our prime randomly from all primes upto Z. the probability we have a false match approach is at most

$$\frac{\log_2}{\prod}\frac{10^{|p|}}{(Z)}$$

Now, the probability that we have a false match anywhere is at most |D| times the probability that we have a false match in any single location, by the union bound. Hence the probability that we have a false match anywhere is at most

$$\frac{|D|\log_2 10^{|p|}}{\prod(Z)}$$

## XI. EXPERIMENTAL RESULTS AND ANALYSIS

Regardless of dip water of wet finger, and dry finger, and dip mud, and oil, and dust, dirty finger are can validation by, can adaptation any bad of natural environment and weather. In the Experiment we got 97.9 % success rate.

## XII. CONCLUSION

It can be concluded that convergence is faster and more accurate using the above technique. Fingerprint sensors are best for devices such as cell phones, USB flash drives, notebook computers and other applications where price, size, cost and low power are key requirements. Fingerprint biometric systems are also used for law enforcement, background searches to screen job applicants, healthcare and welfare. It is also the best method for the attendance systems in colleges, universities and schools. It is also used in Factories, Industries and Companies for the Employee attendance and for the Pay roll preparation based on the attendance. The software also used for the taxation and other deduction methods used in established employee payroll system. DSP used for implementing the CNN gives a higher degree of convergence. Increase in the number of iterations gives better convergence and accurate results in matching the biometric fingerprints. And this technique is entirely new and different from the conventional fingerprint technique.

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# STATUS AND ROLE OF ICT IN EDUCATIONAL INSTITUTION TO BUILD DIGITAL SOCIETY IN BANGLADESH: PERSPECTIVE OF A DIVISIONAL CITY, KHULNA

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## *ABSTRACT*

*Education is one of the main keys to economic development and improvements in human welfare. As global competition grows sharper, education becomes an important source of competitive advantage and appears to be one of the key determinants of standardization of life. Information and communication technology (ICT) is playing a central role in the development of modern economies and societies. As the world is going through the technological revolution, adoption of new technologies in the education system is the most important. This has profound implications for education, both because ICT can facilitate new forms of learning and because it has become important for young people to master ICT in preparation for adult life. The use of ICT has the potential to enhance the real world experiences, the educational institutions should emphasize on the use of ICT for both administrative and academic efficiency. This study investigates current status of ICT in educational institutions and educational organization related activities and provides comprehensive recommendations to build a digital society in Bangladesh in the near future.*

## *KEYWORDS*

*Competitive advantage, ICT, Technological revolution, digital society*

## I. INTRODUCTION

The UNESCO uses the term ICTs to describe: "…the tools and the processes to access, retrieve, store, organize, manipulate, produce, present and exchange information by electronic and other automated means. These include hardware, software and telecommunications in the forms of personal computers, scanners, digital cameras, phones, faxes, modems, CD and DVD players and recorders, digitized video, radio and TV programs, database programs and multimedia programs" (UNESCO Bangkok, 2003).

Any kind of technology can be understood as a tool or technique for extending human capacity. In this sense, ICTs extend our human capacity to perceive, understand and communicate. The mobile phone enables us to speak from wherever we are to others thousands of kilometres away; television permits us to see what is happening on the other side of the planet almost as it happens; and the Web supports immediate access to, and exchange of, information, opinions and shared interests. In the field of formal education, ICTs are increasingly deployed as tools to extend the learner's capacity to perceive, understand and communicate, as seen in the increase in online learning programs and the use of the computer as a learning support tool in the classroom. Although universities were certainly leaders in engineering the Internet and interoperable computer systems to connect researchers for e-mail and data exchange, the use of ICTs for education and training has lagged behind other sectors in society.

In order to best use these technologies in education, new pedagogies and learning assessment methods may, and probably will, be required. In this rapidly advancing field, it is worth reviewing the history, current uses and trends in ICTs that will further influence how education practices may be changed in

future. Educators are continuing to develop new applications and online resources to support learning objectives in all disciplines.

Skilled manpower is an enormous foundation of a country to compete with competitive world and the teachers and institutions are the builders of them. Some universities of Bangladesh are trying to develop a better shape in their educational system by proper utilization of ICTs for learning system. Better policies and standards always support new learning environments, which are very much needed to build up the digital society in Bangladesh. The focus of the research is the level of ICT that the educational institutions (secondary, madrasha, college and university) are using now and what should be the future strategy to cope with upcoming opportunities to build the nation in digital way.

## II. LITERATURE REVIEW

The history of the use of ICTs in education is relatively short. Before 1979, computers existed primarily in tertiary level educational institutions. Then, in the eighties, microcomputers began to be distributed to schools, and teachers began to grapple with the question of how to use computing for education rather than simply educating about computing. Starting from the mid-nineties, the use of ICTs in schools rapidly expanded in developed nations through curriculum support, networking, the professional development of teachers and software improvements [1]. A growing number of researchers and educators began to develop applications that used hypertext, multimedia and networking to build cognitivist and constructivist learning environments aimed at improving learning [2], [3], [4]. However, these applications were initially found to be ineffective in attaining better results as compared to learning outcomes achieved through traditional pedagogies and assessed against traditional metrics. This finding may be largely influenced by teachers' and learners' lack of familiarity with ICTs as well as the inappropriateness of the traditional metrics in and of themselves [5].

In recent years, bandwidth has greatly increased and user familiarity with the Web and ICTs in general has evolved, contributing to an evolution of the Web. Policy based on the prevailing ideas about ICTs has also been a major driver shaping the adoption of ICTs in education. For example, the late 1980s and early 1990s were dominated by rhetoric surrounding the idea of the transition from the Industrial Society to the Information Society, where managing, generating and sharing information would be key to national economies maintaining the cutting edge in an increasingly globalized market [6]. This idea promoted the concept that the education system would need to create a "learning culture," which would prepare citizens for lifelong learning in an information society; which is the prime necessity for building digital society.

The accelerated adoption and use of Information and Communication Technology (ICT) has resulted in the globalization of information and knowledge resources [7]. That is why it has become very important to adopt the technology for the betterment of the education system. ICT is a term used to describe a range of equipment (hardware: personal computers, scanners and digital cameras) and computer programs (software: database programs and multimedia programs), and the telecommunications infrastructures (phones, faxes, modems, video conferencing equipment and web cameras) that allow us to access, retrieve, store, organize, manipulate, present, send material and communicate locally, nationally and globally through digital media [8]. ICT are a diverse set of technological tools and resources used to communicate, create, disseminate, store, and manage information [9].

Bangladesh, located in South Asia is one of the overpopulated, underdeveloped and technologically backward countries in the world but the higher academic institutions of a country are pioneers in adopting and using Information and Communication Technologies [10]. Universities around the world are developing digital strategies to support education in the 21st century. The focus of these strategies is to enable countries to realize their economic, social and cultural capital; to keep pace with rising expectations and technological advancements; to develop creative, thinking people who can solve problems in new ways and within multi-dimensional learning environments [8]. The higher academic institutions of a country are pioneers in adopting and using ICT [10]. Moreover, efforts to connect educational organizations to the ICT are being driven by societal pressure [9].

Effective higher education plays a central role in promoting productivity, innovation, entrepreneurship, gender mainstreaming and overall socio-cultural advancement [11]. Moreover, ICT

revolution imposes particular challenges on education systems in Bangladesh [13]. Now private universities are making praiseworthy contributions in development of ICT in Bangladesh [12]. Around 40% of the private universities of Bangladesh are using ICT at a large extent for administrative purposes and around 35% of the universities are using ICT for teaching at a large extent and 55% of the universities use ICT at a moderate level [19].

Higher education institutions are becoming more reliant upon ICT as a means of providing enhanced learning and teaching. The university administration and academic support services particularly require the use of ICT to provide effective and excellent services [14]. The ICT tool must be central to and through the various levels of university administration. ICT also can enrich the teaching methods, which ultimately facilitates the learning process [15]. ICT is a medium for teaching and learning [16]. This refers ICT as a tool for teaching and learning itself, the medium through which teachers can teach and learners can learn. There are two reasons for which ICT in teaching is important (i) first is, as ICT is everywhere that is why it should present in the university education also so that the students can use enter in their future working life with the enriched knowledge of ICT and (ii) second is, ICT can improve the effectiveness of university education [17]. ICT can solve problems pertaining to quality, equity, and access to higher education and can also promote resource sharing and therefore improve efficiency and productivity while at the same time open up access to global resource of knowledge and information [18].

## III. BACKGROUND

The government is looking at implementing ICT initiatives to revolutionize the education system. With the successful implementation of ICT in the education system, the government can look at a greater participation of the country in the global information society. It is hoped that ICT will impact the access, cost-effectiveness and quality of the education system too. The increasing digital divide needs to be addressed by the uniform and well-administered implementation of ICT. The demographical picture that shows a relatively lower participation of the female population in the ICT education process also needs to be revised through initiatives and programs.

Bangladesh has made significant progress, especially with regard to increasing access and gender equity, both at the primary and secondary levels. Gross enrolment rates at the primary level rose from 90% in the late 1990s to 98% in 2003, while the enrolment rates at the secondary level rose to 44%. Gender parity in access to primary and secondary education has also been achieved to an extent. These achievements are particularly spectacular when compared to countries in the South Asia region and other countries at similar levels of per capita income. Some of the key education indicators for the country are shown in the Table 1.

The ICT industry in Bangladesh has been making steady progress with rapid growth in mobile telephony and Internet usage. The Ministry of Science Information and Communication Technology is tasked with the responsibility of providing the policy framework and institutional mechanism for the development of a robust ICT sector in the country. Further, the Bangladesh Computer Council (BCC), set up by the Ministry in 1990, is an autonomous body responsible for encouraging and providing support for ICT-related activities in Bangladesh. Some of the key ICT-related indicators for the country are shown in Table 2.

Table 1. Key Education Indicators of - Bangladesh.

| Education parameter | | Value | Year |
|---|---|---|---|
| Adult literacy rate | Male<br>Female | 53.9<br>31.8 | 2000–2007<br>2000–2007 |
| Youth literacy rate | Male<br>Female | 71<br>73 | 2000–2007<br>2000–2007 |
| Gross enrollment ratio (%): Primary education | Male<br>Female | 101<br>105 | 2000–2007<br>2000-2007 |
| Gross enrollment ratio (%): Secondary education | Male<br>Female | 43<br>45 | 2000–2007<br>2000-2007 |
| Expenditure on education (% of GDP) | | 2.7 | 2003–2006 |

Source: www.unicef.org; www.cia.gov

Table 2. ICT Indicators - Bangladesh

| ICT parameters | Value | Year |
|---|---|---|
| Internet users (per 100) | 0.3 | 2008 |
| Internet subscribers (per 100) | 0.1 | 2008 |
| Broadband subscribers (per 100) | 0.03 | 2008 |
| Mobile coverage (%) | 90 | 2007 |
| Mobile subscribers (per 100) | 21.7 | 2007 |
| Personal computers (per 100) | 2.42 | 2006–2007 |
| Internet affordability (US $/month) | 22.1 | 2007 |
| Mobile affordability (US$/month) | 2.6 | 2007 |
| Radio subscribers (per 1000) | 42.6 | |
| Households with TV (%) | 22.9 | |

Source: www.itu.int; www.mdgs.un.org; World Development Indicators Database; www.cia.gov

## IV. ICT POLICY FRAMEWORK

The Government of Bangladesh in an effort to harness the power of ICT formulated its National ICT Policy in year 2002. A revised National ICT Policy was passed in 2009. The National ICT Policy 2009 has incorporated all the components of the National ICT Policy 2002 in a more structured manner. Some of the specific policy statements relevant to education are stated below:

- Assess skills of ICT professionals and meet gaps with targeted training programs to overcome the short-term skills shortage in the ICT industry and adopt continuing education and professional skills assessment and enhancement programs.
- Encourage closer collaboration between academia and industry to align curriculum with market needs.
- Establish an ICT Center of Excellence with necessary long-term funding to teach and conduct research in advanced ICTs.
- Enhance the quality and reach of education at all levels with a special focus on Mathematics, Science, and English.
- Boost use of ICT tools in all levels of education, including ECDP, mass literacy, and lifelong learning.
- Ensure access to education and research for people with disabilities and special needs using ICT tools.
- Establish multimedia institutes.
- Initiate diploma and trade courses to enable ICT capacity building for teachers. Teacher training institutes to be empowered with ICT capacity to meet the challenges.
- Create reliable and accessible national databases.
- Promote the use of ICT for the purpose of training in the public sector.
- Initiate development of a sizable resource of globally competitive ICT professionals in order to meet local and global market requirements.
- Administer the successful enactment of laws and regulations that conform to World Trade Organization stipulations to allow for consistent ICT growth.
- Promote distance education, set up institutes and infrastructure for e-learning training programs.
- Develop seamless telecommunication network for the unhindered implementation of ICT policy.
- Ensure public access to information through setting up of kiosks. Encourage the participation of private sector for ICT implementation.

- Work toward setting up a Ministry of ICT, by merging MOSICT and MOPT. The "Science" part from MOSICT can be transferred to MoE and be renamed as the Ministry of Education and Science. BTRC should be brought under the Ministry of ICT.
- Create an e-Education Cell for coordinating and mainstreaming ICTs in education system.

## V. OBJECTIVES

Now a day ICT is the essential parts for participatory teaching system, the objective of the study is to find out the status of ICT use in the educational institutions (secondary school, madrasha, college, university). Specifically the objectives are to identify how the institutions are using ICT for both administrative and academic purposes to increase their efficiency and taking pioneering role to build the digital society in Bangladesh by producing ICT concerned people.

## VI. METHODOLOGY

Questionnaires offer a method of conducting a survey where all respondents are asked exactly the same questions in the same circumstance. In this research, questionnaire survey was conducted to identify the status of use of ICT in the educational institutions of Bangladesh. Structured questionnaire were formulated in order to identify different uses of ICT and the efficiency of using the ICT. Total of 25 educational institutions (5 university/same level institute, 5 colleges, 5 polytechnics, 5 secondary schools and 5 madrashas) were surveyed in Khulna city, Bangladesh. The respondents were employees, students and teachers of those institutions who were representing their institutions and the number of respondents were 4450 (130 employees, 370 teachers, 3950 students). The sampling technique was random sampling. Finally, the study considered both quantitative and qualitative analyses. The statistical package used to conduct the various analyses is the SPSS.

## VII. RESULTS AND DISCUSSION

- We find that only 44% of the institutions have their own web page and 56% of them have no web page. But no secondary school and madrasha have their own web pages (shown in Table 3).

Table 3. Presence of Web in the institution

| Institution Type | Presence of Website (%) | |
|---|---|---|
| | Yes | No |
| University/University Equivalent | 80 | 20 |
| College | 60 | 40 |
| Polytechnic Institute | 80 | 20 |
| Secondary School | 0 | 100 |
| Madrasha | 0 | 100 |
| Total | 44 | 56 |

- We find that 51.60% of the teachers have ICT knowledge and only 36.43% of the teachers have their e-mail address. But the higher education institutions are forward in this regard but mid-level institutions (secondary school, madrasha) are lagging in the regards. Detailed statistics has been provided in Figure 1.

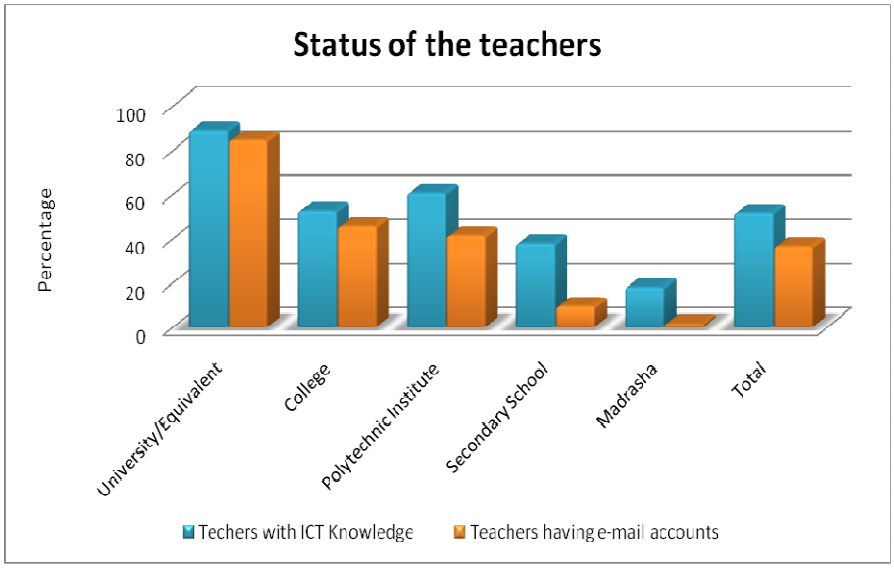


Figure 1. Status of the teachers

- We find that only 39.37% of the supporting staffs have basic ICT knowledge. The staffs of higher education and polytechnic institutions are somehow satisfactory level but colleges, secondary school and madrasha staffs are not in satisfactory level (presented in Table 4).

Table 4. Status of the staffs

| **Institution Type** | **Staff with ICT Knowledge (%)** |
|---|---|
| University/University Equivalent | 55.87 |
| College | 37.64 |
| Polytechnic Institute | 64.00 |
| Secondary School | 27.33 |
| Madrasha | 12.00 |
| Total | 39.37 |

- We also find that among the students 52.97% have basic ICT knowledge, 21.67% have e-mail address, 28.19% have personal computer and 25.72% are used to internet. The students of the higher education institutions are in satisfactory level in all the regards but all other students are not in satisfactory level especially in owing e-mail, personal computer and use of internet as provided in Figure 2.

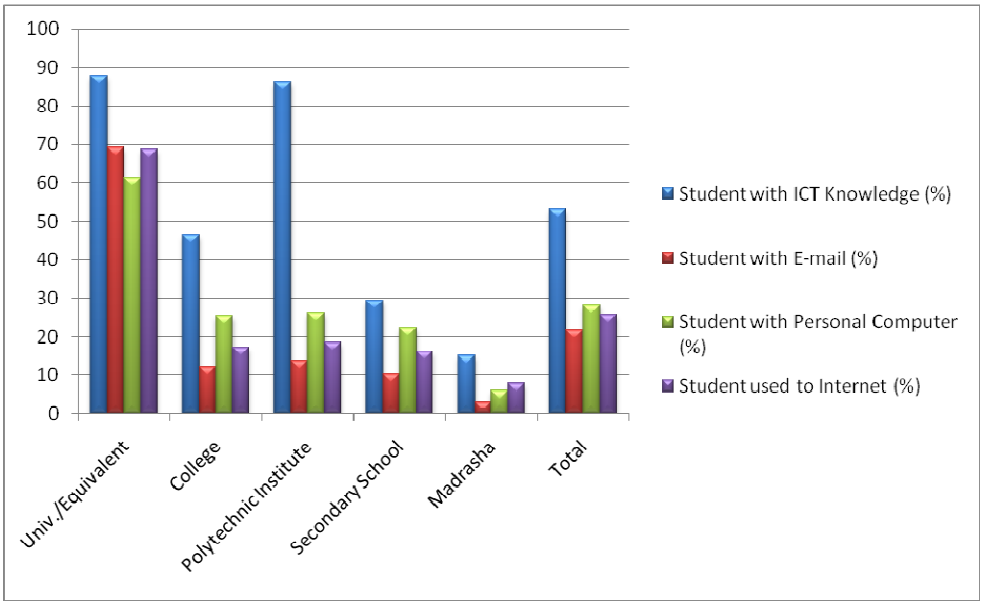


Figure 2. Status of the students

- We find that 50.83% of the class/department/discipline have basic computer course in their syllabus. Only polytechnic institutes have compulsory computer curse in all departments but the same factor for secondary and madrasha level are not satisfactory (shown in Figure 3).

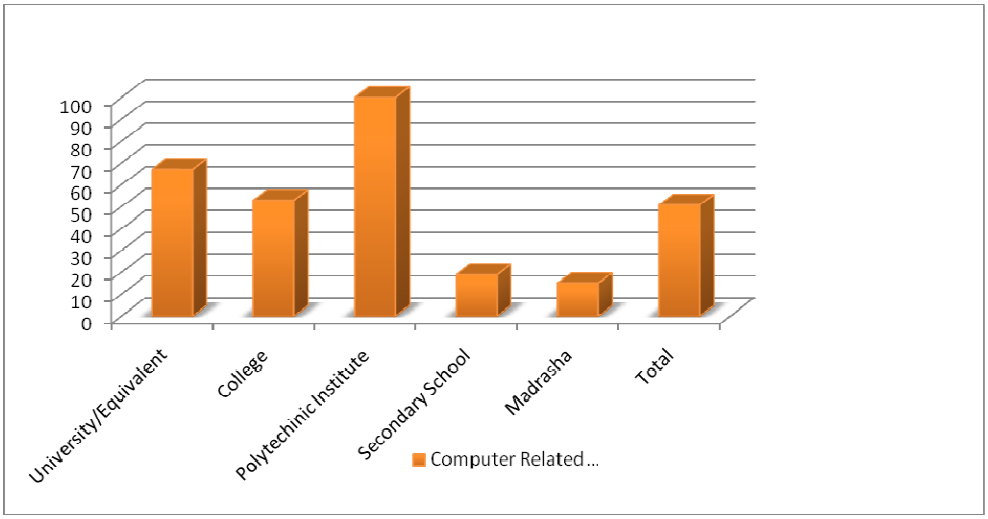


Figure 3. Status of computer related courses

- It has been found that only 32% of the institutions have their own LAN and 60% of the institutions have internet facility. But most of the institutions have internet facilities not for the vast people or students (shown in Table 5).

Table 5. Status of LAN and internet

| **Institution Type** | **Availability of LAN (%)** | | **Availability of internet (%)** | |
|---|---|---|---|---|
| | Yes | No | Yes | No |
| University/University | 80 | 20 | 80 | 20 |

| | | | | |
|---|---|---|---|---|
| Equivalent | | | | |
| College | 20 | 80 | 100 | 0 |
| Polytechnic Institute | 60 | 40 | 40 | 60 |
| Secondary School | 0 | 100 | 60 | 40 |
| Madrasha | 0 | 100 | 20 | 80 |
| Total | 32 | 68 | 60 | 40 |

- Our findings implies that, 48% of the institutions use multimedia in with their educational program and only 15.67% of the teachers use the multimedia in the class or laboratory as presented in Table 6.

Table 6. Status of multimedia use in education

| **Institution Type** | **Multimedia Used in Education (%)** | | **Teacher used to Multimedia (%)** |
|---|---|---|---|
| | Yes | No | |
| University/University Equivalent | 100 | 0 | 62.97 |
| College | 40 | 60 | 2.13 |
| Polytechnic Institute | 80 | 20 | 11.59 |
| Secondary School | 20 | 80 | 1.67 |
| Madrasha | 0 | 100 | 0.00 |
| Total | 48 | 52 | 15.67 |

- It has been noticed that no institutions have digital library and only 16% of the institutions have student database and 8% of the institutions have automated accounts. So administrative duties can be hazardous in the institutions. The statistics has been conveyed in Table 7.

Table 7. Status of multimedia use in education

| **Institution Type** | **Digital Library (%)** | | **Student Database (%)** | | **Automated Accounts (%)** | |
|---|---|---|---|---|---|---|
| | Yes | No | Yes | No | Yes | No |
| University/University Equivalent | 0 | 100 | 20 | 80 | 20 | 80 |
| College | 0 | 100 | 0 | 100 | 20 | 80 |
| Polytechnic Institute | 0 | 100 | 60 | 40 | 0 | 100 |
| Secondary School | 0 | 100 | 0 | 100 | 0 | 100 |
| Madrasha | 0 | 100 | 0 | 100 | 0 | 100 |
| Total | 0 | 100 | 16 | 84 | 8 | 92 |

## VIII. CONCLUSIONS AND RECOMMENDATIONS

Undoubtedly, ICTs are potentially a useful tool both for managing education and teaching. Application of ICT in managing educational institutions should be encouraged, as should use by instructors to gain access to educational materials. By teaching computer skills to youngsters, they may influence inward investment for the future society as well. ICTs are most likely to be cost-effective when used to reach very large numbers of students; when used for research; and when used by administrators irrespective of time and place.

This study reveals that the level of use and infrastructure of ICTs is not highly satisfactory in all forms of educational institutions to meet the current demands of ICT. But their efforts in this regards will help to build a digital society in Bangladesh in the near future as well.

Some of the recommendations that can be followed in the educational institutions to build digital society in Bangladesh:

- Training for all levels of teachers, assistants who are involving in educational institutions. Universities -> Colleges/Polytechnics ->School/Madrasha and from school and madrashas, general people can get trained. They are also modified themselves in this way.
- Establishment of lab facilities and internet availabilities for all the students, teachers and assistants.
- Basic ICT course should be compulsory in all form of educations.
- Personnel with basic ICT knowledge should be appointed in all form of educational institutions.
- Use of ICT and multimedia in the education makes it interesting and fruitful
- Website of the institution should be compulsory along with regular updates.
- Central registration system for the students should be implemented mandatorily.
- Use of student database, automated account in the institutions for faster administration should be employed.
- Facilitating electronic professional research journal and periodicals access to foster the level of technology savvy mind of the people and more importantly featuring the educators and students to access the emerging arena of knowledge.
- Making an open platform to share the academic and other relevant thoughts among vast people which would dimensionalize the incepted concepts.
- Establishment of digital libraries or information repository may also be done by the educational institutions which may provide invaluable materials to the researchers, educators and students as well as other interested people.
- In disseminating ICT and new technologies which may improve the overall life style of the mass people may be acquainted through conferences, workshops and other technical gatherings arranged by the educational institutions in collaboration with other agencies

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# PIECEWISE VECTOR QUANTIZATION APPROXIMATION FOR EFFICIENT SIMILARITY ANALYSIS OF TIME SERIES IN DATA MINING

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***ABSTRACT***

*Efficiently searching for similarities among time series and discovering interesting patterns is an important and non-trivial problem with applications in many domains. The high dimensionality of the data makes the analysis very challenging. To solve this problem, many dimensionality reduction methods have been proposed. PCA (Piecewise Constant Approximation) and its variant have been shown efficient in time series indexing and similarity retrieval. However, in certain applications, too many false alarms introduced by the approximation may reduce the overall performance dramatically. In this paper, we introduce a new piecewise dimensionality reduction technique that is based on Vector Quantization. The new technique, PVQA (Piecewise Vector Quantized Approximation), partitions each sequence into equi-length segments and uses vector quantization to represent each segment by the closest (based on a distance metric) code word from a codebook of key-sequences. The efficiency of calculations is improved due to the significantly lower dimensionality of the new representation. We demonstrate the utility and efficiency of the proposed technique on real and simulated datasets. By exploiting prior knowledge about the data, the proposed technique generally outperforms PCA and its variants in similarity searches.*

***KEYWORDS:*** *Time series, dimensionality reduction, data mining.*

## I. INTRODUCTION

The problem of retrieving similar time sequences may be stated as follows: Given a query $q$, a database $S$: $S_1, S_2, \ldots, S_N$, a distance measure $D$ and a threshold $\varepsilon$, find the sequences $R$ in $S$ that are within distance $\varepsilon$ from $q$. More precisely, $R = \{S_i \in S | D(q, S_i) \leq \varepsilon\}$. In a variant of this problem, no threshold is given, instead the closest neighbours of the query series are to be found. To compare two given time series, a suitable measure of similarity should be given. The Euclidean distance is most often used. In many situations, the high dimensionality of time series makes the distance calculation very inefficient. Promising techniques include those based on dimensionality reduction and multidimensional indexing. An efficient approach is based on piecewise constant approximation (PCA) or piecewise aggregate approximation (PAA). Yi and Faloutsos [7] and Keogh et al [2] proposed to divide each sequence into $k$ segments of equal length and to use the average value of each segment as a coordinate of a $k$-dimensional feature vector. Recently, a symbolic PAA was also introduced [3].In this paper, we introduce a new method to efficiently reduce the dimensionality of time series. Our work is motivated by the observation that the mean value that is being used to approximate each equilength segment in PCA and PAA is the best one can do for a piecewise approximation if there is no prior knowledge about the data or a method needs to be independent of the data. The method proposed here is also based on segmentation of a sequence but extends PCA by allowing a more flexible approximation of each segment, using ideas from data compression and in particular the vector quantization technique, effectively representing a long time series with a symbolic representation of much lower dimensionality. In addition to being comparable to the other

popular methods in terms of complexity, the proposed approach demonstrates advantages of closer approximation of original time series and higher accuracy in time series matching.

## II. METHODOLOGY

The proposed approach, Piecewise Vector Quantized Approximation (PVQA), partitions a sequence into equi-length segments and uses vector quantization (VQ) to represent each segment with the closest code word from a codebook. VQ is widely used in signal compression and coding; it is a lossy compression method based on the principle of block coding [1]. During a training phase, a codebook $C = \{c_1, c_2, \ldots, c_s\}$ of size an arbitrary integer $s$ ($s \geq 2$) is created. A time series $X = x_1, x_2, \ldots, x_n$ of length $n$ is represented with a vector $X' = x'_1, x'_2, \ldots, x'_w$ of length $w$ ($w << n$) by being segmented into $w$ equal size segments .The $i$-th element of $X'$ is: $x'_i = \arg_k \min(D(SEG_i, c_k); k=1,\ldots,s)$ where $SEG_i$ is the $i$-th segment in $X$, $D$ is the distance measure (e.g., Euclidean distance), and $c_k$ is the $k$-th code word in $C$.

### *2.1 Codebook Generation*

Each time series in a training set T is partitioned into a number of segments of a fixed length $l$ and each segment forms a sample that is used to generate the codebook. In order to get the key-sequences (code words) and build the codebook we apply the Generalized Lloyd Algorithm (GLA) [4].

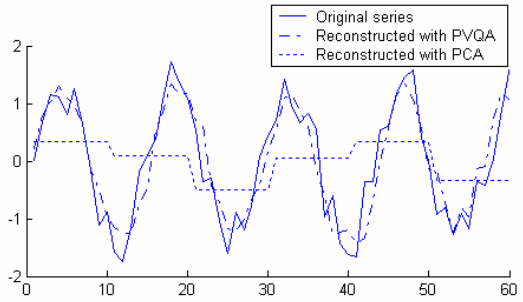



*Figure (1). A time series and its reconstructions*

### *2.2 Data Encoding*

In the process of encoding, every series is decomposed into sub sequences of length $l$ (same as the length of the code words). For each subsequence the closest entry $c_k$ in the codebook is found and its index $k$ is stored. So, the new representation of a time series is a vector of indices to code words. Figure 1 shows an original time series and its reconstruction given a certain codebook by concatenating the corresponding code words. For comparison, we also show the reconstruction using PCA. PVQA has more flexibility than PCA to approximate the original time series arbitrarily close through the adjustment of not only the number of segments, but also the size of the codebook.

### *2.3 Distance Measures*

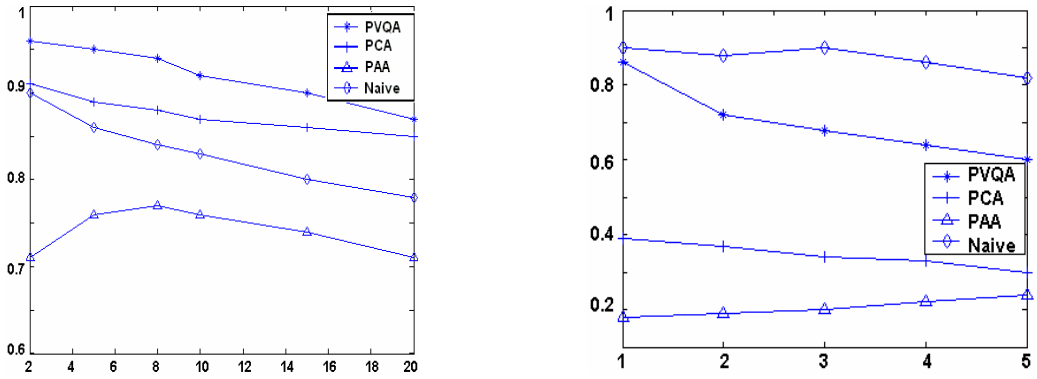
Using PVQA, a time series is represented as $X' = x'_1, x'_2, \ldots x'_w$, and correspondingly a query is represented as $Q' = q'_1, q'_2, \ldots q'_w$. Each $x'_i$ and $q'_i$ ( $1 \leq i \leq w$ ) is an index corresponding to a code word in the codebook. Since the approximate representation for a time series $X$ ($Q$) is the concatenation of all the code words corresponding to $x'_i$ ($q'_i$), we can sum up the distance between each pair of $x'_i$ and $q'_i$ and get a rough distance between the two series:

$$RoughDist(X, Q) = \sqrt{\sum_{i=1}^{w} (D(x'_i, q'_i))^2}$$

The distance between each pair of code words can be pre-calculated and stored. The space complexity of the distance matrix is $O(s^2)$ and the time complexity of computing the rough distance between two time series is $O(w)$.

## III. EXPERIMENTS

To evaluate the proposed method, we performed experiments in best match searching, i.e., given a query sequence, find the best $k$ matches in a database. The evaluation metric we used was the percentage of the results that fall in the same class as the query. We compared the efficiency and accuracy of our method to that of two other piecewise dimensionality reduction techniques: PCA and symbolic PAA. For fairness, we used the same reduced dimensionality for all methods. The accuracy of the Euclidean distance on the original time series (Naïve approach) was also calculated. Using the *tightness of approximation* defined as Rough Dist(X,Q) / D(X,Q), we ran experiments on several synthetic and real datasets and chose $w$=6 and $s$=16 as a nice trade-off between accuracy and efficiency.




(a) ( b)

Figure (2).Matching results on SYNDATA (a) and GENE (b)

In order to assure that the experimental results are reliable, we applied 5-fold cross-validation and the datasets were pre-processed with Z-normalization. In Figure 2 we show the experimental results on a synthetic dataset, SYNDATA [6], and on a real dataset, GENE [5]. SYNDATA contains 527 examples from 38 attributes of control charts. For this dataset, we used $k$ = 2, 5, 8, 10, 15, 20. GENE is a subset of the water treatment dataset gene expression data from the UCI Machine Learning repository form Stanford University [8]. Each series has the expression values of 1375 genes. For GENE, we used $k$= 1, 2, 3, 4, 5.

## IV. RESULT AND DISCUSSION

As shown in Figure 2(a) and 2(b), the matching accuracy of PVQA is close or even better than that of Euclidean distance and is much better than the results obtained with PCA or PAA. With PVQA, while the outline of the original time series is kept, noise that may affect the calculation of similarities between different time series is removed and this leads to the improved accuracy.

## V. CONCLUSIONS

We have proposed a novel symbolic representation of time series that effectively reduces the dimensionality improving the efficiency of calculations in similarity searches. The proposed PVQA approach is a natural extension of the piecewise constant approximation schemes proposed earlier. By exploiting prior knowledge about the data and allowing the use of a very tight approximation of the Euclidean distance we were able to improve performance in time series similarity analysis over previously proposed methods. Moreover, the proposed representation is symbolic and potentially allows the application of text-based retrieval techniques into the similarity analysis of time series.

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# DESIGN AND MODELING OF TRAVELLING WAVE ELECTRODE ON ELECTROABSORPTION MODULATOR BASED ON ASYMMETRIC INTRA-STEP-BARRIER COUPLED DOUBLE STRAINED QUANTUM WELLS ACTIVE LAYER

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***ABSTRACT***

*In this paper, a travelling wave electroabsorption modulators (TWEAMs) based on asymmetric intra-step-barrier coupled double strained quantum wells (AICD-SQW) active layer is designed and analyzed at 1.55 μm for the first time. The AICD-SQW structure has advantages such as very low insertion loss, zero chirp, large Stark shift and high extinction ratio in comparison with the intra-step quantum well (IQW) structure. For this purpose, the influence of the electrode width and ground metal separation on their transmission line microwave properties (microwave index, microwave loss, and characteristic impedance) and modulation bandwidth are analyzed.*

***KEYWORDS:*** *travelling wave electroabsorption modulator, aicd-sqw, microwave properties, modulation bandwidth.*

## I. INTRODUCTION

Electroabsorption modulators (EAMs) are advantageous external modulators in high-speed optical communication systems due to low chirp, small size, high modulation efficiency, low driving voltage, high extinction ratio, wide modulation bandwidth and the capability to be integrated with other semiconductor devices. Improving the operation by overcoming the trade-off between bandwidth and device length, EAMs with travelling wave electrodes have been documented to be a good candidate [1-10]. Fig. 1 shows the principle of operation for a travelling-wave electroabsorption modulator. In a travelling-wave electrode configuration, the microwave signal is applied from one end of the optical waveguide and it co-propagates with the optical signal. At the output end of the waveguide, the microwave signal is terminated with a matching load such that there is little reflection from this end. Therefore, in a TW-EAM, the electrode is designed as a transmission line to distribute the capacitance over the entire device length [5]. This can increase the modulation efficiency while maintaining a large bandwidth. The bandwidth and the device length are only limited by the microwave loss at high frequencies, which includes propagation loss and source port reflection loss and the velocity mismatch between the optical signal and the microwave signal. Another limiting factor is the increased optical loss with a longer device, which is related to the optical signal-to-noise ratio of the modulated signal [3]. Due to waveguide dispersion, high frequency components will experience smaller characteristic impedance and hence higher reflection loss when launched from a 50 Ω driver [8-12]. In previous articles, we have proposed an asymmetric intra-step-barrier coupled double strained quantum well (AICD-SQW) structure based on the InGaAlAs material system that has advantages such as large Stark shift, very low insertion loss, zero chirp, high extinction ratio, and higher figures of merit in comparison with the IQW structure [13-17].

In this article, we have designed and analyzed a TWEAM based on asymmetric intra-step-barrier coupled double strained quantum wells at 1.55 μm optical wavelength for the first time. Design of TWEAM includes the reduction of electrical losses, velocity mismatch, and impedance mismatch. It

is therefore important to have control over parameters such as electrical propagation constant and characteristic impedance of the TWEAM transmission line electrode. Here we focus on the influence of the TWEAM transmission line electrode width and ground metal separation on their transmission line microwave properties such as microwave index, microwave loss, characteristic impedance and modulation bandwidth.

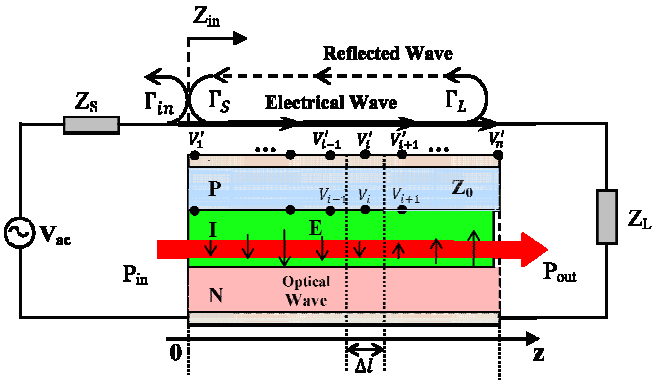



Figure 1. Principle of operation of TWEAM transmission line [14-15]

## II. ACTIVE REGION OF TWEAM

A schematic illustration of the compositions and the thicknesses of the active region layers of TWEAM based on AICD-SQW structure are shown in Fig. 2 [13]. The figure also illustrates the direction of the applied electric field *F*.

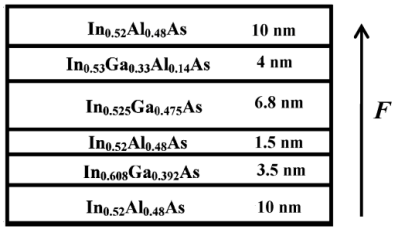



Figure. 2 Schematic of layers for AICD-SQW structure, Direction of applied electric field *F* is indicated as well

The undoped AICD-SQW structure has $In_{0.52}Al_{0.48}As$ barriers, which are lattice matched to the InP substrate, as well as one lattice-matched $In_{0.53}Ga_{0.33}Al_{0.14}As$ intra-step-barrier. The $In_{0.525}Ga_{0.475}As$ wide well is under 0.05% of tensile strain, and the $In_{0.608}Ga_{0.392}As$ narrow well is under 0.52% of compressive strain. The thickness of each of the two external barriers is 10 nm, while the thickness of the middle barrier is 1.5 nm. The thicknesses of the wide well, the narrow well and the intra-step-barrier are 6.8 nm, 3.5 nm and 4 nm, respectively. The middle barrier layer and strain amount of wells cause the electron and heavy hole wave functions are distributed dominantly in the wide and narrow wells, respectively. As a result, the insertion loss significantly decreases at zero electric field [13, 14].

## III. FREQUENCY RESPONSE OF TRAVELLING WAVE ELECTROABSORPTION MODULATOR

TWEAMs are devices to modulate light waves corresponding to travelling electric fields along the electrode consisting of a transmission line. Because the absorption coefficient of TWEAMs is dependent on the electric voltage, the modulation of optical wave occurs by the absorption change due

to modulated electric signals. Fig. 3 shows the circuit model for a unit length of transmission line of TWEAM based on AICD-SQW active layer.

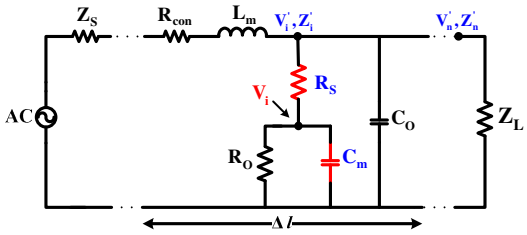



Figure 3. Circuit model for a unit length of transmission line of the TWEAM based on AICD-SQW active layer [14]

The small signal frequency response for TWEAM can be obtained as follows [11]:

$$\left|P_{ac}\right|^2 = \left| \sum_{i=1}^{n} \left( V_i e^{j\frac{\omega}{c_0} n_{o_eff} (i-1)\Delta l} \Delta l \right) \right|^2 \qquad (1)$$

where $V_i$ is the modulating voltage in $i$ section. The voltage on the transmission line is the superposition of forward and backward travelling voltage waves that arise from reflections at the source and the load terminal, respectively. Eq. (1) can be developed analytically as follows [3]:

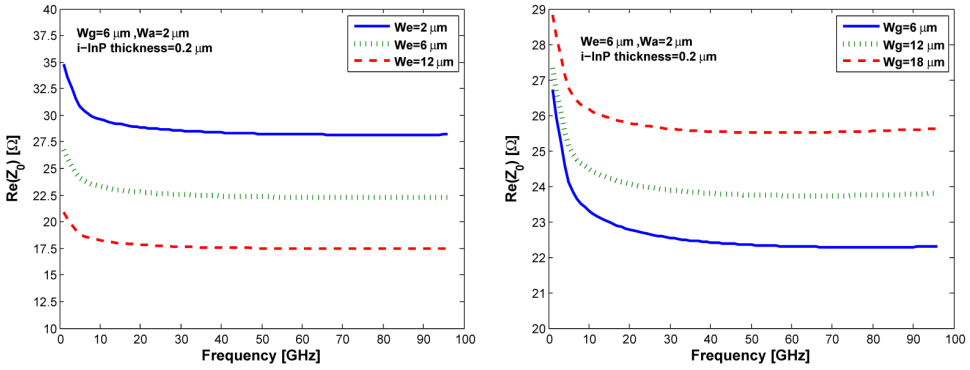
$$\left|P_{ac}\right|^2 = \left| \frac{1}{\left(\frac{R_s}{R_o} + 1 + j\omega R_s C_m\right)} \cdot \frac{V_0 Z_0 / (Z_s + Z_0)}{\left(1 - \Gamma_s \Gamma_L e^{-2\gamma_\mu L}\right)} \cdot \left[ \frac{1 - e^{(-\gamma_\mu + j\beta_o)L}}{\gamma_\mu - j\beta_o} - \frac{\Gamma_L e^{-2\gamma_\mu L}\left(1 - e^{(\gamma_\mu + j\beta_o)L}\right)}{\gamma_\mu + j\beta_o} \right] \right|^2 \qquad (2)$$

where $V_0$ is the forward microwave voltage in the source transmission line, $Z_0$ is the characteristic impedance and $\gamma_\mu$ is the propagation constant of modulator transmission line. $\Gamma_S$ and $\Gamma_L$ are the modulator reflection coefficients at the source and load ports, respectively. $\omega$ is the microwave frequency, and $\gamma_\mu = \alpha_\mu + j\beta_\mu$, where $\alpha_\mu$ is the microwave loss and $\beta_\mu = \omega/v_\mu$, is the wavenumber associated with the microwave phase velocity $v_\mu$ and $\beta_o = (\omega/c_0)\, n_{o_eff}$ is the wavenumber associated with the optical phase velocity. The calculation of the small signal modulation response requires the knowledge of the optical index $n_{o_eff}$ and the circuit model elements. The circuit elements can easily be extracted from the TWEAM transmission line microwave properties $Z_0$ (characteristic impedance) and $\gamma_\mu$ (propagation constant) [6], which are obtained via full-wave calculations of the given geometry.

## IV. RESULTS AND DISCUSSION

In this section, we investigate the effects of the TWEAM transmission line electrode width ($w_e$) and ground metal separation ($w_g$) on their transmission line microwave properties such as microwave index $n_\mu$, microwave attenuation $\alpha_\mu$, characteristic impedance $Z_0$ and modulation bandwidth. In this study, the thickness of the active layer is taken as 0.2064 μm. In order to improve the junction capacitance, we use a small intrinsic buffer layer, i-InP on top of the active layer with thickness of 0.2 μm. The width of the active layer, $w_a$ is considered as 2 μm and modeling is performed for a wavelength of 1.55 μm. In the numerical modeling, the thicknesses of p- and n-mesa are taken as 1.7 μm and 1.5 μm, respectively. The corresponding geometry values and typical material data are in [14]. For our case study, we use data for the InP/InGaAsP material system according to published devices [13, 14]. Furthermore, the effective optical index, $n_{o_eff}$ defines the optical speed, which should be known in the analysis of a travelling wave modulator. The calculated effective optical index using full-vectorial finite difference method is 3.512 [15].

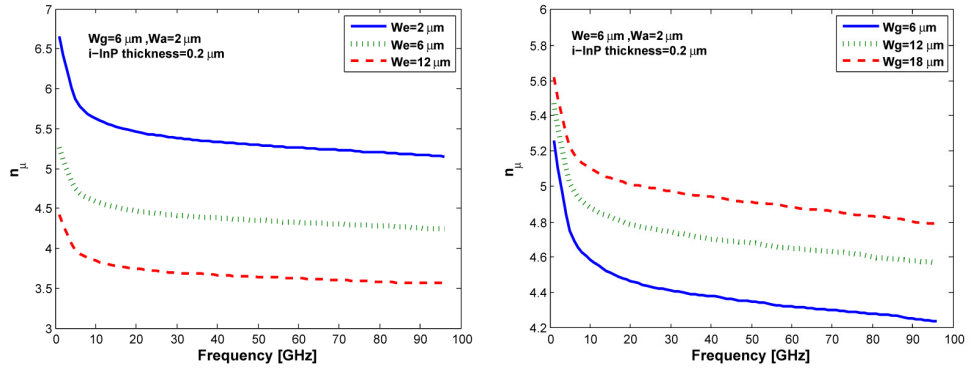
Fig. 4 shows the calculated real part of characteristic impedance Re($Z_0$) over frequency for different combinations of $w_e$ and $w_g$. The real part of characteristic impedance draws near a constant level for frequencies above 10 GHz. This value is usually mentioned to as the modulator impedance. It can be observed that as the electrode width is increased, the real part of characteristic impedance value is reduced (Fig. 4a), but this value increases when the ground metal separation ($w_g$) is increased (Fig. 4b). With the change of the width of electrode, the circuit model elements $R_{con}$, $L_m$, and $C_o$ are affected. Therefore, by widening the electrode, ohmic losses are reduced and the inductance $L_m$, decreases since the magnetic field path length changes. Furthermore, the area for the outer parasitic capacitance increases resulting in higher $C_o$. The junction capacitance $C_m$ is not affected by changing the electrode width.




(a) (b)

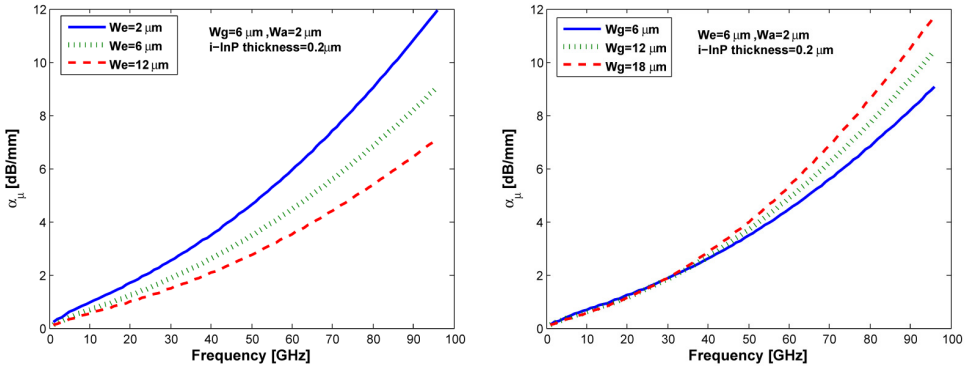
Figure 4. Calculated real part of characteristic impedance Re($Z_0$) versus frequency for different (a) electrode widths $w_e$ and (b) ground metal separations $w_g$

Fig. 5 shows the calculated microwave index over frequency for different combinations of $w_e$ and $w_g$. As the electrode width increases, the microwave index value decreases (Fig. 5a). The main effect of electrode width can be depicted best by considering an ideal transmission line without any losses. In this case microwave index is obtained as $n_\mu=c_0(L_mC_m)^{½}$. Increasing the width of electrode only decreases the inductance $L_m$ in waveguide and decreases thereby the microwave index. Therefore, the microwave velocity increases. On the other hand, the microwave index value increases when the ground metal separation ($w_g$) is increased (Fig. 5b). Fig. 6 shows the calculated microwave loss over frequency for different combinations of $w_e$ and $w_g$. It can be observed that as the electrode width is increased, the microwave loss value is reduced, but this value increases when the ground metal separations $w_g$ is increased.




(a) (b)

Figure 5. Calculated microwave index versus frequency for different (a) electrode widths $w_e$ and (b) ground metal separations $w_g$




(a) (b)

Figure 6. Calculated microwave loss versus frequency versus frequency for different (a) electrode widths $w_e$ and (b) ground metal separations $w_g$

In the design of the TWEAM, the microwave parameters $n_\mu$, $\alpha_\mu$ and $Z_0$ play important roles in determining the bandwidth of the modulator. The bandwidth of a high-speed modulator with a travelling-wave electrode is primarily limited by the velocity mismatch between the optical signal and the modulating microwave signal related to their modal indexes, $n_{o_eff}$ and $n_\mu$. For a high speed modulator, when phase velocity matching is achieved, the next limiting factor is the total microwave propagation losses $\alpha_\mu$. A design challenge for the TWEAM is a low characteristic impedance of 25 Ohm or below in the active waveguide, which causes reflections when driven by a 50 Ohm source and limits the modulation bandwidth. Therefore, low impedance terminations in the range of 12 to 35 Ohm are required to obtain the maximum bandwidth.

Fig. 7 shows the calculated frequency response of TWEAM based on AICD-SQW with different lengths and $Z_L$=25 Ω. The overall waveguide loss and velocity mismatch increase as the device length increases. The microwave loss and velocity mismatch reflect the decrease in optical modulation, as shown in the plot. The 3dB bandwidth for TWEAM based on AICD-SQW is about 83 GHz for 100 μm, 44 GHz for 200 μm and 22 GHz for 400 μm waveguide length, respectively.

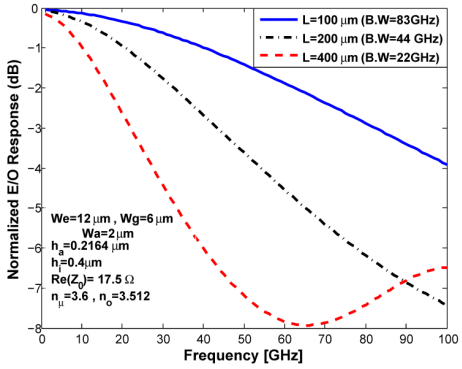



Figure 7. Frequency response for TWEAM based on AICD-SQW with different waveguide lengths

## V. CONCLUSIONS

A travelling wave electroabsorption modulators (TWEAMs) based on asymmetric intra-step-barrier coupled double strained quantum wells (AICD-SQW) active layer was designed and analyzed at 1.55 μm for the first time. The AICD-SQW structure has advantages such as very low insertion loss, zero chirp, large Stark shift and high extinction ratio in comparison with the intra-step quantum well (IQW) structure. For this purpose, the influence of the electrode width and ground metal separation on their transmission line microwave properties (microwave index, microwave loss, and characteristic impedance) and modulation bandwidth were analyzed. The 3dB bandwidth for TWEAM based on

AICD-SQW is about 83 GHz for 100 μm, 44 GHz for 200 μm and 22 GHz for 400 μm waveguide length, respectively.

## ACKNOWLEDGEMENTS

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# POWER SYSTEM STABILITY IMPROVEMENT USING FACTS WITH EXPERT SYSTEMS

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## *ABSTRACT*

*This paper presents exhaustive review of various concept of voltage instability, main causes of voltage instability, classification of voltage stability, dynamic and static voltage stability analysis techniques, modeling, shortcomings, in power systems environments. It also reviews various current techniques/methods for analysis of voltage stability in power systems through all over world. This paper presents a comprehensive review on the research and developments in the power system stability enhancement using FACTS damping controllers. Several technical issues related to FACTS installations have been highlighted and performance comparison of different FACTS controllers has been discussed. In addition, some of the utility experience, real-world installations, and semiconductor technology development have been reviewed and summarized. Applications the EPS equipped with a decentralized modular secondary voltage and reactive power control based on artificial neural network (ANN) is presented. The ANNs were trained on optimal power flows (OPF).*

***KEYWORDS*:** *Stability, FACTS, Artificial neural networks, power system security voltage profile*

## I. INTRODUCTION

Since the development of interconnection of large electric power systems, there have been spontaneous system oscillations at very low frequencies in order of 0.2–3.0 Hz. Once started, they would continue for a long period of time. In some cases, they continue to grow causing system separation due to the lack of damping of the mechanical modes [1; 2]. In the past three decades, power system stabilizers (PSSs) have been extensively used to increase the system damping for low frequency oscillations. The power utilities worldwide are currently implementing PSSs as effective excitation controllers to enhance the system stability [1–12]. However, there have been problems experienced with PSSs over the years of operation. Some of these were due to the limited capability of PSS, in damping only local and not inter area modes of oscillations. In addition, PSSs can cause great variations in the voltage profile under severe disturbances and they may even result in leading power factor operation and losing system stability [13]. This situation has necessitated a review of the traditional power system concepts and practices to achieve a larger stability margin, greater operating flexibility, and better utilization of existing power systems.

Flexible AC transmission systems (FACTS) have gained a great interest during the last few years, due to recent advances in power electronics. FACTS devices have been mainly used for solving various power system steady state control problems such as voltage regulation, power flow control, and transfer capability enhancement. As supplementary functions, damping the inter area modes and enhancing power system stability using FACTS controllers have been extensively studied and investigated. Generally, it is not cost-effective to install FACTS devices for the sole purpose of power system stability enhancement. In this work, the current status of power system stability enhancement using FACTS controllers was discussed and reviewed. This paper is organized as follows. The development and research interest of FACTS is presented in Section 2. Section 3 discusses the potential of the first generation of FACTS devices to enhance the low frequency stability while the potential of the second generation is discussed in Section 4. Section 5 highlights some important issues in FACTS installations such as location, feedback signals, coordination among different control schemes, and performance comparison.

# II. FACTS DEVICES

## 2.1. Overview:

In the late 1980s, the Electric Power Research Institute (EPRI) formulated the vision of the Flexible AC Transmission Systems (FACTS) in which various power-electronics based controllers regulate power flow and transmission voltage and mitigate dynamic disturbances. Generally, the main objectives of FACTS are to increase the useable transmission capacity of lines and control power flow over designated transmission routes. Hingorani and Gyugyi [5] and Hingorani [6; 8] proposed the concept of FACTS. Edris *et al.* [18] proposed terms and definitions for different FACTS controllers. There are two generations for realization of power electronics-based FACTS controllers: the first generation employs conventional thyristor-switched capacitors and reactors, and quadrature tap-changing transformers, the second generation employs gate turn-off (GTO) thyristor-switched converters as voltage source converters (VSCs). The first generation has resulted in the Static Var Compensator (SVC), the Thyristor- Controlled Series Capacitor (TCSC), and the Thyristor-Controlled Phase Shifter (TCPS) [10; 11]. The second generation has produced the Static Synchronous Compensator (STATCOM), the Static Synchronous Series Compensator (SSSC), the Unified Power Flow Controller (UPFC), and the Interline Power Flow Controller (IPFC) [12–15]. The two groups of FACTS controllers have distinctly different operating and performance characteristics. The thyristor-controlled group employs capacitor and reactor banks with fast solid-state switches in traditional shunt or series circuit arrangements. The thyristor switches control the on and off periods of the fixed capacitor and reactor banks and thereby realize a variable reactive impedance. Except for losses, they cannot exchange real power with the system. The voltage source converter (VSC) type FACTS controller group employs self-commutated DC to AC converters, using GTO thyristors, which can internally generate capacitive and inductive reactive power for transmission line compensation, without the use of capacitor or reactor banks. The converter with energy storage device can also exchange real power with the system, in addition to the independently controllable reactive power. The VSC can be used uniformly to control transmission line voltage, impedance, and angle by providing reactive shunt compensation, series compensation, and phase shifting, or to control directly the real and reactive power flow in the line [15]. In the paper, a framework of a new SVQC concept that could be applied to Slovenian power system is envisioned. The Slovenian power system has a peak load of 1700 *MW* and comprises some 30 generators. They operate decomposed in separate generating companies, which could besides energy offer the power system ancillary services as well. Deregulation in the Slovenian power system requires the power producing companies to reconsider their options in the market. In the decomposed power system regarding generators, it would be of advantage to conceive a secondary voltage and reactive power control system adapted to their organization structure. The paper addresses an extreme decomposition of the secondary voltage control system adapted to the above goals. The SQVC-s should be attached to the generator or to the generator-transformer block and adapt the reference voltage for the primary excitation controller to the power system requirements and limitations. That way, the generating companies would obtain a powerful tool to enter the ancillary services market regarding the power system voltage support and reactive power. Especially independent power producers could benefit greatly from the possibility of local control of their voltage and reactive power.

# III. CLASSIFICATION OF FACTS CONTROLLERS

**Coordination Techniques**

A. by Placement of FACTS Controllers in Power Systems References [3]-[5], [14], classify three broad categories such as a sensitivity based methods, optimization based method, and artificial intelligence based techniques for placement of FACTS controllers from different operating conditions viewpoint in multi-machine power systems.

**1) Sensitivity Based Methods:**

There are various sensitivity based methods such as a modal or Eigen-value analysis, and index method. An Eigen value analysis approach has been addressed for modeling and simulation of SVC and TCSC to study their limits on maximum loadability point in [11], [25]. A new methodology

has been addressed for the solution of voltage stability when a contingency has occurred, using coordinated control of FACTS devices located in different areas of a power system. An analysis of the initial conditions to determine the voltage stability margins and a contingency analysis to determine the critical nodes and the voltage variations are conducted. The response is carried out by the coordination of multiple type FACTS controllers, which compensate the reactive power, improving the voltage stability margin of the critical modes. An Eigen value analysis approach has been addressed for the problem of the most effective selection of generating units to be equipped with excitation system stabilizers in multi-machine power systems which exhibit dynamic instability and poor damping of several inter machine modes of oscillations. A new coordination synthesis method using as an Eigen value sensitivity analysis and linear programming has been addressed for simultaneous able to select the generators to which the PSS can be effectively applied and to synthesize the adequate transfer function of the PSSs for these generators. In An Eigen value sensitivity based analysis approach has been addressed for control coordination of series and shunt FACTS controllers in a multi-machine power system for series and shunt FACTS controllers considered are SVC, TCSC and SVC-TCSC combination. An Eigen value sensitivity based analysis approach has been addressed for design and coordinate multiple stabilizers in order to enhance the electro-mechanical transient behavior of power systems. An Eigen-value sensitivity based analysis approach has been addressed for the evaluation and interpretation of Eigen-value sensitivity, in the context of the analysis and control of oscillatory stability in multi-machine power systems. A modal analysis reduction technique has been suggested. A frequency response technique has been used for coordinated design of under-excitation limiters and power system stabilizers (PSS) in power system for enhance the electromechanical damping of power system oscillations. A root locus technique has been proposed for design of power system stabilizers (PSS) for damping out tie-line power oscillations in power system to enhance the damping of power system oscillations for different combinations of power system stabilizers parameters. A projective control method has been addressed for coordinated control of two FACTS devices such as TCSC and Thyristor Controlled Phase Angle Regulator (TCPAR) for damping inter-area oscillations to enhance the power transfers and damping of power system oscillations. A problem of interest in the power industry is the mitigation of power system oscillations. These oscillations are related to the dynamics of system power transfer and often exhibit poor damping, with utilities increasing power exchange over a fixed network, the use of new and existing equipment in the transmission system for damping these oscillations is being considered in several literatures. A non-linear technique has been proposed for robust nonlinear coordinated excitation and SVC control for power systems for enhance the transient stability of the power systems. A new method has been proposed for the design of power system controllers aimed at damping out electro-mechanical oscillations used for applied to the design of both PSS for synchronous generators and supplementary signals associated to other damping sources. Voltage collapse problems in power systems have been a permanent concern for the industry, as several major blackouts throughout the world have been directly associated to this phenomenon, e. g., Belgium 1982, WSCC July 1996, etc. Many analysis methodologies have been proposed and are currently used for the study of this problem, as recently reported in several literatures These problems are solved in literature, Lie et al. presented a linear optimal controller for the designed to implement multiple variable series compensators in transmission networks of inter-connected power system is utilized to damp inter-area oscillations and enhance power system damping. The coordinated power flow control should address the following points such as elimination of interaction between FACTS controllers, ensuring system stability of the control process, security transmission system for both pre and post fault, and achieving optimal and economic power flow. A new method has been suggested for the potential application of coordinated secondary voltage control by multiple FACTS voltage controllers in eliminating voltage violations in power system contingencies in order to achieve more efficient voltage regulation in a power system. The coordinated secondary voltage control is assigned to the SVCs and Static Compensators (STATCOM) in order to eliminate voltage violations in power system contingencies. Use of this power component as the dynamic variables reduces the degree of non-linearity of the VSC model in comparison with the conventional VSC model that uses d-q current components as variables. Furthermore, since wave forms of power components are independent of the selected q-d coordinates, the proposed control is more robust to the conventionally un-modeled dynamics such as dynamic of the VSC phase locked loop system. A new methodology has been

proposed for decentralized optimal power flow control for overlapping area in power systems for the enhancement of the system security. The controllers considered for coordination are voltage regulators, PSS, speed governors, main and auxiliary controllers of HVDC converters, and main and auxiliary controllers of SVC. A new methodology has been proposed for designing a coordinated controller for a synchronous generator excitation and SVC in power system is to extend the operational margin of stability, whilst satisfying control requirements by introducing an integrated multi-variable controller to control both the generator exciter and the firing angle of the thyristor controlled reactor of TCR-FC compensators, an Eigen value analysis technique is used for coordinated control of PSS and FACTS controllers to enhance damping of power system oscillations in multi-machine power system. A sensitivity based analysis approach is used to find out an inter coupling between a variation of set points of different FACTS devices and a volume of load shedding with a variation of active power flow in transmission lines. A systematic procedure for the synthesis of a Supplementary Damping Controller (SDC) for Static VAR Compensator (SVC) for a wide range of operating conditions is used for testing in multi-machine power systems to enhance the damping of the inter-area oscillations, providing robust stability and good performance characteristics both in frequency domain and time domain. Yue and Shlueter et al. presented a multiple bifurcation phenomena for three kinds of μ -synthesis robust controls are designed such as μ -synthesis power system stabilizer (MPSS), μ -synthesis SVC control (MSVC), and a mixed MPSS/MSVC control. A bifurcation subsystem based methodology has been proposed for μ - synthesis power system stabilizers design in a two-area power system. The secure operation of power systems requires the application of robust controllers, such as Power System Stabilizers (PSS), to provide sufficient damping at all credible operating conditions. Recently, many researchers have investigated the use of robust control techniques including H-infinity optimization and μ -synthesis techniques for developing advanced and automated procedures for power system damping controller design. A several control design techniques such as the classical phase compensation approach, the μ –synthesis. A design method that explicitly considers both the coordination and the robustness issues has been proposed for coordinated design of power system stabilizers and supplementary control of FACTS devices to enhance the robustness of the control scheme for drastic changes in the operating condition. This method is based on the formulation and solution of an augmented equation. A projective control principle based on Eigen value analysis has been presented for coordinated control design of supplementary damping controller of HVDC and SVC in power system to enhance the damping of power system oscillations.

**2) Optimization Based Methods:**

This section reviews the optimal placement of FACTS controllers based on various optimization techniques such as a linear and quadratic programming, non-linear optimization programming, integer and mixed integer optimization programming, and dynamic optimization programming. A non-linear optimization programming techniques has been proposed for optimal network placement of SVC controller and a Benders Decomposition technique has been used for these solutions. A mixed integer optimization programming algorithm has been proposed for allocation of FACTS controllers in power system for security enhancement against voltage collapse and corrective controls, where the control effects by the devices to be installed are evaluated together with the other controls such as load shedding in contingencies to compute an optimal VAR planning, a mixed integer non-linear optimization programming algorithm is used for determine the type, optimal number, optimal location of the TCSC for loadability and voltage stability enhancement in deregulated electricity markets. A mixed integer optimization programming algorithm has been used for optimal location of TCSC in a power system . Chang and Huang et al. showed that a hybrid optimization programming algorithm for optimal placement of SVC for voltage stability reinforcement.

**3) Artificial Intelligence Based Techniques:**

This section reviews the optimal placement of FACTS controllers based on various Artificial Intelligence based techniques such as a Genetic Algorithm (GA), Expert System (ES), Artificial Neural Network (ANN), Tabu Search Optimization (TSO), Ant Colony Optimization (ACO) algorithm, Simulated Annealing (SA) approach, Particle Swarm Optimization (PSO) algorithm and

Fuzzy Logic based approach. A genetic algorithm has been addressed for optimal location of phase shifters in the French network to reduce the flows in heavily loaded lines, resulting in an increased loadability of the network and a reduced cost of production [48]. A genetic algorithm has been addressed for optimal location of multiple type FACTS controllers in a power system. The optimization are performed on three parameters; the location of the devices, their types and their values. The system loadability is applied as measure of power system performance. Four different kinds of FACTS controllers are used as models for steady state studies: TCSC, TCPST, Thyristor Controlled Voltage Regulator (TCVR) and SVC in order to minimizing the overall system cost, which comprises of generation cost and investment cost of FACTS controllers [17]. A stochastic searching algorithm called as genetic algorithm has been proposed for optimal placement of static VAR compensator for enhancing voltage stability in [18]. Reference [19], genetic algorithm (GA) and particle swarm optimization (PSO) has been proposed for optimal location and parameter setting of UPFC for enhancing power system security under single contingencies. The VAR planning problem involves the determination of location and sizes of new compensators considering contingencies and voltage collapse problems in a power system. The Genetic Algorithm (GA) and PSO techniques for optimal location and parameter setting of TCSC to improve the power transfer capability, reduce active power losses, improve stabilities of the power network, and decrease the cost of power production and to fulfill the other control requirements by controlling the power flow in multi-machine power system network [27]. In [28], a Particle Swarm Optimization (PSO) technique has been addressed for optimal location of FACTS controllers such as TCSC, SVC, and UPFC considering system loadability and cost of installation. The ACS methodology is coupled with a conventional distribution system load flow algorithm and adapted to solve the primary distribution system planning problem. A Graph Search Algorithm has been addressed for optimal placement of fixed and switched capacitors on radial distribution systems to reduce power and energy losses, increases the available capacity of the feeders, and improves the feeder voltage profile [29]. In [30], the theory of the normal forms of algorithm has been addressed for the SVC allocation in multi-machine power system for power system voltage stability enhancement. Luna and Maldonado et al. has been addressed a new methodology is based on the evolutionary strategies algorithm known as Evolution Strategies (ES) for optimally locating FACTS controllers in a power system for maximizes the system loadability while keeping the power system operating within appropriate security limits [31]. In [32], a knowledge and algorithm based approach is used to VAR planning in a transmission system. The VAR planning problem involves the determination of location and sizes of new compensators considering contingencies and voltage collapse problems in a power system. Applications of FACTS to power system stability in particular have been carried out using same databases. The results of this survey are shown in Figure 1, Figure 2 It was found that the ratio of FACTS applications to the stability study with respect to other power system studies is more than 60% in general. This reflects clearly the increasing interest to the different FACTS controllers as potential solutions for power system stability enhancement problem. It is also clear that the interest in the 2nd generation of FACTS has been drastically increased while the interest in the 1st generation was decreased. The potential of FACTS controllers to enhance power system stability has been discussed, where a comprehensive analysis of damping of power system electromechanical oscillations using FACTS was presented. The damping torque contributed by FACTS devices, where several important points have been analyzed and confirmed through simulations.

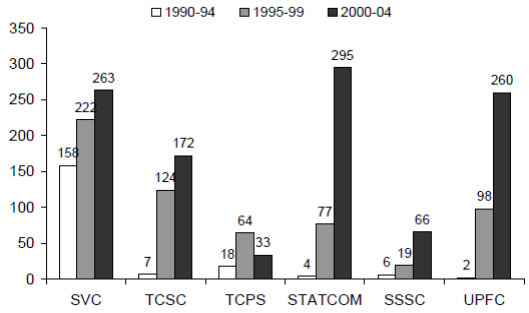


*Fig 1. Statistics for FACTS applications to different power system studies*

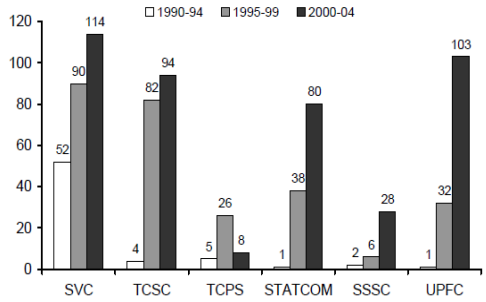


*Fig 2. Statistics for FACTS applications to power system stability*

# IV. NEURAL NETWORKS IN POWER SYSTEMS

Several papers dealing with ANN applications in power systems are briefly described in the subsections below. They have been grouped with respect to the following application areas: Static and dynamic security assessment, transient stability assessment, identification, modeling and prediction, control, load forecasting and fault diagnosis. This work, referenced by the most of the authors in ANNs and power systems, dealt with the assessment of dynamic security. An adaptive pattern recognition approach based on a feed forward neural net with a back propagation learning scheme was implemented to synthesize the Critical Clearing Time (CCT). This parameter is one of paramount importance in the post-fault dynamic analysis of interconnected systems. The net successfully performed the estimation task for the variable system topology conditions. In [4]-1992, the same authors described the results of the investigation to "discover" relevant ANN training information. Simulations results showed how autonomous feature discovery was carried out in terms of direct system measurements instead of pragmatic features based on the engineering understanding of the problem. In this case unsupervised and supervised learning paradigms in tandem were used. The stability boundary was constructed using tangent hyper surfaces. ANNs were used to determine the unknown coefficients of the hyper surfaces independently of operating conditions. Numerical results and comparisons between CCT analytically obtained and ANN-based indicated that this approach provides quick assessment of power system security in [25]-1993, the authors (joined with Lee) presented a methodology applying ANN to carry out real-time stability analysis of power systems. Near-term transient stability of the system, mid-term and long-term dynamic security analysis were performed. The first one dealt with whether the system can return to steady-state, and the second one dealt with the manner of the final state is reached. They utilized the Kohonen Neural Net as classifier of power system states. The relation among the number of clusters, the number of neurons and the size of the power systems were investigated. Simulation results demonstrated the successful generalization property of the ANN. The important feature is that correct assessment was obtained not only when the net was queried with an element of the training set of data, but also at other operating conditions. The input stimulus for the net was contingency parameters such as transmission line status, machine excitations and generation level. Feed forward ANNs were used. Its effectiveness is demonstrated through a steady-state analysis on a synchronous generator. This generator was connected to a large power system. As input to the net, real power, power factor and power system stabilizer parameters were used. The output was a discrete signal: dynamically stable or unstable. The proposed ANN was compared with the multilayer feed forward with a back propagation-momentum learning algorithm. It was determined that the convergence of the proposed ANN was much faster and its misclassification rate was lower than using the back propagation-momentum method. It is said that the proposed ANN is more suitable for discrete output values.

*Transient Stability Assessment*: Decision-making systems (DMS) based on a preprocessor (parallel computational structure) and on two layers of equivalent neurons were used. The important difference between DMS and multilayer ANN is that the DMS doesn't require a back propagation learning rule but a perceptron convergence procedure.

## V. RESULTS & DISCUSSIONS

The control criterion of the *ANN* SVQC balances the voltage profile of the power system, while at the same time diminishes the active and reactive power losses. To evaluate the influence of the proposed ANN SVQC scheme we have focused on the power system operation economy and its security. The ANN SVQC-controlled power system voltage profile (labeled as *ANN)* was compared to that of the base power system operating state in which the voltage references were preset to a fixed value. These power system states also arose immediately after the disturbance and before the ANN SVQC reacted. They have been labeled as base case. The two voltage profiles were in turn compared to the optimal voltage profile, calculated with a help of the OPF. For this purpose, the following criteria were selected: voltage profile of the entire EPS for a selected operating state and voltage histogram for the test set and a selected node. In economical operation, the power system is supposed to have minimal active and reactive power losses. In addition to voltage conditions, a histogram features *ANN* SVQC induced improvement of active and reactive power losses with regards to the base cases been produced for the test set.

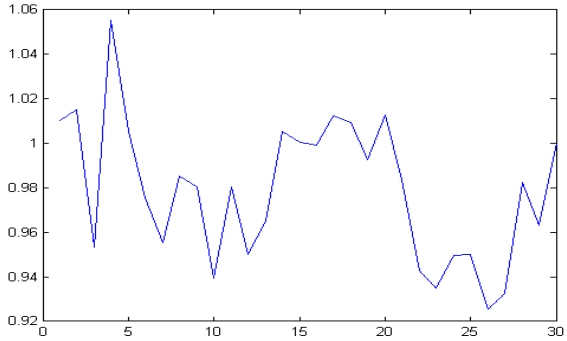


Fig 3.Voltage profiles in a healthy system case 30 base cases

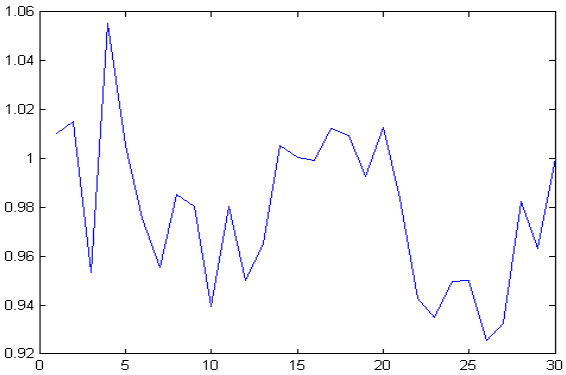


Fig 4.Voltage profiles **in a** healthy system case 30 opf

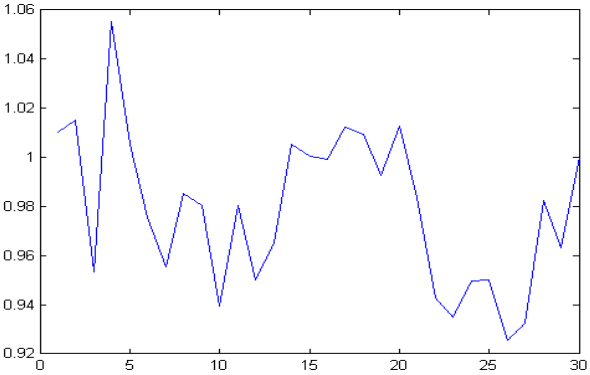


Fig 5.Voltage profiles in a healthy system case 30opf Ann

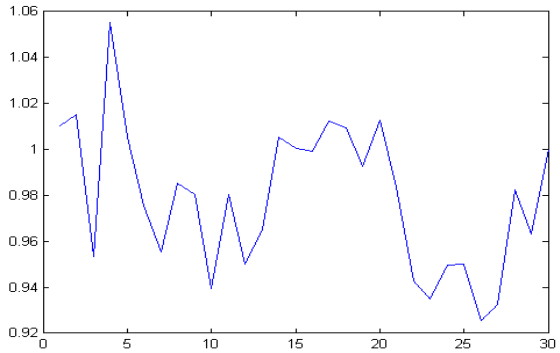

Fig 6.Voltage profiles in a healthy system case 30 opf ANN Outage

The statistical evaluation of the *ANN* SVQC-s performance regarding active power losses may be seen in Fig. 3. It shows significant improvement over the base case, whereas frequency distribution of the ANN results resembles the OPF distribution. A similar conclusion can be drawn for the ANN improvement of reactive power losses when compared to OPF results in Fig. 4. A power system voltage profile presents voltage levels for all the nodes and for a selected operating state. On the figures, the first ten data points depict generator nodes while the rest are load buses. *On* the other hand, voltage histograms offer the frequency of certain voltages in a selected power system bus for all the operating states in the entire test set. In both cases, the comparison comprises base cases, operating states the *ANN* SVQC action and optimal solutions. Through combining both methods it is possible to correlate the events in the power system and the ANN SVQC corrective actions, which in turn leads to security assessment. In Fig. 5, a comparison among base case, ANN and OPF voltage profiles can be observed. The ANN voltages in most buses converge to a sub-optimal profile, close to the optimal one. In addition, the response of the ANN SVQC controlled power system to an outage of the *ANN* controller in generator bus G5 is depicted. The comparison of the voltage profiles in line L1516 outage for a selected operating state is shown on Fig. 6. Although the improvement of the *ANN* controlled profile over base case is not as significant as the one on Fig. 5*,* Fig 6, it is safe to conclude that the ANN SVQC is able to handle line outages adequately. The security of the ANN controlled power system is enhanced.

## VI. CONCLUSION

In this review, the current status of power system stability enhancement using FACTS controllers was discussed and scrutinized. The essential features of FACTS controllers and their potential to enhance system stability was addressed. The location and feedback signals used for design of FACTS-based damping controllers were discussed. The coordination problem among different control schemes was also considered. Performance comparison of different FACTS controllers has been reviewed. The likely future direction of FACTS technology, especially in restructured power systems, was discussed as well. In the paper, a proposal of a decentralized secondary voltage control framework using *ANN* that was developed for a Slovenian power system is outlined. In addition to standard SVQC objectives, the proposed ANN based scheme exerts also favorable influence on power system operation economy and security the voltage profile during normal operation without outages is governed. Sub-optimally using only ANN SVQC. At the same time, the operation remains economical, as the active and reactive power losses are sub-optimal and comparable to those obtained via OPF and improved when compared to base case**.**

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# IMPROVEMENT OF DYNAMIC PERFORMANCE OF THREE-AREA THERMAL SYSTEM UNDER DEREGULATED ENVIRONMENT USING HVDC LINK

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## *ABSTRACT*

*This paper presents an analysis on dynamic performance of a three-area thermal system interconnected with HVDC links when subjected to parametric uncertainties. In this paper all the three areas consists of thermal power plants. The HVDC link is used as a system interconnection between all the three areas. Open transmission access and the evolution of more socialised companies for generation, transmission and distribution affects the formulation of Automatic Generation Control (AGC) problem. So, the traditional three area system is modified to take into account the effect of bilateral contracts on the dynamics. It has been observed that the dynamic response of three-area interconnected thermal plants through tie-line is sluggish and degraded when compared to the dynamic response of three area interconnected thermal power plants connected through a DC link.*

***KEYWORDS*:** *AGC, HVDC link, Deregulated Power system.*

## I. NOMENCLATURE

| | |
|---|---|
| ISO | Independent System Operator |
| VIU | Vertically Integrated Utilities |
| DISCOs | Distribution Companies |
| GENCOs | Generation Companies |
| TRANSCO | Transmission system |
| F | Area frequency |
| P | Tie net tie line power flow |
| $P_T$ | Turbine power |
| $P_V$ | Governor valve position |
| $P_C$ | Governor set point |
| ACE | Area control error |
| apf | Area control error Participation factor |
| cpf | Contract Participation Factor |
| DPM | DISCO Participation Matrix |
| Δ | Deviation from nominal value |
| $K_P$ | Subsystem equivalent gain |
| $T_P$ | Subsystem equivalent time constant |
| $T_T$ | Turbine time constant |
| $T_H$ | Governor Time constant |
| $T_{DC}$ | Time delay of DC Link |
| R | Droop characteristic |
| B | Frequency bias |
| $T_{ij}$ | Tie line synchronizing coefficient between areas I and j |
| $P_d$ | Area load disturbance |
| $P_{Lji}$ | Contracted demand of DISCO j in area i |
| $P_{Ulji}$ | Un-contracted demand of DISCO j in area i |
| $P_{Mji}$ | Power generation of GENCOS j in area i |
| $P_{Loc}$ | Total local demand |
| g | Area interface |
| f | Scheduled power tie line power flow deviation (DPtie,sch) |

## II. INTRODUCTION

In the power system, any sudden load change causes the deviation of tie-line exchanges and the frequency fluctuations. So, AGC is very important for supplying electric power with good quality. Now-a-days, the electric power industry is moving towards an open market deregulated environment in which consumers have an opportunity to select among different competing suppliers of electric energy. Deregulation is the collection of unbundled rules and economic incentives that governments

set up to control and drive the electric power industry. Power system under open market scenario consists of generation companies (GENCOs), distribution companies (DISCOs), and transmission companies (TRANSCOs) and independent system operator (ISO). In deregulated environment, each component has to be modelled differently because each component plays an important role. There are crucial differences between the AGC operation in a vertically integrated industry (conventional case) and horizontally integrated industry (new case). In the reconstructed power system after deregulation, operation, simulation and optimization have to be reformulated although basic approach to AGC has been kept the same. In this case, a DISCO can contract individually with any GENCO for power and these transactions are made under the supervision of ISO. To understand how these contracts are implemented, DISCO participation matrix concept is used. The information flow of the contracts is superimposed on the traditional AGC system. In the literature, there are some research studies on deregulated AGC.

The power system operation in an interconnected grid system improves system security and economy of operation. In addition, the interconnection permits the utilities to make economic transfers and takes the advantages of the most economical sources of power. Each power system within such a pool operates technically and economically, but contractually tied to other pool members in respect to certain generation and scheduling features. To fulfil these contracts, there is a requirement of transmission lines which are capable of exchanging large amounts of power between them over a wide spread area effectively and efficiently. In the early days this purpose was served by AC tie-lines. However, many problems have been faced with AC tie-line interconnections particularly in case of transmission over long distances. These problems have been overcome by the use of asynchronous HVDC link connecting two control areas. By this interconnection with HVDC link, frequency deviation is very low which leads to improvement of quality and continuity of power supply to the customers.

In deregulated system, the structure of power system is modified in such a way that would allow the evolution of more industries for generation (GENCOs), Transmission (TRANSCOs) and Distribution (DISCOs).

The main objective of this paper is to develop a three area thermal system under deregulated environment by incorporating the bilateral contracts on the system. Also, to improve the dynamic performance of the system, the conventional EHVAC tie line is replaced with the HVDC link connecting two areas.

## III. RESTRUCTURED SYSTEM FOR AGC WITH THREE AREAS

Each control area consists of two thermal plants and also two DISCOs as shown in Fig. 1. The detailed schematic diagram of three area thermal system is also given in Fig. 3. In this open market scenario, any GENCO in one area may supply DISCOs in the same area as well as DISCOs in other areas through asynchronous HVDC links allowing power transfer between the areas. In other words, for restructured system having several GENCOS and DISCOs, any DISCO may contract with any GENCO in another control area independently. This is called as ‘‘bilateral transaction’’. The transactions have to be carried out through an independent system operator (ISO). The main purpose of ISO is to control many ancillary services, one of which is AGC. In deregulated environment, any DISCO has the liberty to purchase MW power at competitive price from different GENCOs, which may or may not have contract with the same area as the DISCO. For practice, GENCO–DISCO contracts are represented with ‘DISCO participation matrix’ (DPM). Essentially, DPM gives the participation of a DISCO in contract with a GENCO. In DPM, the number of rows is equal to the number of GENCOs and the number of columns is equal to the number of DISCOs in the system. Any entry of this matrix is a fraction of total load power contracted by a DISCO toward a GENCO. As a result, total of entries of column belong to DISCO1 of DPM is $\sum cpf_{ij}=1$. The corresponding DPM to the considered power system having three areas and each of them including two DISCOs and two GENCOSs is given as follows:

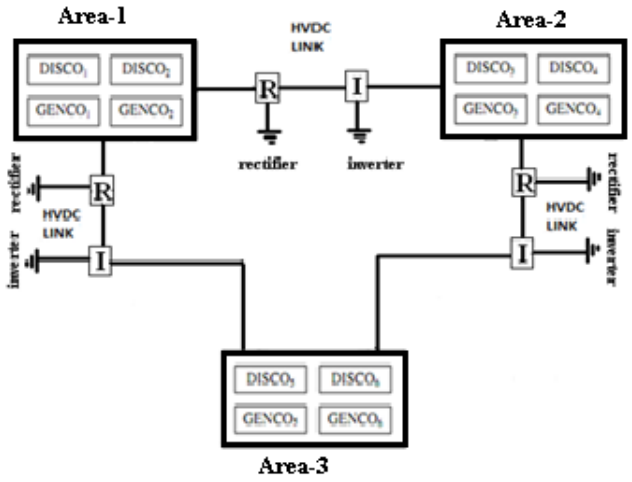


Fig. 1. Configuration of three-area Power System

$$DPM = \begin{bmatrix} cpf_{11} & cpf_{12} & cpf_{13} & cpf_{14} & cpf_{15} & cpf_{16} \\ cpf_{21} & cpf_{22} & cpf_{23} & cpf_{24} & cpf_{25} & cpf_{26} \\ cpf_{31} & cpf_{32} & cpf_{33} & cpf_{34} & cpf_{35} & cpf_{36} \\ cpf_{41} & cpf_{42} & cpf_{43} & cpf_{44} & cpf_{45} & cpf_{46} \\ cpf_{51} & cpf_{52} & cpf_{53} & cpf_{54} & cpf_{55} & cpf_{56} \\ cpf_{61} & cpf_{62} & cpf_{63} & cpf_{64} & cpf_{65} & cpf_{66} \end{bmatrix}$$

Where, cpf represents ‘‘contract participation factor’’. For example, the fraction of the total load power contracted by DISCO1 from GENCO2 is represented by (2, 1) entry. Off-diagonal blocks correspond to demands of the DISCOs in one area to the GENCOs in another area. In the deregulated case, when the load demanded by a DISCO changes, a local load change is observed in the area of the DISCO. In the equations of the system given in Appendix A, such load changes, $\Delta P_{Li}$ (i =1... 6), are contained. Since there are a lot of GENCOs in each area, area control error (ACE) signal must be shared by these GENCOs in proportion to their contributions. The coefficients, which represent this sharing, are called as ‘‘ACE participation factors (apf)’’ and where m is the number of GENCOs in each area. As different from conventional AGC systems, any DISCO can demand power from all of the GENCOs. These demands are determined by cpfs, which are contract participation factors, as load of the DISCO.

The dotted and dashed lines show the demand signals based on the possible contracts between GENCOS and DISCOs that carry information as to which GENCOs have to follow a load demanded by that DISCO. These new information signals were absent in the traditional AGC scheme. As there are many GENCOS in each area, the ACE signal has to be distributed among them due to their ACE participation factor in the AGC task and

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## IV. MATHEMATICAL MODEL OF HVDC LINK AS A CONSTANT CURRENT CONTROLLER

For a two terminal DC link, with the response type controller model, an alternative representation of DC network is to use a transfer function instead of a resistance.

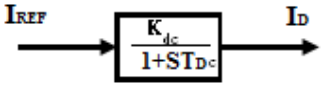



**Fig.2. Transfer function of HVDC**

In this case, the time constant $T_{DC}$ represents the delay in establishing the DC current after a step change in the order is given.

## V. SIMULATION RESULTS

Each control area of the deregulated power system is connected to another control area through a HVDC link as given in Section 3. To illustrate the improvement of dynamic response of the three area deregulated system with HVDC link compared to the three area deregulated system with tie-line under contract variations. Simulation results are studied for two contract variation scenarios.
In deregulated environment, the DISCO participation matrix (DPM) is chosen on the basis of open market strategy. Change of DPM changes the generation schedule of all the GENCOs and hence the system behavior in the restructured environment. So it is interesting to know how the system behaves in the deregulated environment with change in the DPM matrix. To examine this, Different distribution participation matrices (DPM) are introduced on the basis of contact variations. The two different DPMs considered for the present investigations are given below as A and B

*A.Scenario-1:*

In this scenario DISCO has the freedom to contract with any GENCOs or other areas. So, all the DISCOs contracts with the GENCOs on following DPM.

$$DPM = \begin{bmatrix} 0.3 & 0.25 & 0 & 0.4 & 0.1 & 0.6 \\ 0.2 & 0.15 & 0 & 0.2 & 0.1 & 0 \\ 0 & 0.15 & 0 & 0.2 & 0.2 & 0 \\ 0.2 & 0.15 & 1 & 0 & 0.2 & 0.4 \\ 0.2 & 0.15 & 0 & 0.2 & 0.2 & 0 \\ 0.1 & 0.15 & 0 & 0 & 0.2 & 0 \end{bmatrix}$$

It is considered that each GENCO participates in AGC in each control area as defined by following:
$ap_1$ =0.5, ap2= 1-ap1=0.5, ap3=0.5,
ap4= 1-ap3=0.5, ap5=0.6, ap6= 1-ap5=0.4.

ACE participation factor affects only transient behaviour of the system. It does not affect the steady state behaviour

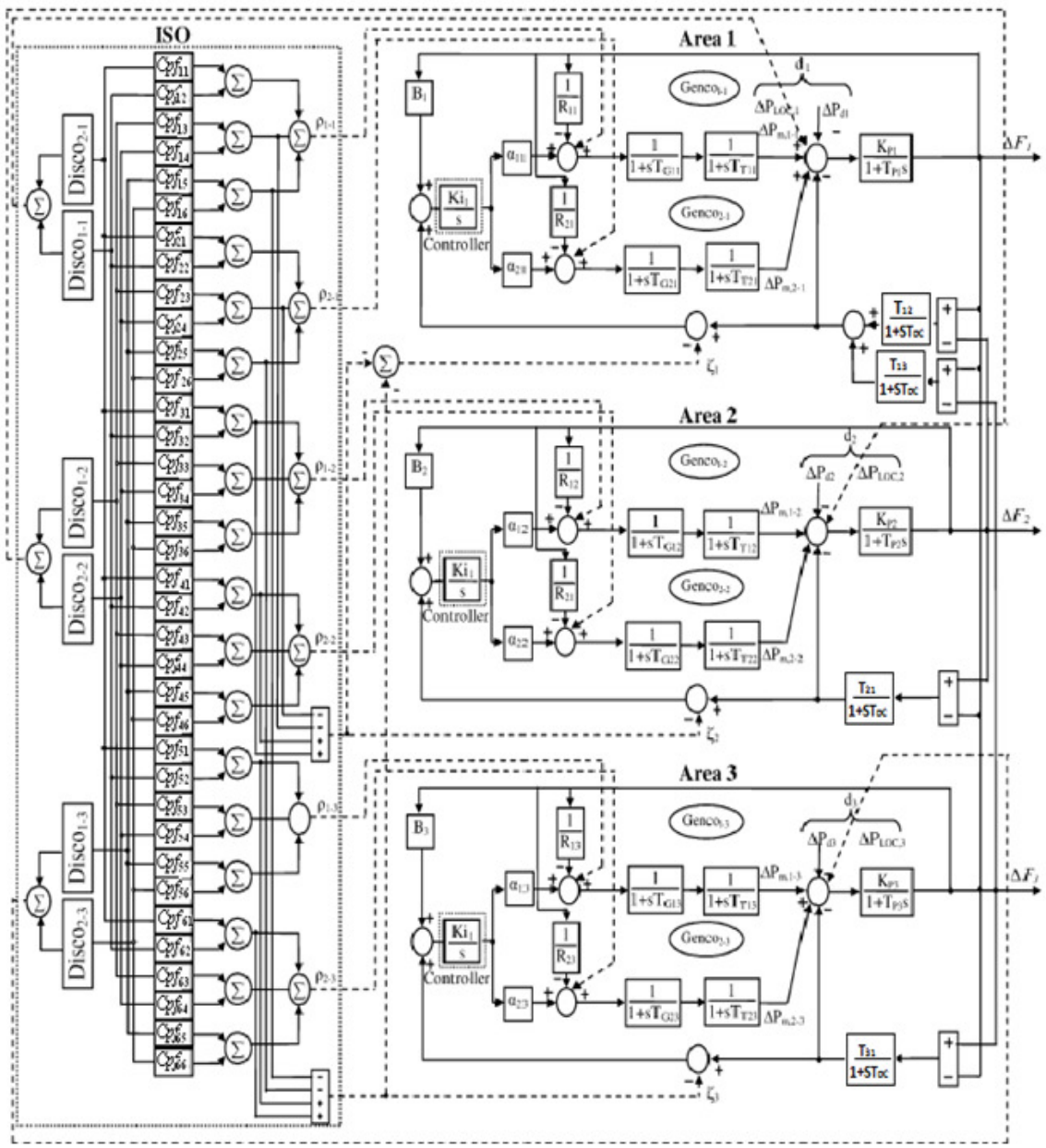
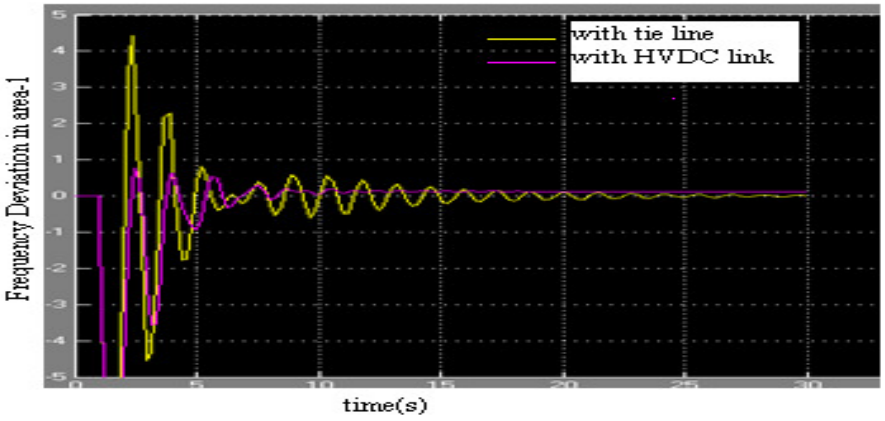
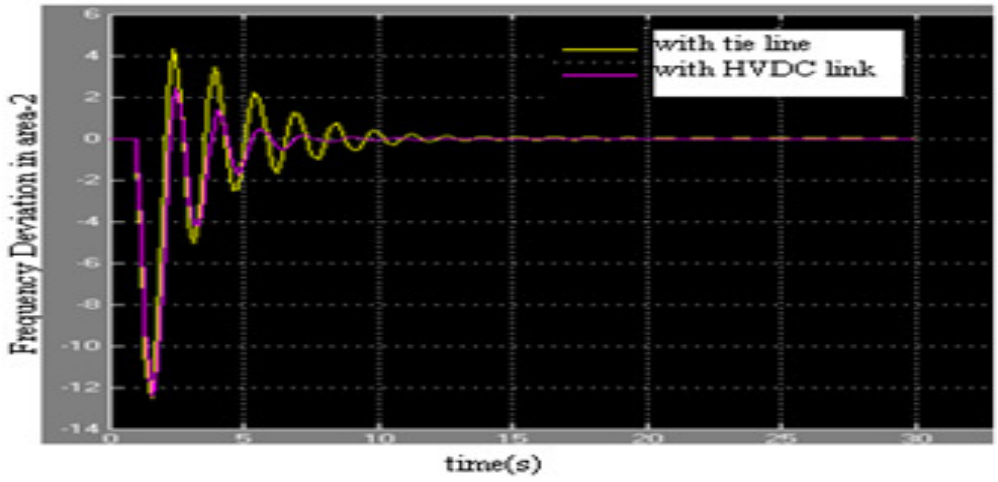



Fig .3.Three-Area Thermal System under Deregulated environment with HVDC link.

(a)



(b)




(c)

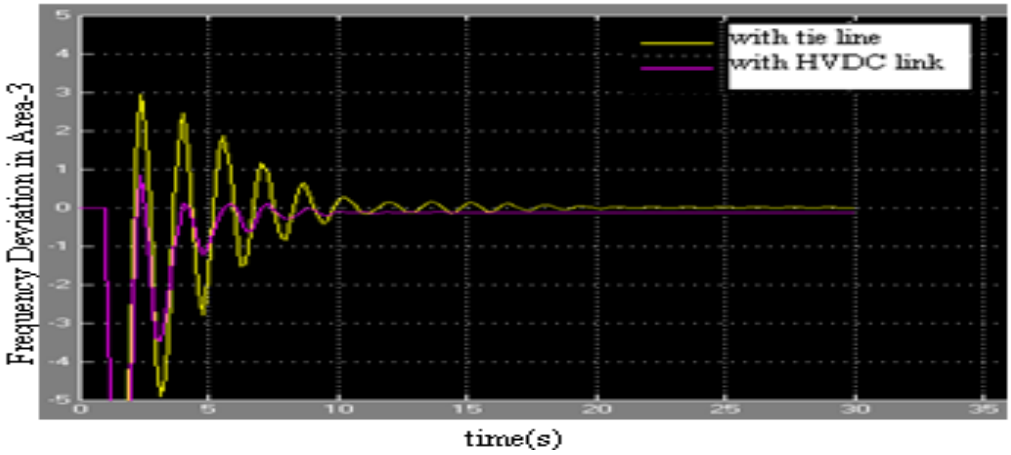



Fig.4. (a) Frequency deviation in area-1(rad/sec), (b) Frequency deviation in area- 2(rad/sec), (c) Frequency deviation in area-3(rad/sec).

*b. Scenario-2:*

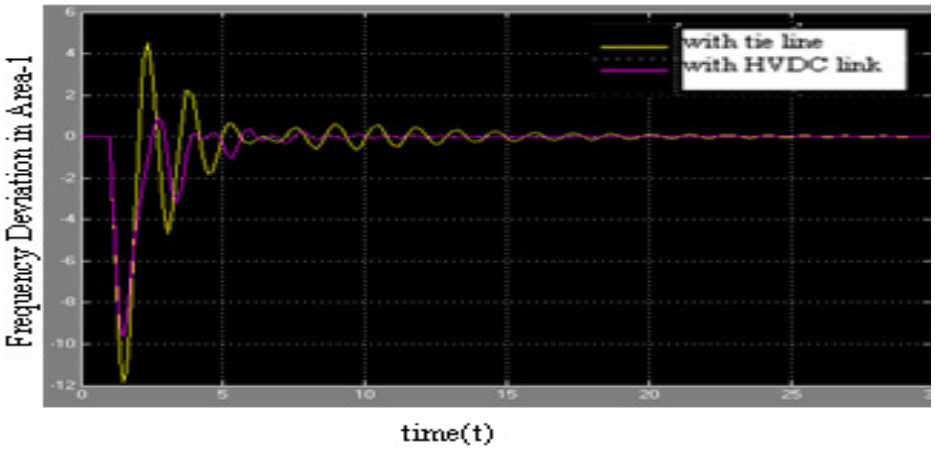
In this case all GENCOs in each control area participate in AGC. DPM matrix is assumed to be

$$DPM = \begin{bmatrix} 0.25 & 0 & 0.25 & 0 & 0.5 & 0 \\ 0.5 & 0.25 & 0 & 0.25 & 0 & 0 \\ 0 & 0.5 & 0.25 & 0 & 0 & 0 \\ 0.25 & 0 & 0.5 & 0.75 & 0 & 0 \\ 0 & 0.25 & 0 & 0 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

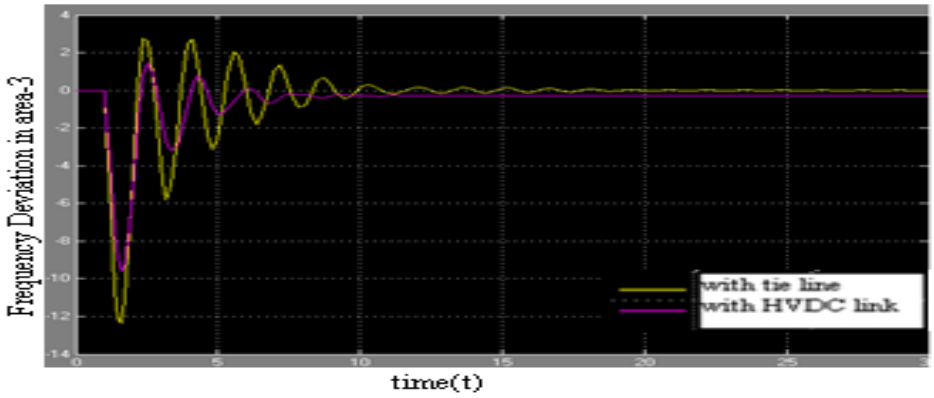
In this scenario, it is considered that, each GENCO participates in AGC in each control area as defined by following:

$ap_1$ =0.3, ap2= 1-ap1=0.7, ap3=0.3, ap4= 1-ap3=0.7, ap5=0.3, ap6= 1-ap5=0.7.

(a)




(b)




(c)

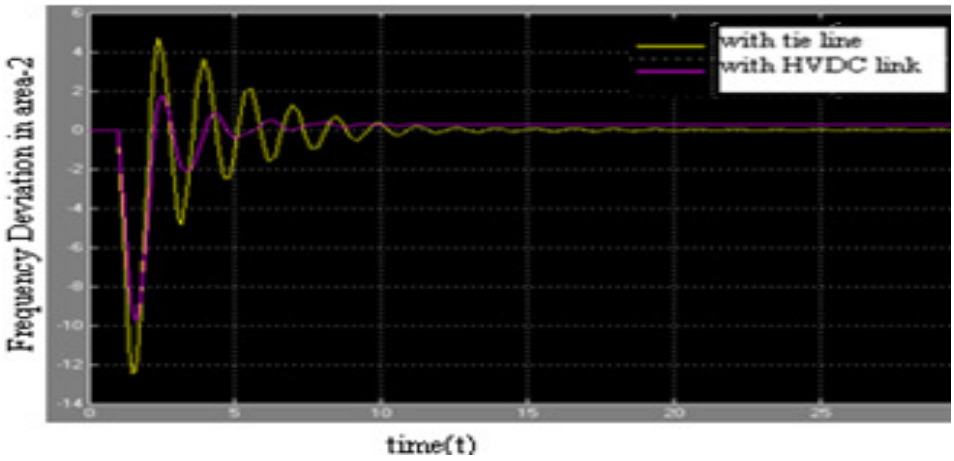



Fig.5. (a) Frequency deviation in area-1(rad/sec), (b) Frequency deviation in area- 2(rad/sec), (c) Frequency deviation in area-3(rad/sec).

# VI. CONCLUSION

The dynamic performance of the system due to sudden load disturbance in 3-area interconnected power system under deregulated environment with HVDC link has been studied comprehensively. The power system model with thermal power plants is considered for the study in deregulated environment. The dynamic response of three-area power system with HVDC link has been improved compared to dynamic response of same system with AC tie-line. With HVDC link, the dynamic oscillations die out quickly and system comes to steady state with negligible frequency deviation. So, it may be concluded that HVDC link can be a new ancillary service for stabilization of frequencies in the three-area deregulated environment.

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# VOLTAGE SECURITY IMPROVEMENT USING FUZZY LOGIC SYSTEMS

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## *ABSTRACT*

*This paper presents a new approach using fuzzy bet theory for voltage and reactive power control of power systems. The predication of steady state voltage stability conditions in a transmission network. The voltage stability is checked by formulating an L and the corresponding uncertainties input parameters are efficiently modeled in terms of fuzzy sets by using triangular membership function. The proposed technique will be highly useful to ensure voltage security of power system by predicting the nearness of voltage collapse with respect to the existing load condition. The approach translates violation level of buses voltage and controlling ability of controlling devices into fuzzy set notations using linearized model. A modified IEEE 30-bus test system is used to demonstrate the application of the proposed approach. Simulation result shows that the approach is efficient and has good flexibility and adaptability for voltage-reactive power control.*

***KEYWORDS:*** *Fuzzy sets, membership functions, voltage-reactive power control voltage violation level, Power system enhancement, Stability, Voltage Stability.*

## I. INTRODUCTION

Power system throughout the world is undergoing tremendous changes and developments due to rapid Restructuring, Deregulation and Open-access policies. Greater liberalization, larger market and increasing dependency on the electricity lead to the system operators to work on limited spinning reserve and to operate on vicinities to maximize the economy compromising on the reliability and security of the system for greater profits, which lead to establishment of a monitoring authority and accurate electronic system to prevent any untoward incidents like Blackouts. Optimal Power Flow (OPF) study plays an important role in the Energy Management System (EMS), where the whole operation of the system is supervised in each conceivable real time intervals. Optimal Power flow is the assessment of the finest settings of the control variables viz. the Active Power and Voltages of Generators, Discrete variables like Transformer taps, Continuous variables like the Shunt reactors and Capacitors and other continuous and discrete variables so as to attain a common objective such as minimization of operating cost or Social Welfare while respecting all the system limits for safe operation. This greater dependency on Electric Power has brought in the stage where the consumer depends not only on the availability of the electricity, but also looks for Reliable, Secure, Quality and Uninterrupted supply. In order to enhance the voltage security; power systems are equipped with a lot of voltage controlling devices such as generators, tap changing transformers, shunt capacitors/reactors, synchronous condensers, and static VAR compensators etc. Either by the variations of load or by the changes of network configuration, a real time control employing those controlling devices is required to fast alleviate the problems caused by the perturbations. For voltage security problems, linear programming (LP) [1]–[4] utilized linearized models to attain an objective function and constraints to formulate the problem. The LP results may not represent the optimal solution for inherently nonlinear objective functions; also, the approach requires a great deal of computation. In the other way, rule-based approach [5] and expert systems [6], [7] as well as hybrid (heuristic and algorithmic) systems [8]–[10] proposed rigorous mathematical models and numerical approaches to solving the problems. Fuzzy set theory [11], [12] was also applied to solve the

problems [13]–[17], in this application, objectives and constraints were first translated into fuzzy set notations, then LP was employed to find the optimal solution. In [18], an approximate reasoning based on a flexible model which employed an expert system and fuzzy sets to solve the VAR control problems was proposed. In [19], a new fuzzy control approach which repeatedly uses fuzzy operations to effectively enhance voltage profile was presented. In this paper, we introduce a new voltage/reactive power control model which uses fuzzy sets to formulate the problem, such that the voltage security improvement is achieved while loss reduction is also attained. In this modeling, bus voltage violation level and controlling ability of controlling device are first translated into fuzzy set notations, and then max–min operation is employed to find a feasible solution set which enhances the voltage security. Final solution is attained using min-operation aiming at further reducing the power loss. The method is very simple and straightforward. The proposed method has been applied to a modified IEEE 30-bus test system. Results show that the approach is effective for improving voltage security and simultaneously lowering power loss. In this paper, we introduce a new voltage-reactive power control model using fuzzy sets, which aims at the enhancement of voltage security. In this modeling, two linguistic variables are applied to measure the proximity of a given quantity to a certain condition to be satisfied. Both bus voltage violation level and controlling ability of controlling devices are first translated into fuzzy set notations, and then through fuzzy operations it could fast found the answer for the realistic question. The proposed approach is simple and straightforward, which defines the membership functions of the two linguistic variables ingeniously, so that the merits of fuzzy technique are brought into play. The proposed method has been applied to a modified IEEE 30-bus and the simulation results has got.

## II. MATHEMATICAL MODELLING OF LINE VOLTAGE STABILITY

The proposed line voltage stability is capable of yielding accurate, consistent and reliable results as demonstrated in the case studies carried out under this paper.

$$L_i = \frac{2\frac{B}{A}\sqrt{(P_m^{\,2}+Q_m^{\,2}}}{\frac{V_K^{\,2}}{A^2} - 2\frac{B}{A}P_m\cos(\beta-\alpha) - 2\frac{B}{A}Q_m\sin(\beta-\alpha)} \le 1 \qquad \text{----- (1)}$$

where,
Pm – Receiving end real power in p.u
Qm – Receiving end reactive power in p.u
Vk – Sending magnitude voltage in p.u
As long as above is less than unity, the system is stable. Li is termed as voltage stability of the line. At collapse point, the value of Li will be unity. Based on voltage stability indices, voltage collapse can be accurately be predicted. The lines having high value of the can be predicted as the critical lines, which contribute to voltage collapse. This method is used to assess the voltage stability.

## III. FUZZY BASED LOAD FLOW ANALYSIS

In Newton-Raphson load flow method the repetitive solution is obtained by the equations (1). By using these equations "δ" and "V" is updated in each iteration. In fuzzy load flow problem "Fuzzy Logic" is used to update "δ" and "V".

$$\begin{bmatrix}\Delta P\\ \Delta Q\end{bmatrix} = \begin{bmatrix}H & N\\ M & L\end{bmatrix}\begin{bmatrix}\Delta\delta\\ \Delta|V|\end{bmatrix} \qquad \text{------- (2)}$$

### A. Main Idea of Fuzzy Load Flow (FLF) Algorithm

The Equation (1) given by Newton-Raphson can be expressed as for the proposed Fuzzy by the equation (**2**) the above equation denotes that the correction of state vector ΔX at each node of the system is directly proportional to vector ΔF. The proposed fuzzy load flow algorithm is based on the

previous Newton – Raphson load flow equation but the repeated update of the state vector of the system will be performed via expressed by, ΔF [J]ΔX The above equation denotes that the correction of state vector ΔX at each node of the system is directly proportional to vector ΔF. The proposed fuzzy load flow algorithm is based on the previous Newton – Raphson load flow equation but the repeated update of the state vector of the system will be performed via expressed by ΔX = fuzzy[ ΔF]

## B. Fuzzy Logic Load Flow Algorithm

In Figure 1 the power parameters such as real power (ΔFp ) and reactive power (ΔFq ) are calculated and introduced to the p- and q-v fuzzy logic controller (FLC) respectively. The FLCs algorithm executes the state vector ΔX namely, the correction of voltage magnitude Δδ for the p-q cycle and the voltage magnitude ΔV for the q-v cycle.

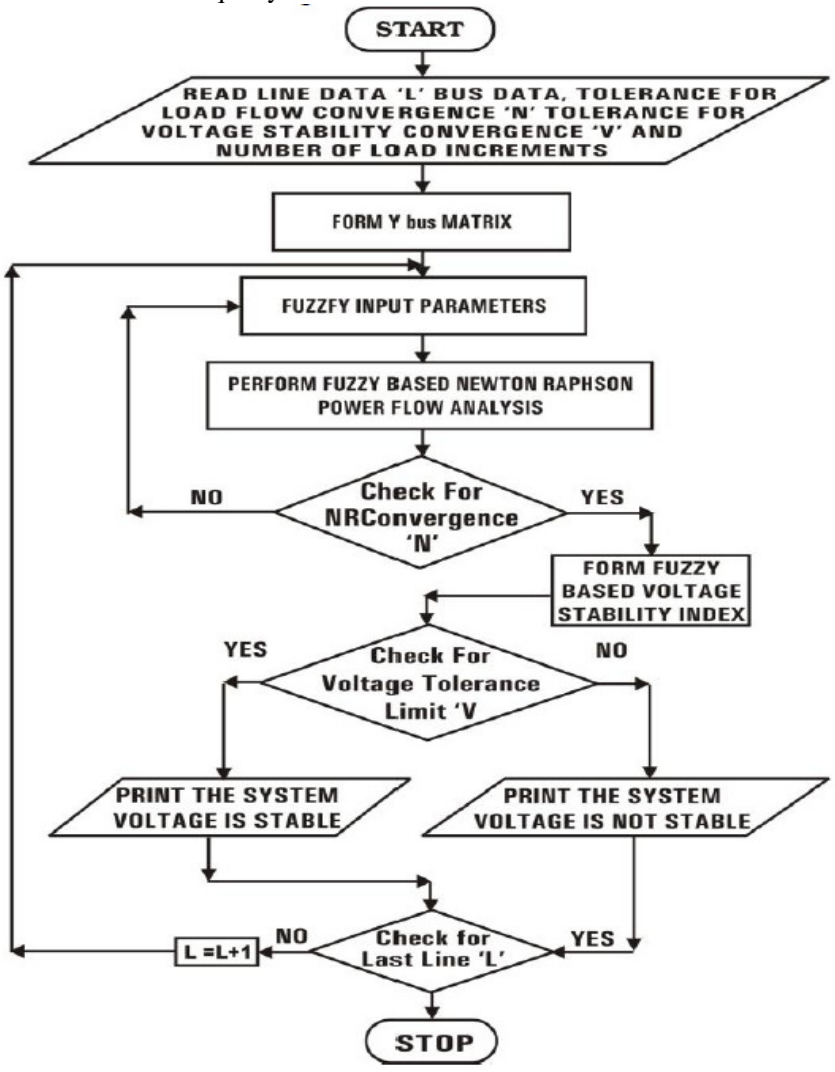


Figure1. Flow Chart for the Proposed Fuzzy

The described computational procedures iii the solution process of the proposed control are given as follows:

Step 1: Input data of network configuration, line impedance, bus power, bus voltage limits and controlling margin.

Step 2: Perform a base case load flow by Newton-Raphson method.

Step 3: Find the sensitivity coefficients.

Step 4: Calculate the controlling ability.

Step ***5:*** Find the membership value of bus voltage violation and controlling ability.

Step 6: Evaluate the optimal control solution.

Step *7:* Modify the value of the control variables.
Step 8: If all buses are enhanced to the desired voltage level, go to nest step; otherwise, go to step 4.
Step 9: Perform the load flow study and output the results.

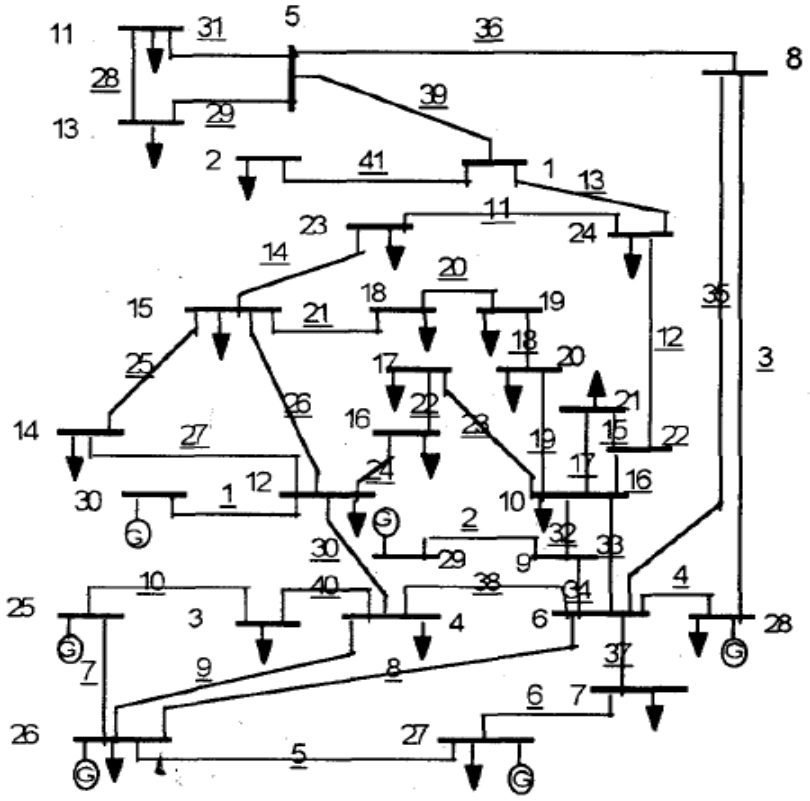

Figure 2: A modified IEEE 30-bus test system

## IV. REACTIVE POWER COMPENSATION

We need to release the power flow in transmission lines for partially solving of problem of losses as well as other problems. We can't do anything with active power flow, but we could supply the reactive power locally where it is highly consumed in a system. In this way the loading of lines would decrease. It would decrease the losses also and with this action the problem of voltage drops could be solved also. By means of reactive power compensation transmission system losses can be reduced as shown in many papers in the literature, see e.g., [20]-[22]. It has also been widely known that the maximum power transfer of the transmission system can be increased by shunt reactive power compensation, typically by capacitors banks placed at the end of the transmission lines or a the load terminals [23]. Therefore, planning of reactive power supports would give benefits to the users of the transmission systems, in terms of loss reduction, among other technical benefits, such as improving steady-state and dynamic stability, improve system voltage profiles, etc. which are documented in [24]. The reactive power planning problem involves optimal allocation and sizing of reactive power sources at load centers to improve the system voltage profile and reduce losses. However, cost considerations generally limit the extent to which this can be applied. The transmission of active power requires a difference in *angular phase* between voltages at the sending and receiving points (which is feasible within wide limits), whereas the transmission of reactive power requires a difference in *magnitude* of these same voltages (which is feasible only within very narrow limits). But why should we want to transmit reactive power anyway? Is it not just a troublesome concept, invented by the theoreticians, that is best disregarded? The answer is that reactive power is consumed not only by most of the network elements, but also by most of the consumer loads, so it must be supplied somewhere. If we can't transmit it very easily, then it ought to be generated where is needed. Reactive power is needed to form magnetic fields in motors and other equipment, but it cannot perform any

actual work itself. The more reactive power that is distributed in the electrical system, the less space is left for productive or active power. By generating reactive power as close as possible to the machine which is to use it, there is less need to waste valuable resources in transporting it in the power network. This is known as reactive power compensation improvement in the power factor - the efficiency rating - of the plant. The best part is, everyone is a winner.

Shunt capacitors are employed at substation level for the following reasons:

***1. Voltage regulation***: The main reason that shunt capacitors are installed at substations is to control the voltage within required levels. Load varies over the day, with very low load from midnight to early morning and peak values occurring in the evening between 4 PM and 7 PM. Shape of the load curve also varies from weekday to weekend, with weekend load typically low. As the load varies, voltage at the substation bus and at the load bus varies. Since the load power factor is always lagging, a shunt connected capacitor bank at the substation can raise voltage when the load is high. The shunt capacitor banks can be permanently connected to the bus (fixed capacitor bank) or can be switched as needed. Switching can be based on time, if load variation is predictable, or can be based on voltage, power factor, or line current.

***2. Reducing power losses***: Compensating the load lagging power factor with the bus connected shunt capacitor bank improves the power factor and reduces current flow through the transmission lines, transformers, generators, etc. This will reduce power losses (I2R losses) in this equipment.

***3. Increased utilization of equipment*:** Shunt compensation with capacitor banks reduces KVA loading of lines, transformers, and generators, which means with compensation they can be used for delivering more power without overloading the equipment. Reactive power compensation in a power system is of two types—shunt and series. Shunt compensation can be installed near the load, in a distribution substation, along the distribution feeder, or in a transmission substation. Each application has different purposes. Shunt reactive compensation can be inductive or capacitive. At load level, at the distribution substation, and along the distribution feeder, compensation is usually capacitive. In a transmission substation, both inductive and capacitive reactive compensation are installed [16].

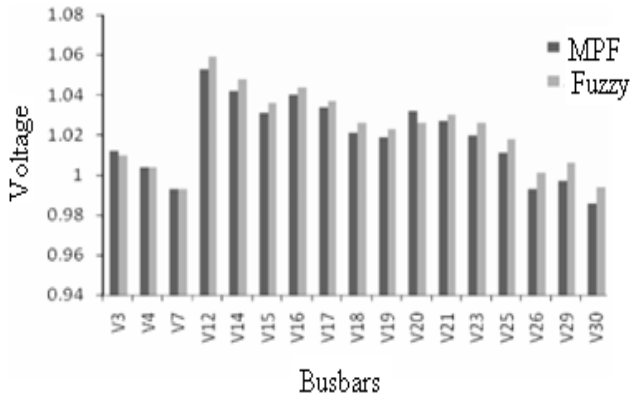


Figure 3: Voltages at load buses at full load

## V. RESULTS AND DISCUSSIONS

For verifying the effectiveness of the proposed method, a modified IEEE 30-bus test system shown in Fig 2 is tested Tables 1 and 2 list system parameters and initial buses data In this system, there are reactive power sources a1 buses 10, 11 19. 24 and terminal generator voltage regulators at buses *25,* 26. 27. 28, 29 In order to show the effectiveness and adaptability of the proposed technique, executing the control actions of Fuzzy give the results of load voltages as in Fig3. The same figure compares the resultant load voltages obtained by MPF and Fuzzy techniques. It is clear that error between load voltages obtained by the two techniques is acceptable. Then, the Fuzzy is capable of suggesting proper control action to keep voltages at load buses within limits.

Four cases are investigated the following

*Case 1*: Load of bus 2 increases, which causes bus 2 to violate the voltage constraint, but the violation, is not serious.
*Case 2*: Load of buses 2, 11 and 13 increases, it causes voltage violations at buses 2, 11 and 13.
*Case 3*: Buses 2, 11 and 13 are heavily loaded like case 2; a double-circuit breakdown at line 28 is occurred. Simultaneously, the upper limit of reactive power at bus 10 is reduced to 13.2 p.u.. It causes a larger range of voltage violation at buses 2, 11 and 13.
*Case 4*: In addition to the disturbances described in case 3, there are the upper limits of reactive power at buses 10, 11, 19, and 24 all reduced to 0.2 p.u..
Very interesting definition of benefit with capacitor application can be found in one of the main benefits of applying capacitors is that they can reduce distribution line losses. Losses come from current through the resistance of conductors. Some of that current transmits real power, but some flows to supply reactive power. Reactive power provides magnetizing for motors and other inductive loads. Reactive power does not spin kWh meters and performs no useful work, but it must be supplied. Using capacitors to supply reactive power reduces the amount of current in the line. Since line losses are a function of the current squared, *I2R*, reducing reactive power flow on lines significantly reduces losses.

# VI. METHOD APPLIED TO REGIONAL GRID

In this method, the candidate positions of reactive power sources will be first identified using an optimal power flow (OPF) framework with the minimum total cost objective including costs of new reactive power sources.

Table1. Variation of line voltage stability using fuzzy with load increments for IEEE 30 bus system

| Line Details | | | Load in Percent of Base Case Load | | | | | |
|---|---|---|---|---|---|---|---|---|
| No. | Starting Bus | Ending Bus | 100 % | 200 % | 300 % | 350 % | 380 % | 401 % |
| 1 | 1 | 2 | 0.0359 | 0.0359 | 0.0359 | 0.0359 | 0.0359 | 0.0359 |
| 2 | 2 | 3 | 0.0867 | 0.0867 | 0.0867 | 0.0867 | 0.0867 | 0.0867 |
| 3 | 2 | 6 | 0.0332 | 0.1373 | 0.3225 | 0.4875 | 0.6517 | 0.9157 |
| 4 | 1 | 8 | 0.0572 | 0.1558 | 0.3420 | 0.5144 | 0.6895 | 0.9722 |
| 5 | 2 | 8 | 0.0209 | 0.1184 | 0.3036 | 0.4764 | 0.6536 | 0.9455 |
| 6 | 3 | 6 | 0.0516 | 0.0494 | 0.2313 | 0.3964 | 0.5639 | 0.8427 |
| 7 | 6 | 8 | 0.0121 | 0.0180 | 0.0175 | 0.0104 | 0.0019 | 0.0361 |
| 8 | 8 | 4 | 0.0785 | 0.1682 | 0.3208 | 0.4467 | 0.5638 | 0.7430 |
| 9 | 6 | 7 | 0.0830 | 0.0947 | 0.1251 | 0.1587 | 0.1979 | 0.2793 |
| 10 | 7 | 5 | 0.0531 | 0.1382 | 0.2661 | 0.3639 | 0.4160 | 0.5821 |
| 11 | 6 | 9 | 0.0821 | 0.0529 | 0.0258 | 0.0162 | 0.0170 | 0.0449 |
| 12 | 7 | 9 | 0.0010 | 0.0435 | 0.1047 | 0.1524 | 0.1968 | 0.2652 |
| 13 | 9 | 10 | 0.0070 | 0.0039 | 0.0069 | 0.0199 | 0.0353 | 0.0672 |
| 14 | 4 | 11 | 0.0062 | 0.0808 | 0.1893 | 0.2719 | 0.3465 | 0.4578 |
| 15 | 4 | 12 | 0.0185 | 0.0642 | 0.1200 | 0.1553 | 0.1822 | 0.2133 |
| 16 | 4 | 13 | 0.0265 | 0.0928 | 0.1783 | 0.2357 | 0.2819 | 0.3399 |

After solving the basic OPF we choose the candidate locations for optimal allocations of reactive power to the system. Then the reactive power sources are applied to different candidate places one by one and at several candidate places at the same time iteratively. The cost-benefit analysis will then be worked out against the candidate locations, with different standard sizes of reactive power sources, so as to arrive at the optimal plan for reactive power support in an iterative manner. Fig.1. presents the flow chart for the proposed method. The selected positions and sizes of reactive power are those which generate the system benefits larger than the costs involved which make the investment

economically justifiable. The simulations and results of this method will be given in below.Table1 implies the load variation of the system with uniform increment and clearly indicates that voltage collapse is to be occurred in the critical lines (3, 4 and 5) of the IEEE 30 bus system.

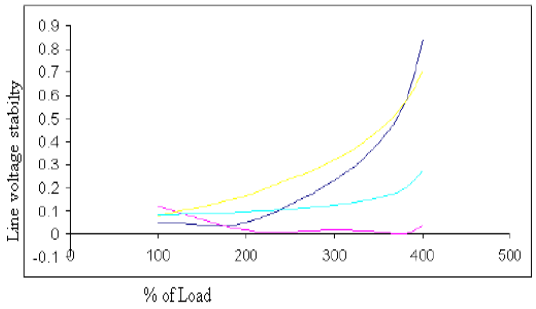


Fig4. Variation of bus voltage stability using fuzzy index with load increments of line on IEEE 30 bus system

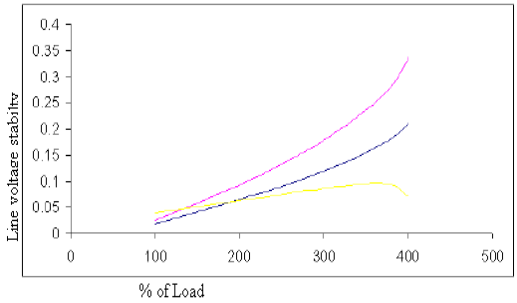


Fig5. Variation of bus voltage stability using fuzzy index with load increments of line of the IEEE 30 Bus system

Table2: y-bus Vs Bus Voltage Magnitudes in p.u

| Y | V |
|---|---|
| 4.2881 - 12.9014i | 0.9861 |
| 2.8588 - 8.6009i | 0.9545 |
| 0.7210 - 1.6759i | 1.0097 |
| 1.5443 - 5.0094i | 1.0112 |
| 1.4279 - 4.0956i | 0.9938 |
| 1.6077 - 4.8491i | 1.0110 |
| 5.2963 - 14.1159i | 0.9922 |
| 1.0310 - 4.1223i | 1.0096 |
| 3.2349 - 9.5033i | 1.0055 |
| 4.2644 - 14.0424i | 0.9979 |
| 2.1751 - 5.9006i | 0.9758 |
| 1.5164 - 5.1666i | 1.0074 |
| 2.7847 - 8.2039i | 0.9749 |
| 4.6436 - 16.2812i | 1.0076 |
| 4.1406 - 21.1681i | 0.9964 |
| 2.6050 - 17.9710i | 1.0002 |
| 2.6921 - 14.3083i | 0.9967 |
| 3.2926 - 13.0793i | 0.9899 |
| 5.8773 - 15.2118i | 0.9902 |
| 4.1459 - 20.8194i | 0.9917 |
| 1.8325 - 7.3300i | 0.9948 |
| 4.8804 - 19.4813i | 0.9958 |
| 2.1604 - 8.4658i | 0.9931 |
| 4.3854 - 18.1333i | 0.9891 |
| 1.8487 - 7.3604i | 1.0150 |
| 1.3556 - 5.1270i | 1.0250 |
| 4.6948 - 14.0845i | 1.0160 |
| 2.2695 - 2.6877i | |
| 1.0313 - 2.6339i | |
| 2.7922 - 10.0847i | |
| 1.1657 - 2.6998i | |
| 6.3532 - 19.0194i | |
| 2.2994 - 7.4099i | |

Table3. Bus Data

| Bus | Type | Vsp | theta | PGi | QGi | PLi | QLi |
|---|---|---|---|---|---|---|---|
| 1 | 3 | 0.984 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 2 | 3 | 0.9602 | 0.00 | 0.00 | 0.00 | 0.1032 | 0.0288 |
| 3 | 3 | 1.0086 | 0.00 | 0.00 | 0.00 | 0.1431 | 0.0563 |
| 4 | 3 | 1.0087 | 0.00 | 0.00 | 0.00 | 0.1834 | 0.0774 |
| 5 | 3 | 0.9921 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 6 | 3 | 1.0092 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 7 | 3 | 0.9917 | 0.00 | 0.00 | 0.00 | 0.2410 | 0.1163 |
| 8 | 3 | 1.0082 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 9 | 3 | 1.0033 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 10 | 3 | 0.9945 | 0.00 | 0.00 | 0.00 | 0.112 | 0.0518 |
| 11 | 3 | 0.9741 | 0.00 | 0.00 | 0.00 | 0.1024 | 0.0294 |
| 12 | 3 | 1.0009 | 0.00 | 0.00 | 0.00 | 0.1291 | 0.0367 |
| 13 | 3 | 0.9732 | 0.00 | 0.00 | 0.00 | 0.1041 | 0.0421 |
| 14 | 3 | 0.9917 | 0.00 | 0.00 | 0.00 | 0.1235 | 0.0467 |
| 15 | 3 | 0.9873 | 0.00 | 0.00 | 0.00 | 0.0812 | 0.0255 |
| 16 | 3 | 0.9944 | 0.00 | 0.00 | 0.00 | 0.0731 | 0.0475 |
| 17 | 3 | 0.9915 | 0.00 | 0.00 | 0.00 | 0.1122 | 0.0475 |
| 18 | 3 | 0.9831 | 0.00 | 0.00 | 0.00 | 0.1122 | 0.0475 |
| 19 | 3 | 0.9843 | 0.00 | 0.00 | 0.00 | 0.0612 | 0.0172 |
| 20 | 3 | 0.9871 | 0.00 | 0.00 | 0.00 | 0.1423 | 0.0573 |
| 21 | 3 | 0.9912 | 0.00 | 0.00 | 0.00 | 0.0552 | 0.0552 |
| 22 | 3 | 0.9922 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 23 | 3 | 0.9853 | 0.00 | 0.00 | 0.00 | 0.0923 | 0.0342 |
| 24 | 3 | 0.9848 | 0.00 | 0.00 | 0.00 | 0.0782 | 0.0232 |
| 25 | 2 | 1.0150 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 26 | 2 | 1.0250 | 0.00 | 0.1073 | 0.0342 | 0.00 | 0.00 |
| 27 | 2 | 1.0160 | 0.00 | 0.1192 | 0.0362 | 0.00 | 0.00 |
| 28 | 2 | 1.0212 | 0.00 | 0.0993 | 0.0483 | 0.00 | 0.00 |
| 29 | 2 | 1.0123 | 0.00 | 0.00 | 0 | 0.00 | 0.00 |
| 30 | 1 | 1.0500 | 0.00 | 0.00 | 0 | 0.00 | 0.00 |

# 7. CONCLUSIONS

This work presents the successful analysis on voltage stability using Fuzzy Based and performs satisfactorily on power systems under all possible conditions such as increased load and line compensation with series and shunt capacitances for both in off-line and on- line simulation applications. The shortcomings of previous methods are overcome and consistent results are obtained. Though the number of iterations is more in fuzzy logic load flow method, the proposed algorithm does not require the factorization, refactorization and computation of Jacobin matrix at each iteration which shows the validity of the proposed algorithm. In the proposed model, more than one controlling devices are likely to be selected for coordinated control. Therefore, robust voltage control can be easily accomplished by the proposed model. Simulation results of the application example show that the proposed voltage control will lead as closely as possible to the desired system conditions and flexible operation of the controlling devices is realized by employing the fuzzy model, the problem can be solved simply by applying the max and min-operations. By defining certain fuzzy variables, the operator's intuition in operating a power system is more pertinently reflected. This method enables the system engineers to have coordinated variable control for satisfactorily operating the system. Besides, owing to its much less computational requirements, the method can be applied on line in this paper, the method for successful capacitor placement with the objective function of active power losses reduction together with cost-benefit analysis was proposed. The method was implemented on the example of real power grid of one of the Georgian regions. As we could observe from our iterations, in case if we make investments for addition of reactive power in power system for loss reduction objective, reduced losses will easily recover investment costs caused due to the capacitors addition. However this was not true for all the cases in our iterations and some cases were not successful and effective. Our iterations, made on real power grid shows, that in some cases even though the losses are reduced, the investment cost could be so high, that economically it becomes not effective to implement such changes. Especially it is true when we maximally reduce losses and for this we need to apply many sources of reactive power in different locations of the grid. In such case it becomes even more difficult to operate the number of capacitors as with connection and disconnections of reactive power sources many factors of power system should be considered. However in our iterations we made assumptions regarding the time for the investment recovery, average peak-hours per day and number of peak-hour days per year as well as the investment cost for reactive power support addition. If we change these assumptions, then the results of cost-benefit comparisons will change and unsuccessful iterations could become successful or vice versa. Also our suggested method of reactive power addition for the loss reduction purpose becomes even more effective and economically worthwhile in power systems with higher loads and where peak-hour operations are longer. For being able to significantly improve the performance of power systems and to reduce losses, reactive power should be applied properly and controlled.

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# EFFECT OF TEMPERATURE OF SYNTHESIS ON X-RAY, IR PROPERTIES OF MG-ZN FERRITES PREPARED BY OXALATE CO-PRECIPITATION METHOD

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***ABSTRACT***

*The magnetic properties of $Mg_{1-x}Zn_xFe_2O_4$ (where x = 0.3,0.4,0.5,0.6) ferrites have been studied. Magnesium Zinc Ferrites was synthesized by oxalate co-precipitation method at different synthesis temperature and characterized by X-ray diffraction and far IR absorption techniques, scanning Electron microscopy .Far infrared absorption spectra show two significant absorption bands ,first at about 600 $cm^{-1}$ and second at about 425 $cm^{-1}$,which were respectively attributed to tetrahedral (A) and octahedral (B) sites of the spinel .The positions of the bands are found to be composition dependent and dependent on the temperature of synthesis. The force constants $K_T$ and $K_0$ were calculated and plotted against zinc concentration and temperature of synthesis. Composition dependent of force constants is explained on the basis of cation-oxygen bond distances of respective sites and cation distribution.*

***KEYWORDS:*** Polycrystalline ferrites, Oxalate precursor, IR absorption, X-ray diffraction, Cation distribution, force constants.

## I. INTRODUCTION

Polycrystalline ferrite materials have wide application range in the field of electronic and communication industries due to their interesting electrical and magnetic properties [1]. Infrared absorption spectroscopy is an important and non-destructive characterizing tool, which provides qualitative information regarding structural details of crystalline materials [2,3]. The results from IR absorption study can be used to interpret the electrical and magnetic properties of the ferrites [4]. The absorption bands from which the details regarding functional groups and their linkages can be explored, are found to be dependent on atomic mass, cation radius, cation-anion bond distances, cation distribution etc. Infrared spectral analysis have been carried out for several ferrites by Woldron (1955)[5] who reported two absorption bands within the wave numbers 800 – 200 $cm^{-1}$, which could respectively attributed to the tetrahedral and octahedral group complexes of the spinel structure. El Hitti et al (1996) [6] studied the IR absorption spectra of Ni-Zn-Mg ferrites and reported four absorption bands, out of which $\nu_1$ and $\nu_2$ are due to tetrahedral and octahedral sites and $\nu_3$ and $\nu_4$ are assigned to the vibrations in divalent metal ion-oxygen group complexes in octahedral site.[7] and mass of divalent cations [8] respectively. Kolekar et al (1994)[9] studied the $Gd^{3+}$ substituted cd-cu ferrite system by using IR absorption spectroscopy and the results showing the compositional dependent behaviour of force constant are attributed to the cation oxygen bond distances. The structural distortion in case of chromium substituted nickel ferrites was studied by Ghatage et al

(1996) [10] . The IR spectra of Cd, Co, Mg, Ni, Zn, Cu etc. containing ferrites have been reported (Srivastav and Srinivasan 1982; Nathwani and Darshane 1987) [11,12]. The synthesis of ferrites can be carried out using different methods but the low temperature synthesis and molecular level mixing is reported to be useful in obtaining desired magnetic properties and the reaction kinematics in a chemical process dependent on the temperature at which it is carried out.

The present study reports on the synthesis of Mg-Zn ferrite powders of controlled composition by oxalate co-precipitation method. The effect of synthesis temperature and process parameters on particle size and crystallinity has been investigated. In the present communication the results regarding IR absorption spectral analysis, magnetic properties and XRD of Mg-Zn ferrites are discussed.

## II. EXPERIMENTAL SETUP

The Mg Zn ferrites having general formula $Mg_{1-x}Zn_xFe_2O_4$ (where x= 0.3,0.4,0.5,0.6) were prepared by co-precipitation method at different reaction temperatures – room temperature ($38^0$C), below room temperature ($10^0$C) and above room temperature ($70^0$C). The AR grade Magnesium sulphate, zinc sulphate, and ferrous sulphate were weighed carefully on single pan microbalance (make – Conteque and L.C. – 0.001 gm) to have proper stoichiometric proportion required in the final product. The synthesis was carried out at room temperature ($38^0$C), in which 200ml distilled water was taken and sulphates of magnesium (mg), zinc (Zn), and ferrous (Fe) were added in stoichiometry proportion to the water at that temperature. A clear solution was obtained. Ammonium oxalate was taken in burette and was added drop by drop until the precipitation was completed. The chemical reactions can be given as,

1. $MgSO_4 + 2H_2O + C_2O_4 \longrightarrow MgC_2O_4 2H_2O + SO_4$

2. $ZnSO_4 + 2H_2O + C_2O_4 \longrightarrow ZnC_2O_4 2H_2O + SO_4$

3. $FeSO_4 + 2H_2O + C_2O_4 \longrightarrow FeC_2O_4 2H_2O + SO_4$

The precipitate was filtered through whatman filter paper No. 41. The filtrate was washed with distilled water to remove unreacted chemicals. The residue was checked for the absence of sulphates using Barium chloride test. The solution was maintained at same temperature. Similar reaction was carried out using ice bath below room temperature at $10^0$C and above room temperature at $70^0$C where the magnetic stirrer was maintained at $70^0$C to carry out the reaction. The precipitate was dried using electric lamp. The solid state reaction was carried out in muffle furnace maintained at $600^0$C for 6 hours, and the powders so obtained were finely ground using agate mortar to obtain fine powders. The pellets of diameter 1 cm and thickness 0.5 cm were formed with the hydraulic press at the pressure of 9 kg/cm$^2$ for five minutes, for the study of saturation magnetization. The palletized samples were finally heated in a furnace at $700^0$C for 7 hours, for hardening. Oxalates in precursor act like a combustion agent which helps in lowering the calcinations temperature. Therefore the solid state reaction to obtain the ferrites was carried out in muffle furnace at optimized temperature of $600^o$C for 6 Hrs for all samples irrespective of the oxalate reaction temperature.

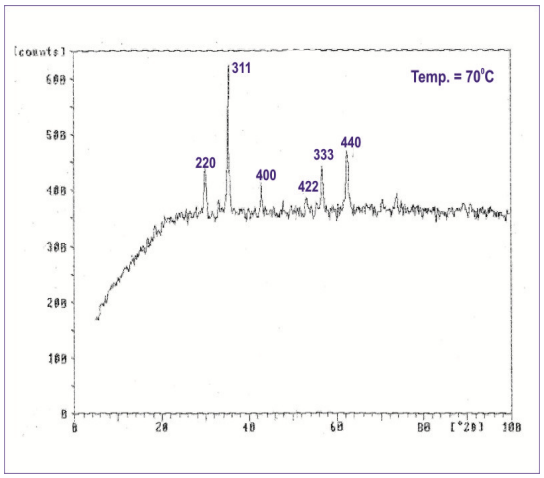
X-ray diffractgrams of all the samples were recorded with Philips make PW 1710 powder diffractometer by continuous scanning in the range of $2\theta^0$ to $85\theta^0$ using CuK$\alpha$ radiation. The x-ray tube was excited at 40kV and 40mA. IR spectrographs were taken using SHIMATZU (FTIR-8400S) spectrometer by using IR spectrometer in the range of 200 cm$^-$1 to 800 cm$^{-1}$. The spectrum, transmittance (%) against wavenumber (cm$^{-1}$) is used for interpretation of the results.

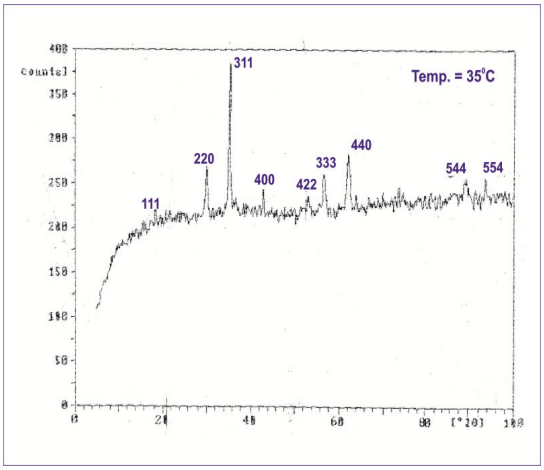
## III. RESULT AND DISCUSSION:

The X-Ray diffraction patterns obtained for the samples $Mg_xZn_{1-x}Fe_2O_4$ using Cu K$\alpha$ radiation ($\lambda$ = 1.5418 AU) are shown in Fig 1 to 4. The (h,k,l) values which diffracts in X-ray spinels are (220), (311), (400), (422), (333) and (400) . All the planes are the allowed planes, which indicate the formation of single-phase cubic spinel structure [13].The lattice parameter were calculated using the

standard relation [14] for the cubic system and presented against composition and temperature of synthesis shown in fig. 5 and 6.

X = 0.3



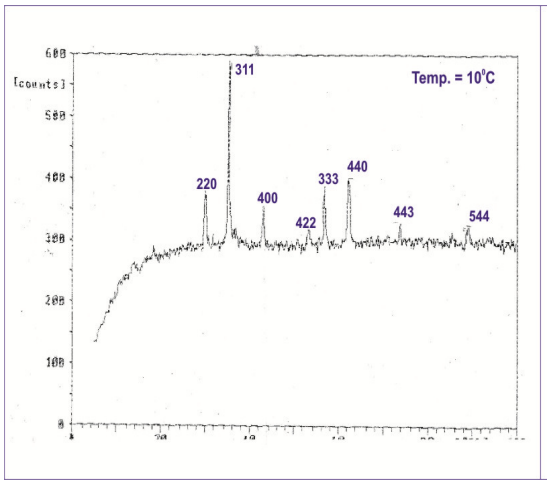
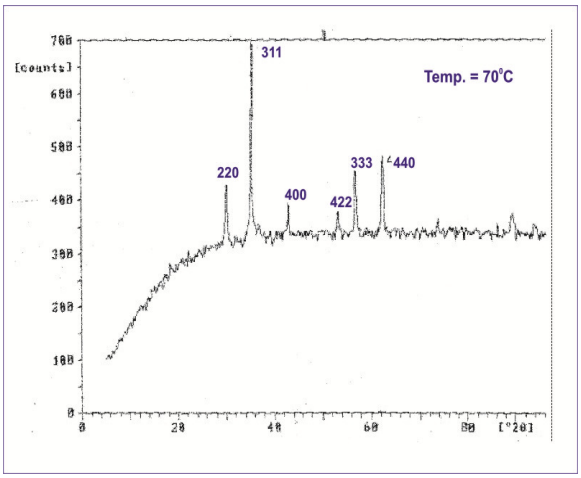
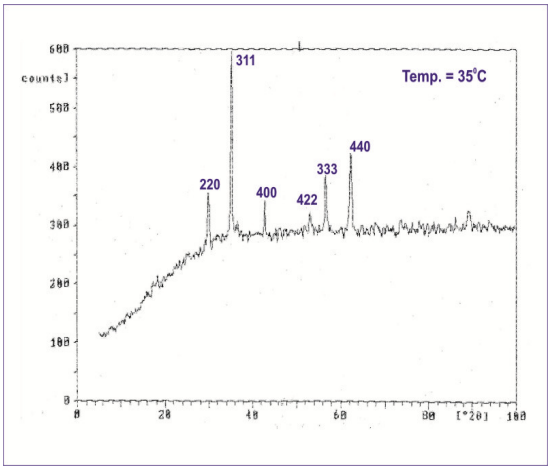




Figure 1-Variation of most intense (311) peak with temperature of chemical reaction for the composition x = 0.3

X= 0.4



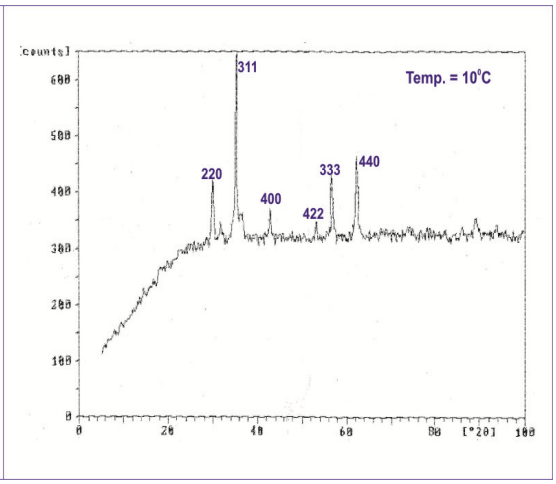
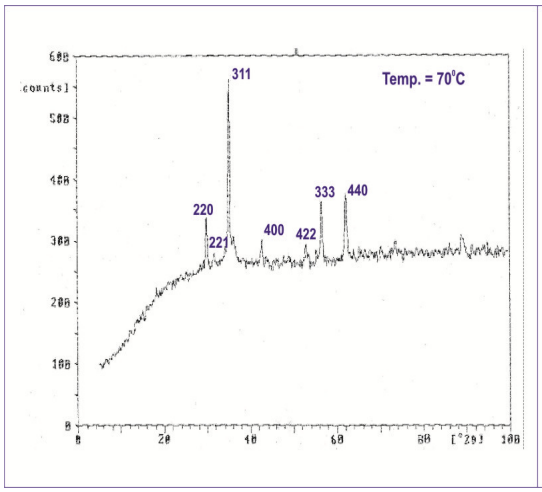
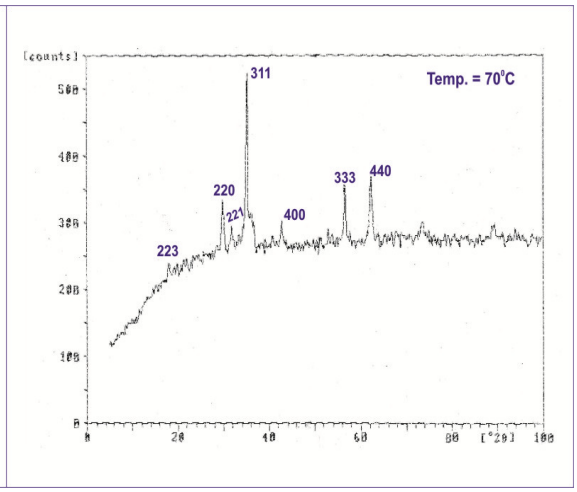
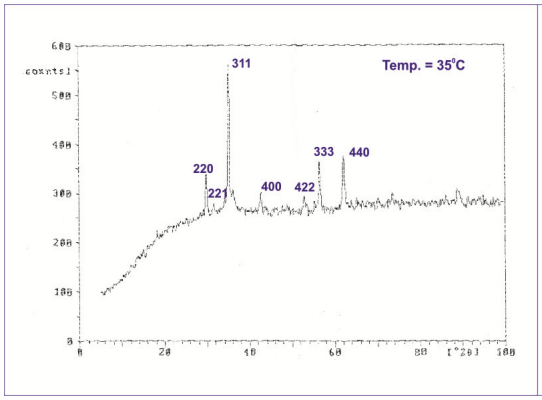
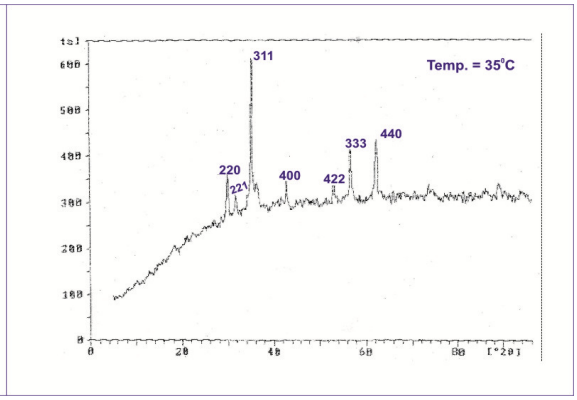



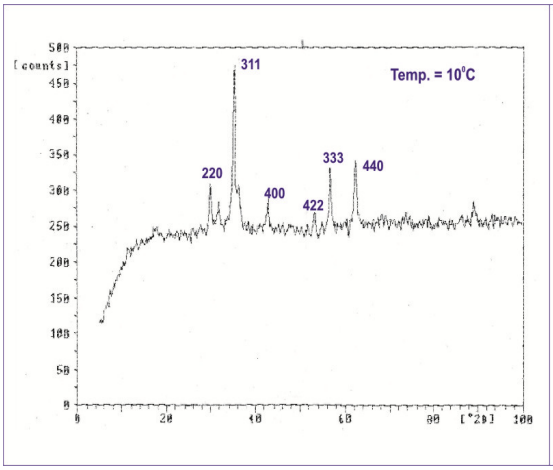

Figure 2 -Variation of most intense (311) peak with temperature of chemical reaction for the composition x = 0.4



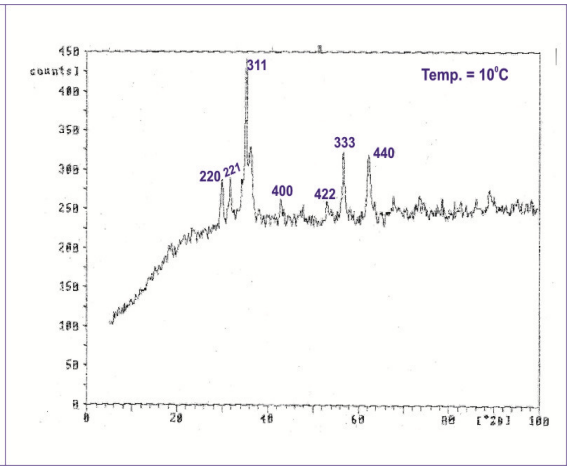




Figure 3 -Variation of most intense (311) peak with temperature of chemical reaction for the composition x = 0.5

Figure 4 -Variation of most intense (311) peak with temperature of chemical reaction for the composition x = 0.6

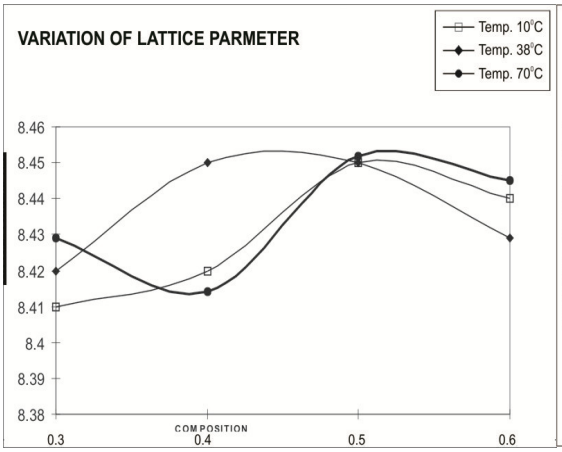



Figure 5- Variation of lattice parameter with composition

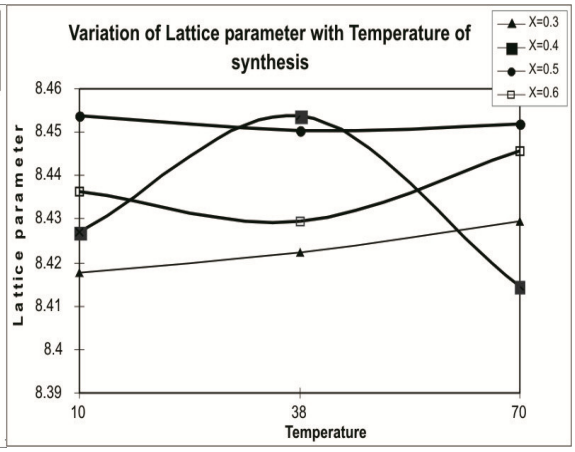



Figure 6- Variation of lattice parameter with temperature of synthesis.

The lattice parameter obtained using the XRD data is found to be in the range 8.42A° to 8.45 A°. The variation may be attributed to the ionic size difference between $Mg^{2+}$(0.06 nm) and $Zn^{2+}$ ion (0.074 nm) where $Zn^{2+}$ ion replaces $Mg^{2+}$ ion on B site. For high concentration of Zinc (X=0.6), the lattice parameter is found to decrease, which may be attributed to shifting on some $Fe^{3+}$ ions from A site to B site for higher composition [13]. The Temperature of synthesis does not seem to show variation in lattice parameter indicating that the range of temperature chosen for synthesis does not appreciably affect the lattice parameter. From Fig. 5 it can be seen that the samples synthesized at room temperature shows largest values for lattice parameter.

Infrared absorption spectra for the sample $Mg_{1-x}Zn_XFe_2O_4$ under investigation obtained using IR spectrophotometer and the variation of $\nu_1$ and $\nu_2$ bands with composition at different reaction temperatures is shown in Figure 7.These spectra show two strong absorption bands at the frequency about (600 $cm^{-1}$ and 400 $cm^{-1}$) for all the compositions. The absorption bands observed within these specific frequency limits reveal the formation of single-phase spinel structure having two sublattices, tetrahedral (A) site and octahedral (B) site [9].

The absorption band, $\nu_1$ observed at about is 600 $cm^{-1}$ is attributed to the tetrahedral site whereas that of $\nu_2$ observed at about 420 $cm^{-1}$ is assigned to octahedral group complexes. The position of absorptions bands and wave numbers are presented in the fig. 7, 8 ,9 , it is found that the positions of bands are composition dependent. The wave number of band $\nu_1$ shifts towards higher values with increasing zinc concentration (x). This variation in the band positions may be due to variations in the cation-oxygen bond length (A-0) [9]. Zinc ion, which when substituted, resides on tetrahedral (A) site, displacing proportional amount of $Fe^{2+}$ ion from A to B site [14]. This leads to increase in the cation oxygen bond length of tetrahedral lattice site (A) of Spinel [14].The position of $\nu_2$ band is seen to be independent of composition, which suggests the occupancy of cations of different characters on the same site [15].

The force constants for tetrahedral ($k_t$) and Octahedral site ($K_o$) , have been calculated by using the method suggested by Woldron [5]. The values of force constants as a function of Zn concentration have been estimated using the cation distribution depicted in table 1,in accordance with the observed values of magnetic moment are given in table1.

Table 1 Magnetic moment, cation distribution

| Sr. No | Conc. Zn | Cation distribution | | μB (Observed) | μB (Calculated) |
|---|---|---|---|---|---|
| 1 | 0.3 | $[Zn_{0.01}Fe_{0.99}]^A$ | $[Mg_{0.7}Zn_{0.29}Fe_{1.01}]^B$ | 0.15 | 0.11 |
| 2 | 0.4 | $[Zn_{0.013}Fe_{0.987}]^A$ | $[Mg_{0.6}Zn_{0.387}Fe_{1.013}]^B$ | 0.27 | 0.23 |
| 3 | 0.5 | $[Zn_{0.016}Fe_{0.984}]^A$ | $[Mg_{0.5}Zn_{0.484}Fe_{1.016}]^B$ | 0.14 | 0.19 |
| 4 | 0.6 | $[Zn_{0.02}Fe_{0.98}]^A$ | $[Mg_{0.4}Zn_{0.58}Fe_{1.02}]^B$ | 0.12 | 0.12 |

On inspection of figure 8,9**.** It is seen that the force constant of tetrahedral site ($k_t$) decreases with increasing zinc concentration. This behavior can be attributed to the variation in cation oxygen bond lengths. The octahedral force constant ($K_o$) is found to increase up to X=0.4 and then it becomes constant on $Zn^{2+}$ substitution, which supports Zn $^{2+}$on B site [16]. The increase in force constant is associated with increase in lattice parameter. The value of magnetic moment is greater for X=0.4 compositions and then it decreases due to the canted spin [17].The Temperature of synthesis does not seem to show variation in force constant indicating that the range of temperature chosen for synthesis does not appreciably affect the force constant.

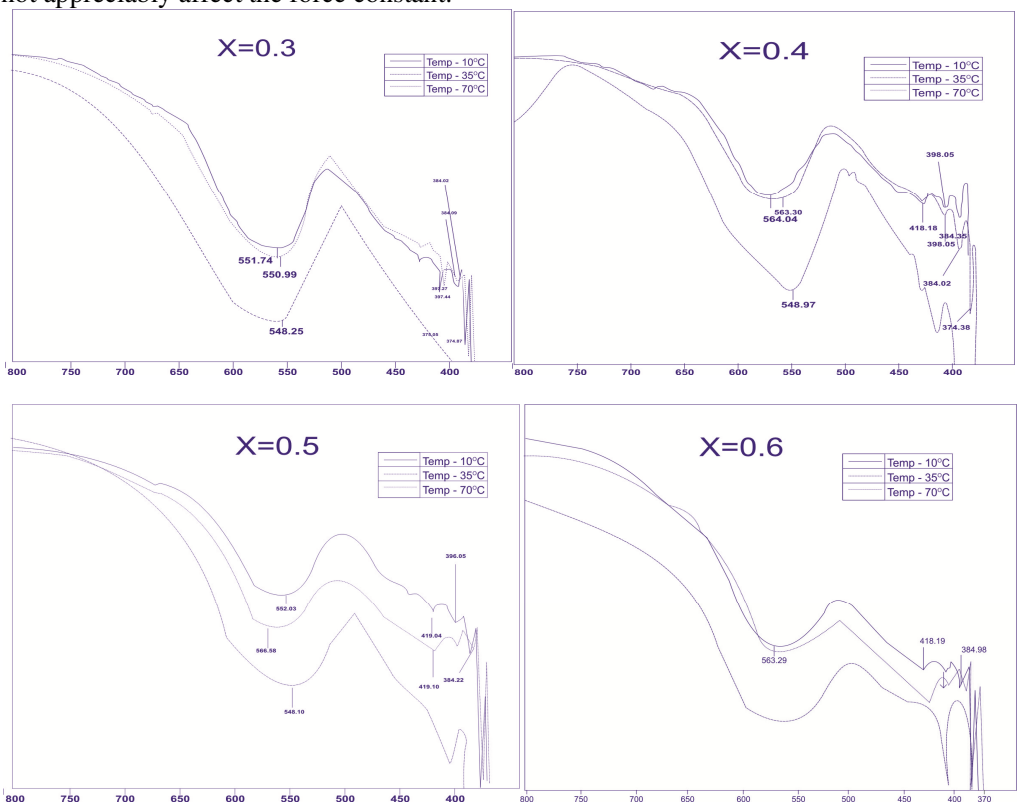
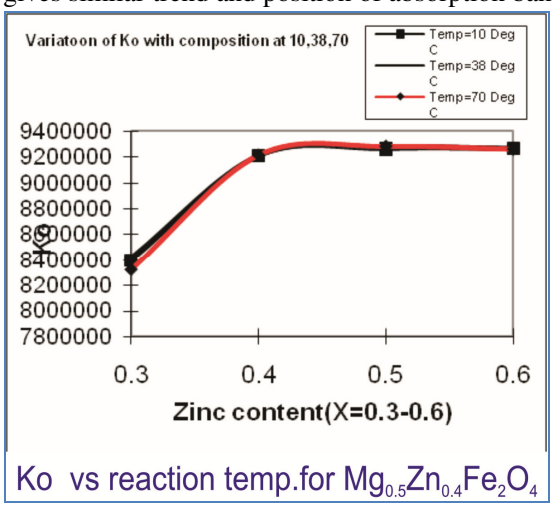



Figure7- Infrared Absorption spectra for the system $Mg_{1-x}Zn_xFe_2O_4$ for X= 0.3 -0.6

Ladgaonkar et.al [16] have synthesized the sample at temperature above 1000ºC and obtained the values $\nu_1$ ,$\nu_2$ in the range 585cm$^{-1}$ to 555 cm$^{-1}$ and force constant in the range 2.5X10$^5$ dyne/cm -- 2.4X10$^5$ dyne/cm. Mazen et.al[13] have synthesized the sample at temperature above 1000 ºC and obtained the lattice parameter 8.41°A,also Pradeep et.al[18], Joshi et.al[19], A.Vital et.al [20], Bhosale et.al [21], have observed similar trend of results and they have synthesized the sample at higher temperature. Whereas in the present case the samples have been synthesized below 100ºC but

the force constant showing similar trend. Hence it can be concluded that room temperature synthesis gives similar trend and position of absorption band to other reported value.



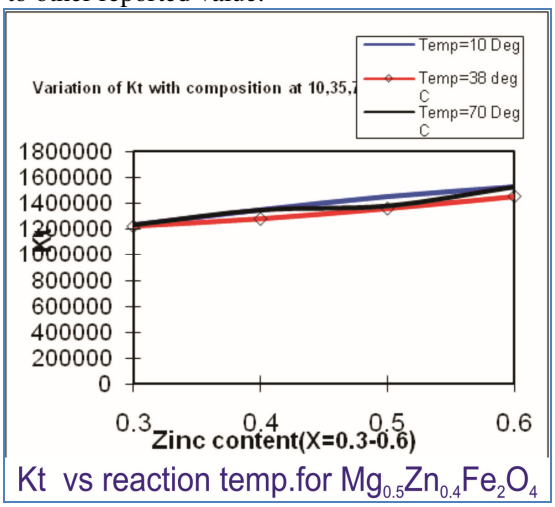




Figure 8- Variation of Kt and Ko verses reaction temperature $Mg_{1-x}Zn_xFe_2O_4$ for X= 0.3 -0.6

## IV. CONCLUSION

Infrared absorption spectra of the compositions under investigation reveal formation of single phase cubic spinel, showing two significant absorption bands. The position of absorption bands are compositional dependent, whose dependence could be attributed to the variation in cation oxygen bond distances. Variations in the force constants of tetrahedral and octahedral sites support predicted cation distribution, wherein $Zn^{2+}$ ion gets preferentially distributed among A and B sites and Mg occupies B site.

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# AN IMPROVED ENERGY EFFICIENT MEDIUM ACCESS CONTROL PROTOCOL FOR WIRELESS SENSOR NETWORKS

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## *ABSTRACT*

*Wireless Sensor Networks (WSN) constitute a special class of wireless data communication networks. In wireless sensor networks, sensor nodes are randomly deployed. Since the sensor nodes are required to operate under remote conditions without fresh supply of power to replenish itself, energy conservation becomes the major constraint. This necessitates the design of WSNs with the capability of prolonging the lifetime of network. To achieve minimum energy consumption, several MAC protocols have already proposed. This paper aims to survey and analyze the most energy efficient medium access control protocols and to compare their performances. Further, this paper proposes a new MAC protocol based on Orthogonal Frequency Division Multiplexing (OFDM).In ELE-MAC protocol, by employing OFDMA the energy consumption of the node can be minimized.*

***KEYWORDS:*** *Wireless Sensor Networks, Media Access Control, Energy, Sensor MAC, Orthogonal Frequency Division Multiplexing.*

## I. INTRODUCTION

Wireless *ad hoc* sensor network is an emerging technology that promises a great potential for both military and civilian applications. Such a network can be used to monitor environment, detect, classify, and locate objects and then track them over a specified region.

The sensor network is expected to deploy varying number of sensor nodes that can sense the environment using different modalities such as acoustic, seismic, and infrared. The sensors also have the capability to communicate and interact with neighboring sensors via wireless channels and also they are able of processing the information. It is expected that these components can be integrated into a tightly packed, low cost sensor nodes ready for massive deployment.

For military applications, these low-cost, integrated wireless sensor nodes can be rapidly deployed by air over remote regions to monitor vehicles and personnel movements and to relay the findings back to the command center on a real-time basis.

Research and Development on sensor networks relies on many concepts and protocols from distributed computer networks, such as Internet. However, several technical challenges in sensor networks need to be addressed due to the specialized nature of the sensors and the very fact that many sensor network applications may involve remote mobile sensors with limited power sources that must dynamically adapt to their varying environment. As the field of communication networks continues to evolve, a very interesting and challenging area of WSN is rapidly coming of age.

The basic issue in communication networks is the transmission of messages to achieve a prescribed message throughput (Quantity of Service) and Quality of Service (QoS). QoS can be specified in terms of message delay, message due dates, bit error rates, packet loss, economic cost of transmission,

transmission power, etc. This necessitates suitable MAC protocol to transmit packets over a shared channel.

### 1.1 Issues in Medium Access Scheme

The primary responsibility of a MAC protocol in WSN is the distributed arbitration[1]for the shared channel for transmission of packets. The major issues to be considered in designing a MAC protocol for WSNs are as follows.

#### 1.1.1 Distributed Operation

WSNs need to operate in environments where no centralized coordination is possible. MAC protocol design should be fully distributed involving minimum control overhead.

#### 1.1.2 Synchronization

Time synchronization is needed for TDMA based systems to manage transmission and reception slots. It involves usage of scarce sources such as bandwidth and battery power.

#### 1.1.3 Hidden Terminals

MAC protocol should be able to alleviate the effects of hidden terminals. In addition to the above said issues, MAC protocol is to be designed in such a way that it should minimize the access delay and maximize the throughput.

The remainder of the presentation is organized as follows. In section 2, we provide a review of the related work. Section 3 discusses various existing MAC protocols. A new energy efficient multiple access scheme is proposed in section 4.Simulation results of various MAC protocols are given in section 5. Section 6 concludes the paper.

## II. RELATED WORK

When multiple nodes desire to transmit, protocols are needed to avoid collisions and data loss. In the 1970's at the University of Hawaii, ALOHA scheme was first used. In this ALOHA scheme, a node simply transmits a message when it desires [1]. If it receives an acknowledgement, all is well. If not, the node waits for a random time and retransmits the message. However, its simplicity comes at an expense of very high probability of a packet collision. It increases the energy expenditure due to packet retransmission. Therefore, Carrier Sense Multiple Access (CSMA) protocol was developed [2] with the objective of minimizing collision by implementing a small time for channel listening in order to detect channel activity. However, the protocol cannot solve the hidden terminal problem which normally occurs in ad-hoc networks where the radio range is not large enough to allow communication between arbitrary nodes. Further, two or more nodes may share a common neighbor while being out of each other's reach. The MAC protocol introduces a three-way handshake mechanism to make hidden nodes aware of upcoming transmission from neighboring nodes and hence collision may be avoided. However, the handshaking mechanism causes overhead on control packets.

In Frequency Division Multiple Access (FDMA), different nodes have different carrier frequencies. Since, the frequency resources are divided, the bandwidth available for each node decreases [3]. FDMA also requires additional hardware and intelligence at each node.

In Code Division Multiple Access (CDMA), a unique code is used by each node to encode its messages. This increases the complexity of the transmitter and the receiver.

In Time Division Multiple Access (TDMA), the RF link is divided on a time axis with each node being given a predetermined time slot that can be used for communication. This decreases the sweep rate, but a major advantage is that TDMA can be implemented in software. All nodes require accurate, synchronized clocks for TDMA. Meanwhile, software power management techniques can greatly decrease the power consumed by RF sensor nodes. TDMA is especially useful for power conservation, since a node can power down or 'sleep' between its assigned time slots, waking up in time to receive and transmit messages [4]. The required transmission power increases as the square of the distance between source and destination.

Therefore, multiple short message transmission hops require less power than one long hop. In fact, if the distance between source and destination is *R*, the power required for single-hop transmission is

proportional to $R^2$. If nodes between source and destination are taken advantage of, to transmit *n* short hops instead, the power required by each node is proportional to $R^2/n^2$. This is a strong argument in favor of distributed networks with multiple nodes, *i.e.* nets of the mesh variety.All these protocols require all nodes to continuously listen to the channel due to unpredictable packet transmission by its neighboring nodes.

# III. MULTIPLE ACCESS PROTOCOLS

Media Access Control (MAC) layer manages the medium accessibility to minimize collision among transmitting packets. Packet collision requires node to retransmit the packet and hence consumes additional energy. MAC layer controls the physical layer (radio transceiver) which has greater effect on the overall energy consumption and lifetime of a node.

## 3.1 Energy Efficient MAC Protocols

If all nodes continuously listen to the channel due to unpredictable packet transmission by its neighboring nodes, hence introducing a problem called idle listening [5]. This situation causes a node to waste energy unnecessarily and thus making the implementation of these protocols in Wireless Sensor Networks inefficient.

### 3.1.1 Sensor MAC Protocols (SMAC)

This protocol solves the idle listening problem by introducing an active sleep cycle. Locally managed synchronization and periodic sleep listen schedules based on these synchronizations form the basic idea behind the Sensor MAC protocol [6]. Neighboring nodes form virtual clusters so as to set up a common sleep schedule. If two neighboring nodes reside in two different virtual clusters, they wake up at the listen periods of both clusters.

Periodic sleep may result in high latency, especially for multi-hop routing algorithms, since all intermediate nodes have their own sleep schedules [7]. The latency caused by periodic sleeping is called sleep delay. Another drawback of this protocol is sleep and listen periods are predefined and constant, which decreases the efficiency of the algorithm under variable traffic load.

### 3.1.2 Adaptive SMAC Protocols (ASMAC)

The great energy cost associated with idle time and overhearing suggests that optimizations must turn off the radio not simply reduce packet transmission and reception. This protocol reduces the listen time by putting nodes into periodic sleep state. Each node sleeps for predefined time and then wakes up and listens to see if any other node wants to talk to it. During sleeping, the node turns off its radio and sets a timer to wake it up later.

All nodes are free to choose their own listen-sleep schedules. In order to reduce control overhead, neighboring nodes are synchronized together. That is, they listen at the same time and go to sleep at the same time. In ASMAC, nodes coordinate their sleep schedules rather than randomly sleep on their own. This protocol also presents a technique to reduce latency due to periodic sleep on their own. This protocol also presents a technique to reduce latency due to periodic sleep on each node.

Before each node starts its periodic listen and sleep, it needs to choose its schedule and exchange it with the neighbors [8]. Each node maintains a schedule table that stores the schedule of all its known neighbors.

### 3.1.3 Energy Latency Efficient MAC Protocols (ELE-MAC)

The basic idea of this protocol is to minimize the control packets exchanged in the ASMAC protocol. At the same time, ELE-MAC should conserve the SMAC's benefits. Here personalized Request to Send (RTS) packet is adopted. Further, this packet provides two additional fields called Acknowledgement destination node address and Acknowledgement flag [8]. This added fields allow the new RTS packet to play the role of an ACK and RTS same time. This new packet will be exchanged only when data are sent adaptively. Thus, no ACK packet will be emitted in that case. Else-where, the transmission is performed normally. In other words, each data packet received is followed by an ACK to the sender.

In this protocol, adaptive wake up period starts immediately after receiving the data packet instead of waiting for the ACK packet like ASMAC protocol. This modification is made for allowing a receiver to inform its neighbors about the data reception through the ACK flag field. Also, this packet allows the receiver to mention its need to transmit the received packet to the next hop, if it exists.
ELE-MAC does not propose a fragmentation mechanism, like SMAC. It broadcasts packets only when virtual and physical carrier sense indicates that the medium is free[9]. In addition, these packets will not be preceded RTS/CTS and will not be acknowledged by their recipients.

# IV. PROPOSED SCHEME

In order to satisfy the design requirements of WSN, a new Multiple Access based scheme called Orthogonal Frequency-Division Multiplexing (OFDM) is used along with ELE-MAC.
OFDM is essentially identical to Coded OFDM (COFDM), It is a digital multi-carrier modulation scheme that uses a large number of closely-spaced orthogonal sub-carriers to carry data. These sub-carriers typically overlap in frequency but are designed not to interfere with each other as would be the case with traditional FDM. This may be efficiently separated using a Fast Fourier Transform (FFT) algorithm [10]. Each subcarrier is modulated with a conventional modulation scheme (such as quadrature amplitude modulation) at a low symbol rate maintaining data rates similar to conventional single-carrier modulation schemes in the same bandwidth.
The primary advantage of OFDM over single-carrier schemes is its ability to cope with severe channel conditions .For example, attenuation of high frequencies in a long copper wire, narrow band interference and frequency-selective fading due to multipath without complex equalization filters. Channel equalization is simplified because OFDM may be viewed as using many slowly-modulated narrow band signals rather than one rapidly-modulated wide band signal. The low symbol rate makes the use of a guard interval between symbols affordable, making it possible to handle time-spreading and eliminate Inter Symbol Interference (ISI).

## 4.1 Subcarrier Based OFDM

If we consider a multiuser subcarrier, bit and power allocation scheme, where all users transmit in all the available time slots. Our objective is to minimize the overall transmit power by allocating the subcarriers to the users and by determining the number of bits and the power level transmitted on each subcarrier based on the instantaneous fading characteristics of all users. We formulate the multiuser subcarrier, bit and power allocation problem and propose an iterative algorithm to perform the multiuser subcarrier allocation. Once the subcarrier allocation is determined, the bit and power allocation algorithm can be applied to each user on its allocated subcarriers.

## 4.2 Sub- Band Based OFDM

For “subcarrier-to-subcarrier” allocation algorithm, different number of bit or power may be allocated to different subcarriers; the computational complexity overhead may be too large to bear for OFDM systems with large number of subcarriers. To decrease the computational complexity overhead, sub band based bit and power allocation algorithm are developed.

## 4.3 Orthogonality and OFDM

If the FDM system above had been able to use a set of subcarriers that were orthogonal to each other, a higher level of spectral efficiency could have been achieved. The guard bands that were necessary to allow individual demodulation of subcarriers in an FDM system would no longer be necessary [10]. The use of orthogonal subcarriers would allow the subcarriers’ spectra to overlap, thus increasing the spectral efficiency. As long as orthogonality is maintained, it is still possible to recover the individual subcarriers’ signals despite their overlapping spectrums. If the dot product of two deterministic signals is equal to zero, then these two signals are said to be orthogonal to each other. Orthogonality can also be viewed from the standpoint of stochastic processes. If two random processes are uncorrelated, then they are orthogonal. Given the random nature of signals in a communications system, this probabilistic view of orthogonality provides an intuitive understanding of the implications of orthogonality in OFDM. Later in this article, we will discuss how OFDM is implemented in practice using the discrete Fourier transform (DFT). From a basic knowledge of signals and systems,

the sinusoids of the DFT form an orthogonal basis set and a signal in the vector space of the DFT can be represented as a linear combination of the orthogonal sinusoids. One view of the DFT is that the transform essentially correlates its input signal with each of the sinusoidal basis functions. If the input signal has some energy at a certain frequency, there will be a peak in the correlation of the input signal and the basis sinusoid that is at that corresponding frequency. This transform is used at the OFDM transmitter to map an input signal onto a set of orthogonal subcarriers, i.e., the orthogonal basis functions of the DFT. Similarly, the transform is used again at the OFDM receiver to process the received subcarriers. These signals from the subcarriers are then combined to form an estimate of the source signal from the transmitter. The orthogonal and uncorrelated nature of the subcarriers is exploited in OFDM with powerful results. Since the basis functions of the DFT are uncorrelated, the correlation performed in the DFT for a given subcarrier only sees energy for that corresponding subcarrier. The energy from other subcarriers does not contribute because it is uncorrelated. This separation of signal energy is the reason that the OFDM subcarriers' spectrums can overlap without causing interference.

Orthogonal property can be mathematically represented as follows.

For Continuous Time signals:

$$\int_0^T \cos(2\pi nf0t) \times \cos(2\pi mf0t)dt = 0\ (n \neq m) \quad \text{---------- (1)}$$

For Discrete Time signals:

$$\sum_{k=0}^{N-1} \cos(\frac{2\pi kn}{N}) \times \cos\left(\frac{2\pi km}{N}\right) = 0\ (n \neq m) \quad \text{---------- (2)}$$

The carriers of an OFDM system are sinusoids that meet this requirement because each one is a multiple of a fundamental frequency. Each one has an integer number of cycles in the fundamental period.

## V. RESULTS AND DISCUSSIONS

This section describes the performance metrics of various MAC protocols. We simulated SMAC, ASMAC and ELE-MAC using Ns-2 with the defined topologies for our scenario with three parameters i.e., number of nodes **N**, maximum transmission radius **R** and side-length of the square area **L.** Another parameter defined in the topology is its density ***d***, which is defined as the average number of neighbors per node. Then, generate a network with parameters $N = 80, R = 30m$ *and* $L = 120m$. From Figures 1 and 2, it is clear that ELE-MAC protocol consumes less energy and offer low latency delay than ASMAC and SMAC protocols.

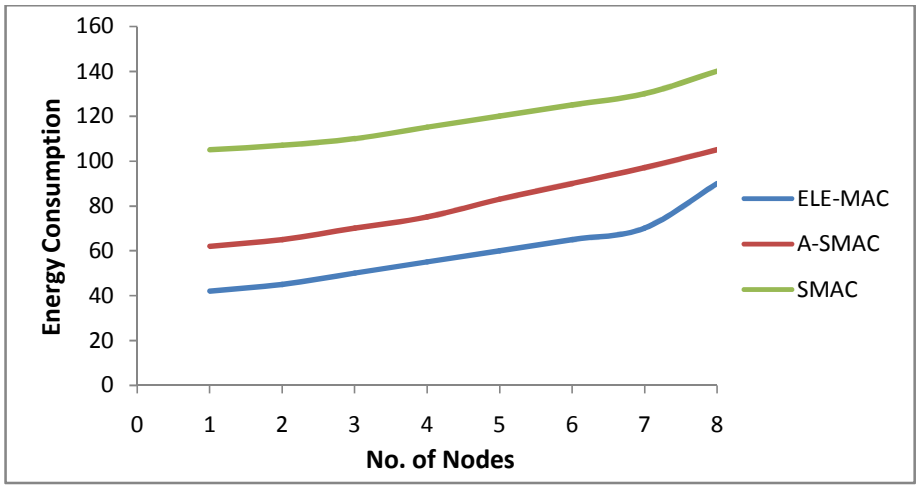


Fig.1: Energy Consumption Performance

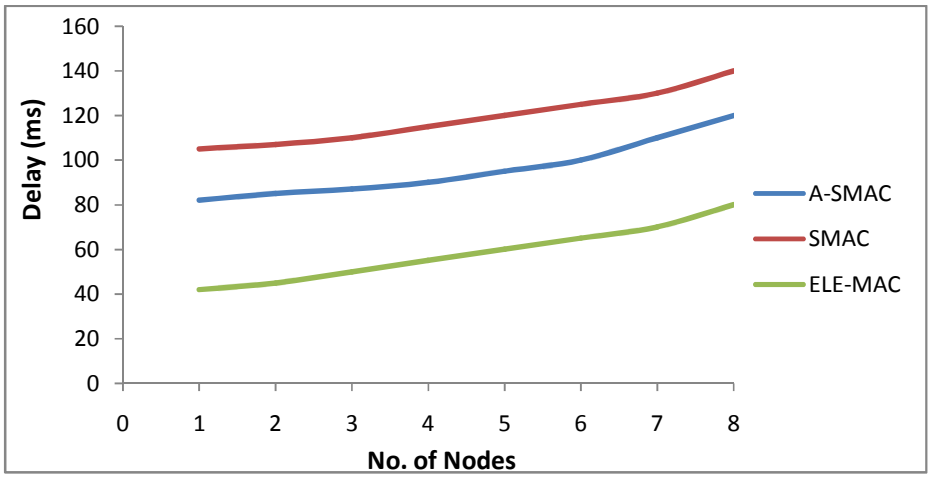


Fig.2: Energy Latency Performance

# VI. CONCLUSION

This paper focuses the MAC issues in the context of minimum energy consumption and less delay in wireless sensor networks. Three energy efficient MAC protocols were studied and their performances were analyzed by implementing these MAC protocols using NS-2 simulator.
From this WSN MAC protocols survey, It has been emphasized that novel protocols and algorithms are needed to effectively tackle the application requirements of sensor networks. So, the design of optimal WSNMAC protocol is required to achieve minimum energy consumption and minimum delay. By using ELE-MAC along with OFDMA, the adjacent packets are transmitted with orthogonal nature; we may achieve better energy consumption.

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